CS 267
Dense Linear Algebra:
Parallel Gaussian Elimination

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Outline

• Review Gaussian Elimination (GE) for solving Ax=b
• Optimizing GE for caches on sequential machines
  - using matrix-matrix multiplication (BLAS and LAPACK)
• Minimizing communication for sequential GE
  - Not LAPACK, but Recursive LU minimizes bandwidth (latency possible)
• Data layouts on parallel machines
• Parallel Gaussian Elimination (ScaLAPACK)
• Minimizing communication for parallel GE
  - Not ScaLAPACK (yet), but "Comm-Avoiding LU" (CALLU)
  - Same idea for minimizing bandwidth and latency in sequential case
• Summarize rest of dense linear algebra
• Dynamically scheduled LU for Multicore
• LU for Heterogeneous computers (CPU + GPU)

Refine GE Algorithm (1)

• Initial Version

... for each column i
... zero it out below the diagonal by adding multiples of row i to later rows
for i = 1 to n-1
... for each row j below row i
for j = i+1 to n
... add a multiple of row i to row j
	tmp = A(j,i);
	for k = i to n
		A(j,k) = A(j,k) - (tmp/A(i,i)) * A(i,k)

... for each column i
... zero it out below the diagonal by adding multiples of row i to later rows
for i = 1 to n-1
... for each row j below row i
for j = i+1 to n
... add a multiple of row i to row j

tmp = A(j,i);
for k = i to n
A(j,k) = A(j,k) - (tmp/A(i,i)) * A(i,k)

... for each column i
... zero it out below the diagonal by adding multiples of row i to later rows
for i = 1 to n-1
... for each row j below row i
for j = i+1 to n
	tmp = A(j,i);
	for k = i to n
		A(j,k) = A(j,k) - m * A(i,k)

Remove computation of constant tmp/A(i,i) from inner loop.
Refine GE Algorithm (2)

- Last version

\[
\begin{align*}
&\text{for } i = 1 \text{ to } n-1 \\
&\quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad m = A(j,i)/A(i,i) \\
&\quad \quad \text{for } k = i+1 \text{ to } n \\
&\quad \quad \quad A(j,k) = A(j,k) - m \cdot A(i,k)
\end{align*}
\]

- Don’t compute what we already know: zeros below diagonal in column \( i \)

\[
\begin{align*}
&\text{for } i = 1 \text{ to } n-1 \\
&\quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad m = A(j,i)/A(i,i) \\
&\quad \quad \text{for } k = i+1 \text{ to } n \\
&\quad \quad \quad A(j,k) = A(j,k) - m \cdot A(i,k)
\end{align*}
\]

Refine GE Algorithm (3)

- Last version

\[
\begin{align*}
&\text{for } i = 1 \text{ to } n-1 \\
&\quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad m = A(j,i)/A(i,i) \\
&\quad \quad \text{for } k = i+1 \text{ to } n \\
&\quad \quad \quad A(j,k) = A(j,k) - m \cdot A(i,k)
\end{align*}
\]

- Store multipliers \( m \) below diagonal in zeroed entries for later use

\[
\begin{align*}
&\text{for } i = 1 \text{ to } n-1 \\
&\quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad A(j,i) = A(j,i)/A(i,i) \\
&\quad \quad \text{for } k = i+1 \text{ to } n \\
&\quad \quad \quad A(j,k) = A(j,k) - A(j,i) \cdot A(i,k)
\end{align*}
\]

Refine GE Algorithm (4)

- Last version

\[
\begin{align*}
&\text{for } i = 1 \text{ to } n-1 \\
&\quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad A(j,i) = A(j,i)/A(i,i) \\
&\quad \quad \text{for } k = i+1 \text{ to } n \\
&\quad \quad \quad A(j,k) = A(j,k) - A(j,i) \cdot A(i,k)
\end{align*}
\]

- Split Loop

\[
\begin{align*}
&\text{for } i = 1 \text{ to } n-1 \\
&\quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad A(j,i) = A(j,i)/A(i,i) \\
&\quad \quad \text{for } k = i+1 \text{ to } n \\
&\quad \quad \quad A(j,k) = A(j,k) - A(j,i) \cdot A(i,k)
\end{align*}
\]

Refine GE Algorithm (5)

- Last version

\[
\begin{align*}
&\text{for } i = 1 \text{ to } n-1 \\
&\quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad A(j,i) = A(j,i)/A(i,i) \\
&\quad \quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad \quad A(j,k) = A(j,k) - A(j,i) \cdot A(i,k)
\end{align*}
\]

- Express using matrix operations (BLAS)

\[
\begin{align*}
&\text{for } i = 1 \text{ to } n-1 \\
&\quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad A(j,i) = A(j,i)/A(i,i) \\
&\quad \quad \text{for } j = i+1 \text{ to } n \\
&\quad \quad \quad A(j,k) = A(j,k) - A(j,i) \cdot A(i,k)
\end{align*}
\]

\[
\begin{align*}
&\text{A(j+1:n,i) = A(j+1:n,i) * (1/A(i,i))} \\
&\quad \ldots \text{BLAS 1 (scale a vector)} \\
&\text{A(j+1:n,i+1:n) = A(j+1:n,i+1:n) - A(j+1:n,i) * A(i,j+1:n)} \\
&\quad \ldots \text{BLAS 2 (rank-1 update)}
\end{align*}
\]
What GE really computes

- Call the strictly lower triangular matrix of multipliers M, and let L = I+M
- Call the upper triangle of the final matrix U
- **Lemma (LU Factorization):** If the above algorithm terminates (does not divide by zero) then A = L*U
- Solving A*x=b using GE
  - Factorize A = L*U using GE (cost = 2/3 n^3 flops)
  - Solve L’y = b for y, using substitution (cost = n^2 flops)
  - Solve U’x = y for x, using substitution (cost = n^2 flops)
- Thus A’x = (L’U’)x = L’(U’x) = L’y = b as desired

Problems with basic GE algorithm

- What if some A(i,i) is zero? Or very small?
  - Result may not exist, or be "unstable", so need to pivot
- Current computation all BLAS 1 or BLAS 2, but we know that BLAS 3 (matrix multiply) is fastest (earlier lectures...)

Pivoting in Gaussian Elimination

- A = \[
\begin{bmatrix}
0 & 1 \\
1 & 0
\end{bmatrix}
\] fails completely because can’t divide by A(1,1)=0
- But solving Ax=b should be easy!
  - When diagonal A(i,i) is tiny (not just zero), algorithm may terminate but get completely wrong answer
  - Numerical instability
  - Roundoff error is cause
  - **Cure:** Pivot (swap rows of A) so A(i,i) large

Gaussian Elimination with Partial Pivoting (GEPP)

- Partial Pivoting: swap rows so that A(i,i) is largest in column

```
for i = 1 to n-1
  find and record k where |A(k,i)| = max_{j \leq i \leq n} |A(j,i)|
  i.e. largest entry in rest of column i
  exit with a warning that A is singular, or nearly so
  if |A(k,i)| = 0
    exit with a warning that A is singular, or nearly so
    else k \neq i
      swap rows i and k of A
  end if
  A(i+1:n,i) = A(i+1:n,i) / A(i,i)  ... each |quotient| \leq 1
  A(i+1:n,i+1:n) = A(i+1:n,i+1:n) - A(i+1:n,i)*A(i,i+1:n)
end for
```

- **Lemma:** This algorithm computes A = P’L’U, where P is a permutation matrix.
- This algorithm is numerically stable in practice
- For details see LAPACK code at [http://www.netlib.org/lapack/single/sgetf2.f](http://www.netlib.org/lapack/single/sgetf2.f)
- Standard approach – but communication costs?
Problems with basic GE algorithm

- What if some A(i,i) is zero? Or very small?
  - Result may not exist, or be "unstable", so need to pivot
- Current computation all BLAS 1 or BLAS 2, but we know that BLAS 3 (matrix multiply) is fastest (earlier lectures...)

\[
\text{for } i = 1 \text{ to } n-1
\]
\[
A(i+1:n, i) = A(i+1:n, i) / A(i, i)
\]
\[
A(i+1:n, i+1:n) = A(i+1:n, i+1:n) - A(i+1:n, i) * A(i, i+1:n)
\]

Converting BLAS2 to BLAS3 in GEPP

- Blocking
  - Used to optimize matrix-multiplication
  - Harder here because of data dependencies in GEPP
- BIG IDEA: Delayed Updates
  - Save updates to "trailing matrix" from several consecutive BLAS2 (rank-1) updates
  - Apply many updates simultaneously in one BLAS3 (matmul) operation

  - Same idea works for much of dense linear algebra
    - Not eigenvalue problems or SVD – need more ideas
- First Approach: Need to choose a block size \( b \)
  - Algorithm will save and apply \( b \) updates
  - \( b \) should be small enough so that active submatrix consisting of \( b \) columns of \( A \) fits in cache
  - \( b \) should be large enough to make BLAS3 (matmul) fast

Efficiency of Blocked GEPP (all parallelism "hidden" inside the BLAS)

\[\begin{align*}
\text{Speed (LAPACK LU) / Speed (best effort)} \\
\text{Speed (Matmul) / HW Peak} \\
\text{Speed (LAPACK LU) / Speed (Matmul)}
\end{align*}\]
Communication Lower Bound for GE

- Matrix Multiplication can be “reduced to” GE
- Not a good way to do matmul but it shows that GE needs at least as much communication as matmul
- Does blocked GEPP minimize communication?

\[
\begin{bmatrix}
1 & 0 & -B \\
A & I & 0 \\
0 & 0 & I
\end{bmatrix}
= 
\begin{bmatrix}
I & 0 & -B \\
A & I & A\cdot B \\
0 & 0 & I
\end{bmatrix}
\]

Does LAPACK’s GEPP Minimize Communication?

- Case 1: \( n \geq M \) - huge matrix – attains lower bound
  - \( b = \sqrt{M} \) optimal, dominated by matmul
- Case 2: \( n \leq \sqrt{M} \) - small matrix – attains lower bound
  - Whole matrix fits in fast memory, any algorithm attains lower bound
- Case 3: \( \sqrt{M} < n < M \) - medium size matrix – not optimal
  - Can’t choose \( b \) to simultaneously optimize matmul and BLAS2 GEPP of \( n \times b \) submatrix
  - Worst case: Exceed lower bound by factor \( M^{1/6} \) when \( n = M^{2/3} \)

Alternative cache-oblivious GE formulation (1/2)

- Toledo (1997)
  - Describe without pivoting for simplicity
  - “Do left half of matrix, then right half”

\[
\text{function } [L,U] = RLU(A) \quad \text{... assume } A \text{ is } m \times n
\]

- if (\( n=1 \)) \( L = A/A(1,1), \ U = A(1,1) \)
- else
  - \( [L1,U1] = RLU(A(1:m, 1:n/2)) \quad \text{... do left half of } A \)
  - let \( L11 \) denote top \( n/2 \) rows of \( L1 \)
  - \( A(1:n/2, n/2+1:n) = L11^{-1} \cdot A(1:n/2, n/2+1:n) \)
  - update top \( n/2 \) rows of right half of \( A \)
  - \( - A(1:n/2, 1:n/2) \cdot A(1:n/2, n/2+1:n) \)
  - update rest of right half of \( A \)
  - \( [L2,U2] = RLU(A(n/2+1:m, n/2+1:n)) \quad \text{... do right half of } A \)
  - return \( [L1,L2] \) and \( [U1, [A(:,); U2]] \)

Alternative cache-oblivious GE formulation (2/2)

\[
\text{for } \text{ib = 1 to n-1 step b} \quad \text{... Process matrix b columns at a time}
\end{bmatrix} \cdot \text{ib + b-1} \quad \text{... Point to end of block of b columns}
\]

apply BLAS2 version of GEPP to get \( A(ib:end, ib:end) = P' \cdot L' \cdot U' \)

- let \( LL \) denote the strict lower triangular part of \( A(ib:end, ib:end) \)
- \( A(ib+1:n, ib+1:n) = A(ib:end, ib+1:n) \)
- \( A(ib+1:n, ib+1:n) = A(ib+1:n, ib+1:n) \)
- \( A(ib+1:n, ib+1:n) = A(ib+1:n, ib+1:n) \)

... apply delayed updates with single matrix-multiply
  - ... with inner dimension \( b \)

Still doesn’t minimize latency, but fixable

CLASS PROJECT
Explicitly Parallelizing Gaussian Elimination

- **Parallelization steps**
  - Decomposition: identify enough parallel work, but not too much
  - Assignment: load balance work among threads
  - Orchestrate: communication and synchronization
  - Mapping: which processors execute which threads (locality)

- **Decomposition**
  - In BLAS 2 algorithm nearly each flop in inner loop can be done in parallel, so with \( n^2 \) processors, need \( 3n \) parallel steps, \( O(n \log n) \) with pivoting
  - This is too fine-grained, prefer calls to local matmuls instead
  - Need to use parallel matrix multiplication

- **Assignment and Mapping**
  - Which processors are responsible for which submatrices?

Different Data Layouts for Parallel GE

- **1D Column Blocked Layout**
  - Bad load balance: \( P_0 \) idle after first \( n/4 \) steps

- **1D Column Cyclic Layout**
  - Load balanced, but can’t easily use BLAS3
  - Can trade load balance and BLAS3 performance by choosing \( b \), but factorization of block column is a bottleneck

- **1D Column Block Cyclic Layout**
  - Complicated addressing, may not want full parallelism
  - In each column, row

- **Block Skewed Layout**
  - The winner!

- **2D Row and Column Blocked Layout**
  - Bad load balance: \( P_0 \) idle after first \( n/2 \) steps

- **2D Row and Column Block Cyclic Layout**
  - The winner!

Matrix multiply of green = blue * pink

Distributed Gaussian Elimination with a 2D Block Cyclic Layout

for \( b = 1 \) to \( n-1 \) step \( b \)
  
  end = min( \( b / b-1, n \) )

for \( i = b \) to end
  
  (1) end pivot row \( k \), column broadcast

  (2) swap rows \( k \) and \( 1 \) in thick column, broadcast row \( k \)

  (3) \( A(>1, i) = A(<1, i) / A(1, i) \)

  (4) \( A(>1, i+1:end) = A(>1, i+1:end) * A(1, i+1:end) \)

  end for

  (5) broadcast all swap information right and left

  (6) apply all rows swaps to other columns
Review of Parallel MatMul

- Want Large Problem Size Per Processor

PDGEMM = PBLAS matrix multiply

Observations:
- For fixed N, as P increases, Mflops increases, but less than 100% efficiency
- For fixed P, as N increases, Mflops (efficiency) rises

DGEMM = BLAS routine for matrix multiply

Maximum speed for PDGEMM = # Procs * speed of DGEMM

Observations:
- Efficiency always at least 48%
- For fixed N, as P increases, efficiency drops
- For fixed P, as N increases, efficiency increases

Does ScalAPACK Minimize Communication?

- Lower Bound: \( O(n^2 / P^{1/2}) \) words sent in \( O(P^{1/2}) \) messes.
  - Attained by Cannon and SUMMA (nearly) for matmul

ScalAPACK:
- \( O(n^2 \log P / P^{1/2}) \) words sent – close enough
- \( O(n \log P) \) messages – too large
- Why so many? One reduction costs \( O(\log P) \) per column to find maximum pivot, times \( n \) = #columns

- Need to abandon partial pivoting to reduce messages
  - Suppose we have \( n \times n \) matrix on \( P^{1/2} \times P^{1/2} \) processor grid
  - Goal: For each panel of \( b \) columns spread over \( P^{1/2} \) procs, identify \( b \) “good” pivot rows in one reduction
    - Call this factorization TSLU = “Tall Skinny LU”
    - Several natural bad (numerically unstable) ways explored, but good way exists
  - SC08, “Communication Avoiding GE”, D., Grigori, Xiang

PDGESV = ScalAPACK Parallel LU

Since it can run no faster than its inner loop (PDGEMM), we measure:
Efficiency = Speed(PDGESV)/Speed(PDGEMM)

Observations:
- Efficiency well above 50% for large enough problems
- For fixed N, as P increases, efficiency decreases (just as for PDGEMM)
- For fixed P, as N increases efficiency increases (just as for PDGEMM)
- From bottom table, cost of solving \( Ax = b \) about half of matrix multiply for large enough matrices.
- From the flop counts we would expect it to be \( (2n^3)/(2/3n^3) = 3 \) times faster, but communication makes it a little slower.
Minimizing Communication in TSLU

Parallel: \[ W = \begin{bmatrix} W_1 & W_2 & W_3 & W_4 \end{bmatrix} \rightarrow LU \rightarrow LU \rightarrow LU \rightarrow LU \]

Sequential: \[ W = \begin{bmatrix} W_1 & W_2 & W_3 & W_4 \end{bmatrix} \rightarrow LU \rightarrow LU \rightarrow LU \rightarrow LU \]

Dual Core: \[ W = \begin{bmatrix} W_1 & W_2 & W_3 & W_4 \end{bmatrix} \rightarrow LU \rightarrow LU \rightarrow LU \rightarrow LU \]

Multicore / Multisocket / Multirack / Multisite / Out-of-core: ? Can Choose reduction tree dynamically

Same idea for QR of Tall-skinny matrix (TSQR)

Parallel: \[ W = \begin{bmatrix} W_1 & W_2 & W_3 & W_4 \end{bmatrix} \rightarrow QR \rightarrow QR \rightarrow QR \rightarrow QR \]

Sequential: \[ W = \begin{bmatrix} W_1 & W_2 & W_3 & W_4 \end{bmatrix} \rightarrow QR \rightarrow QR \rightarrow QR \rightarrow QR \]

Dual Core: \[ W = \begin{bmatrix} W_1 & W_2 & W_3 & W_4 \end{bmatrix} \rightarrow QR \rightarrow QR \rightarrow QR \rightarrow QR \]

First step of SVD of Tall-Skinny matrix

Performance vs ScaLAPACK LU

- TSLU
  - IBM Power 5
    - Up to 4.37x faster (16 procs, 1M x 150)
  - Cray XT4
    - Up to 5.52x faster (8 procs, 1M x 150)
- CALU
  - IBM Power 5
    - Up to 2.29x faster (64 procs, 1000 x 1000)
  - Cray XT4
    - Up to 1.81x faster (64 procs, 1000 x 1000)
- See INRIA Tech Report 6523 (2008), paper at SC08

TSQR Performance Results

- Parallel
  - Intel Clovertown
    - Up to 8x speedup (8 core, dual socket, 10M x 10)
  - Pentium III cluster, Dolphin Interconnect, MPICH
    - Up to 6.7x speedup (16 procs, 100K x 200)
  - BlueGene/L
    - Up to 4x speedup (32 procs, 1M x 50)
  - Tesla C 2050 / Fermi
    - Up to 13x (110,592 x 100)
  - Grid – 4x on 4 cities vs 1 city (Dongarra, Langou et al)
  - Cloud – (Gleich and Benson) ~2 map-reduces
- Sequential
  - “Infinite speedup” for out-of-core on PowerPC laptop
    - As little as 2x slowdown vs (predicted) infinite DRAM
  - LAPACK with virtual memory never finished
- SVD costs about the same
- Joint work with Grigori, Hoemmen, Langou, Anderson, Ballard, Keutzer, others
optimal algorithms for numerical linear algebra”, Ballard et al, 2014

References are from Table 3.2 in “Communication lower bounds and attaining communication lower bounds”

Assume nxn matrices on p processors, minimum memory per proc: M = O(n^2/p)
- #words moved = Ω(n^2/p)^1/2, #messages = Ω(n^2/p)^1/2
- Ours, ScalAPACK, Randomized

<table>
<thead>
<tr>
<th>Computation</th>
<th>2-Level Mem</th>
<th>Multiple Level</th>
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</thead>
<tbody>
<tr>
<td>BLAS3</td>
<td></td>
<td></td>
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<tr>
<td>Cholesky</td>
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<td>LU</td>
<td></td>
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<td>Sym Indef</td>
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<tr>
<td>Matmul</td>
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<tr>
<td>Cholesky QR</td>
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<tr>
<td>Eig(A=A^T) and SVD</td>
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<td>[10]</td>
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</tbody>
</table>

Can we do even better?
- Assume nxn matrices on p processors
- Use c copies of data: M = O(cn^2 / p) per processor
- Increasing M reduces lower bounds:
  - #words Moved = Ω(n^2/P / M^1/2) = Ω(n^2 / (c^{1/2} P^{1/2}))
  - #messages = Ω(n^2 / M^1/2) = Ω(n^2 / (c^{1/2} P^{1/2}))
- Attainable for Matmul
- Not attainable for LU, Cholesky
- Tm: #words moved * #messages / M must increase #messages by same factor
- Cor: Perfect strong scaling impossible for LU, Cholesky, QR
- Both lower bounds attainable for Cholesky, LU, QR (via Cholesky QR):
  - #words Moved = Ω(n^2 / (c^{1/2} P^{1/2}))
  - #messages = Ω(c^{1/2} P^{1/2})
LU Speedups from Tournament Pivoting and 2.5D

2.5D vs 2D LU
With and Without Pivoting

Dense Linear Algebra on Recent Architectures
- Multicore
  - How do we schedule all parallel tasks to minimize idle time?

- GPUs
  - Heterogeneous computer: consists of functional units (CPU and GPU) that are good at different tasks
  - How do we divide the work between the GPU and CPU to take maximal advantage of both?
  - Challenging now, will get more so as platforms become more heterogeneous

Multicore: Expressing Parallelism with a DAG
- DAG = Directed Acyclic Graph
  - S1 → S2 means statement S2 "depends on" statement S1
  - Can execute in parallel any Si without input dependencies

- For simplicity, consider Cholesky A = LLᵀ, not LU
  - N by N matrix, numbered from A(0,0) to A(N-1,N-1)
  - "Left looking" code: at step k, completely compute column k of L

for k = 0 to N-1
  for n = 0 to k-1
    A(k,k) = A(k,k) – A(k,n)*A(k,n)
    A(k,k) = sqrt(A(k,k))
  for m = k+1 to N-1
    for n = 0 to k-1
      A(m,k) = A(m,k) – A(m,n)*A(k,n)
      A(m,k) = A(m,k) / A(k,k)
Expressing Parallelism with a DAG - Cholesky

for k = 0 to N-1
  for n = 0 to k-1
    \( S_1(k,n) \) = \( A(k,k) - A(k,n)A(k,n)^T \)
    \( S_2(k) \) = \( \sqrt{A(k,k)} \)
  for m = k+1 to N-1
    for n = 0 to k-1
      \( S_3(k,m,n) \) = \( A(m,k) - A(m,n)A(k,n)^T \)
      \( S_4(k,m) \) = \( A(m,k)A(k,k)^{-1} \)

DAG has \( \approx N^3/6 \) vertices:

- Each \( A[i,j] \) is a b-by-b block

Expressing Parallelism with a DAG – Block Cholesky

for k = 0 to N/b-1
  for n = 0 to k-1
    \( S_1(k,n) \) = \( A[k,k] - A[k,n]A[k,n]^T \)
    \( S_2(k) \) = \( \text{unblocked}_\text{Cholesky}(A[k,k]) \)
  for m = k+1 to N/b-1
    for n = 0 to k-1
      \( S_3(k,m,n) \) = \( A[m,k] - A[m,n]A[k,n]^T \)
      \( S_4(k,m) \) = \( A[m,k]A[k,k]^{-1} \)

Same DAG, but only \( \approx (N/b)^3/6 \) vertices

Sample Cholesky DAG with

#blocks in any row or column = N/b = 5

- Note implied order of summation from left to right
- Not necessary for correctness, but it does reflect what the sequential code does
- Can process DAG in any order respecting dependences

Scheduling options

- Static (pre-assign tasks to processors) vs Dynamic (idle processors grab ready jobs from work-queue)
  - If dynamic, does scheduler take user hints/priorities?
- Respect locality (eg processor must have some task data in its cache) vs not
- Build and store entire DAG to schedule it (which may be very large, \( (N/b)^3 \)), vs Build just the next few “levels” at a time (smaller, but less information for scheduler)
- Programmer builds DAG & schedule vs Depend on compiler or run-time system
  - Ease of programming, vs not exploiting user knowledge
  - If compiler, how conservative is detection of parallelism?
  - Generally useful, not just linear algebra
Schedulers tested

- Cilk
  - programmer-defined parallelism
  - spawn – creates independent tasks
  - sync – synchronizes a sub-branch of the tree

- SMPSs
  - dependency-defined parallelism
  - pragma-based annotation of tasks (directionality of the parameters)

- PLASMA (Static Pipeline)
  - programmer-defined (hard-coded)
  - apriori processing order
  - stalling on dependencies

Measured Results for Tiled Cholesky

- PLASMA (static pipeline) – best
- SMPSs – somewhat worse
- Cilk 2D – inferior
- Cilk 1D – still worse

More Measured Results for Tiled Cholesky

- Measured on Intel Tigerton 2.4 GHz
- Cilk 1D: one task is whole panel, but with “look ahead”
- Cilk 2D: tasks are blocks, scheduler steals work, little locality
- PLASMA works best

Still More Measured Results for Tiled Cholesky

- quad-socket, quad-core (16 cores total) Intel Tigerton 2.4 GHz
Dense Linear Algebra on GPUs

- Source: Vasily Volkov’s SC08 paper
  - Best Student Paper Award (729 citations)
- New challenges
  - More complicated memory hierarchy
  - Not like "L1 inside L2 inside …
  - Need to choose which memory to use carefully
  - Need to move data manually
  - GPU does some operations much faster than CPU, but not all
  - CPU and GPU fastest using different data layouts

Motivation

- NVIDIA released CUBLAS 1.0 in 2007, which is BLAS for GPUs
- This enables a straightforward port of LAPACK to GPU
- Consider single precision only

Scheduling on Multicore – Next Steps

- PLASMA 2.8.0 released 12/2015
  - Includes BLAS, Cholesky, QR, LU, LDL, eig, svd
  - icl.cs.utk.edu/plasma/
- Future of PLASMA
  - Continue adding functions
  - Add dynamic scheduling
    - QUARK dynamic scheduler released 12/2011
    - DAGs for eigenproblems are too complicated to do by hand
    - Plan to adopt OpenMP4.0 DAG scheduling features
  - Still assumes homogeneity of available cores
    - What about GPUs, or mixtures of CPUs and GPUs?
- MAGMA
  - icl.cs.utk.edu/magma

CLASS PROJECTS

CS267 Lecture 13
GPU Memory Hierarchy

- Register file is the fastest and the largest on-chip memory
  - Constrained to vector operations only
- Shared memory permits indexed and shared access
  - However, 2-4x smaller and 4x lower bandwidth than registers
  - Only 1 operand in shared memory is allowed versus 4 register operands
  - Some instructions run slower if using shared memory

__global__ void sgemmNN (const float *A, int lda, const float *B, int ldb, float* C, int ldc, int k, float alpha, float beta) {
  A += blockIdx.x * 64 + threadIdx.x + threadIdx.y * 16;
  B += threadIdx.x + (blockIdx.y * 16 + threadIdx.y) * ldb;
  C += blockIdx.x * 64 + threadIdx.x + (threadIdx.y + blockIdx.y * ldc) * 16;
  __shared__ float bs[16][17];
  float c[16] = {0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0};
  const float *Blast = B + k;
  do {
    #pragma unroll for(int i = 0; i < 16; i++)
    bs[threadIdx.x][threadIdx.y + i] = B[i * ldb];
    B += 16;
    __syncthreads();
  } while( B < Blast );
  for(int i = 0; i < 16; i++)
    C[i] = alpha * c[i] + beta * C[i];
}

(CS267 Lecture 13)

(Some new) NVIDIA coding recommendations

- Minimize communication with CPU memory
- Keep as much data in registers as possible
  - Largest, fastest on-GPU memory
  - Vector-only operations
- Use as little shared memory as possible
  - Smaller, slower than registers; use for communication, sharing only
  - Speed limit: 66% of peak with one shared mem argument
- Use vector length VL=64, not max VL = 512
  - Strip mine longer vectors into shorter ones
- Final matmul code similar to Cray X1 or IBM 3090 vector codes

New code vs. CUBLAS 1.1

Performance in multiplying two NxN matrices on GeForce 8800 GTX:

- Our implementation (60%) vs. CUBLAS 1.1 (37%)
- % of peak: multiply-and-add with an operand in shared memory

Compute pointers to the data

Declare the on-chip storage

Read A's columns

Store C's block to memory

The bottleneck:
Read A's columns
Do Rank-1 updates

03/01/2016 CS267 Lecture 13 55
The Progress So Far

- Achieved predictable performance in SGEMM
  - Which does $O(N^3)$ work in LU factorization
- But LU factorization (naïve SGETRF) still underperforms
  - Must be due to the rest $O(N^3)$ work done in BLAS1 and BLAS2
  - Why $O(N^3)$ work takes so much time?

Row-Pivoting in LU Factorization

Exchange two rows of an $N \times N$ matrix ($SSWAP$ in CUBLAS 2.0):

Row pivoting in column-major layout on GPU is very slow
This alone consumes half of the runtime in naïve SGETRF

Panel Factorization

Factorizing $N\times64$ matrix in GPU memory using LAPACK’ s SGETF2:

- Invoking small BLAS operations on GPU from CPU is slow
- Can we call a sequence of BLAS operations from GPU?
  - Requires barrier synchronization after each parallel BLAS operation
  - Barrier is possible but requires sequential consistency for correctness

BLAS1 Performance

Scale a column of an $N \times N$ matrix that fits in the GPU memory
(assumes aligned, unit-stride access)

- Peak bandwidth of these GPUs differs by a factor of 4.4
- But runtimes are similar
- Small tasks on GPU are overhead bound
Design of fast matrix factorizations on GPU

- Use GPU for matmul only, not BLAS2 or BLAS1
- Factor panels on CPU
- Use “look-ahead” to overlap CPU and GPU work
  - GPU updates matrix while CPU factoring next panel
- Use row-major layout on GPU, column-major on CPU
  - Convert on the fly
- Substitute triangular solves $LX=B$ with multiply by $L^{-1}$
  - For stability CPU needs to check $|| L^{-1} ||$
- Use variable-sized panels for load balance
- For two GPUs with one CPU, use column-cyclic layout on GPUs

Raw Performance of Factorizations on GPU

- Where does the time go?
  - Time breakdown for LU on 8800 GTX
Importance of various optimizations on GPU

- Slowdown when omitting one of the optimizations on GTX 280

Class Projects

- Pick one (of many) functions/algorithms
- Pick a target parallel platform
- Pick a “parallel programming framework”
  - LAPACK – all parallelism in BLAS
  - ScaLAPACK – distributed memory using MPI
  - PLASMA – DAG scheduling on multicore
    - Parallel Linear Algebra for Scalable Multi-core Architectures
    - http://icl.cs.utk.edu/plasma/
  - MAGMA – DAG scheduling for heterogeneous platforms
    - Matrix Algebra on GPU and Multicore Architectures
    - http://icl.cs.utk.edu/magma/
    - Spark, Elemental, ...
- Design, implement, measure, model and/or compare performance
  - Can be missing entirely on target platform
  - May exist, but with a different programming framework

Results for matmul, LU on NVIDIA

- What we’ve achieved:
  - Identified realistic peak speed of GPU architecture
  - Achieved a large fraction of this peak in matrix multiply
  - Achieved a large fraction of the matrix multiply rate in dense factorizations