include both multi-level signaling and phase modulation using a weighted sum of quadrature square waves. On the efficiency front we are looking at techniques that reduce the area and power dissipation of our prototype signaling systems. In particular we are investigating alternative timing circuits based on regulated inverter delay lines and regenerative circuits that avoid the static power dissipation of the source-coupled delay lines we currently employ.

9. Acknowledgement

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10. References

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Figure 14b. A quantitative comparison of the simulation run and sampler data must await a full characterization of the sampler's behavior. For example, it is not yet clear whether the substantial differences in clock rise time and output pair amplitude is an artifact of the sampler's slew rate or an indication that we have not properly modeled circuit parasitics in the simulation. The samplers have been used so far only to determine whether internal circuits are behaving qualitatively correctly; in this role, they were very useful in verifying correct operation of the DLLs, for example.

A set of samplers is currently being fabricated on a second test chip with provisions for more careful characterization. We hope that in future chips, fairly precise measurements may be possible.

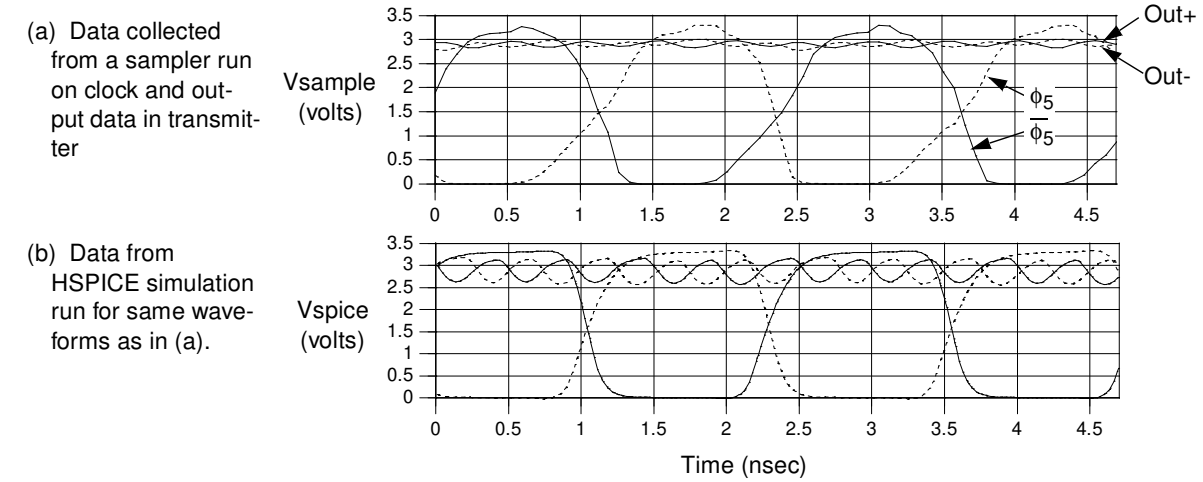


Figure 14: Sampled and simulated waveforms from the transmitter (one of the clock pairs and the output pair).

7.5 Tracking Receiver Operation

Because of the previously described problems with package-parasitic-induced noise, we were unable to test the receiver at 4Gb/s. We were, however, able to fully test its ability to acquire the framing sequence and to operate the LFSR checker at 2.5Gb/s. Because of various problems with the data transmitter, described above, bit-error rates were unacceptably high (about 10^{-4}). Simulation suggests that the BER can be brought to acceptable levels with a redesigned transmitter.

8. Conclusions and Future Work

We have described an initial experiment to verify the usefulness of transmitter equalization to remove the amplitude and timing noise introduced by frequency-dependent attenuation on a transmission line. Though only partly successful, the test chip and system verified that our simple equalization technique, a FIR filter implemented as a transition filter, is effective for this purpose. It appears, in fact, that only a simple 2-step transition filter is necessary to reap most of the benefits of the approach. This type of filter can be implemented with very simple circuitry. We are able to report only correct operation of the tracking clock recovery receiver; operation at full speed and meaningful measurements of bit error rates will have to wait for the next iteration of the design.

We are commencing the design of a new test chip with a number of improvements. The transmitter will be a true current-steering design with an adjustable on-chip terminator. We plan to include only a 2-step transition filter equalizer in this design, and therefore expect it to be much more compact and lower power. An improved DLL, clock buffer, and layout will solve the systematic timing problems encountered in the first chip. We also plan to build two receiver systems, one with tracking clock recovery and one with oversampling clock recovery. Implemented on the same die, in the same noise environment, and using many of the same circuit components, these should provide a useful experimental comparison of the two clock recovery techniques.

Our longer term plan is to improve both the speed and efficiency of high-performance signaling. In addition to increasing our transmission rate we are currently investigating methods of sending more than one bit per baud. These

adjustment of weights for non-adjacent bits. We speculate that a 2-tap transition filter may be sufficient to obtain most of the benefits of this equalization technique, allowing much simpler transmitter circuitry than we used in the test chip.

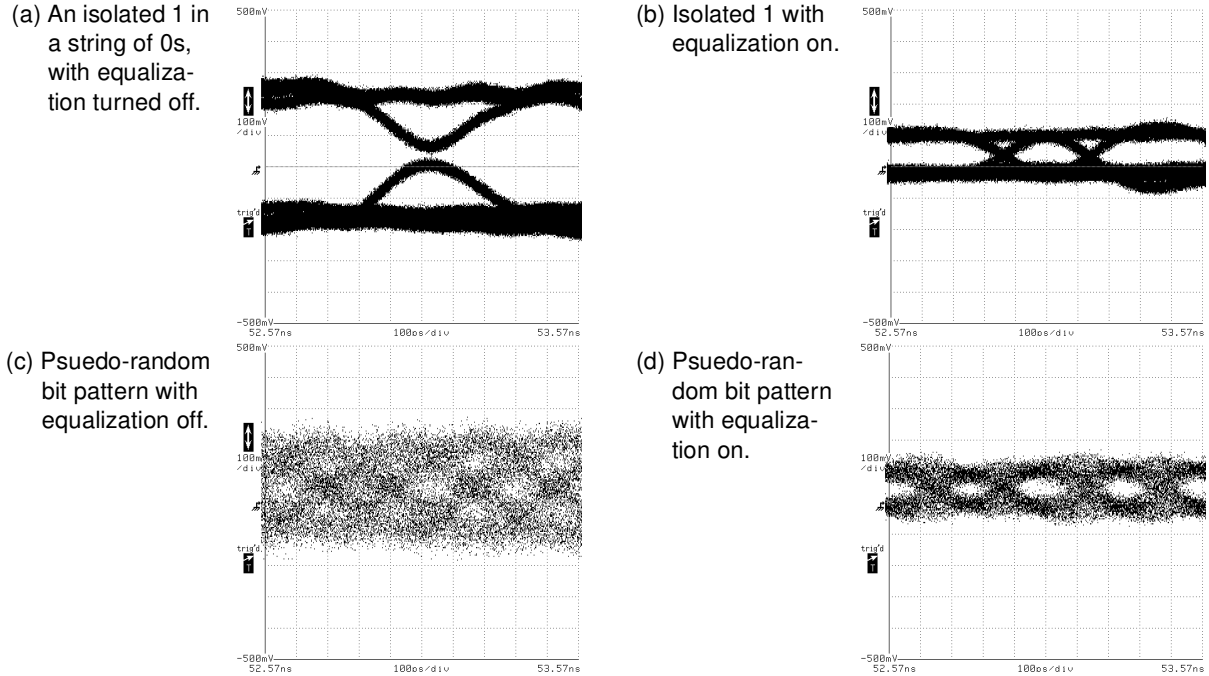


Figure 13: Transmitter timing jitter measured for a 1m twisted-pair transmission line with and without equalization.

7.3 Transmitter Problems

In the isolated-bit waveforms of the previous figures, various effects that arise from transmitter imperfections and package parasitics can be seen. The "ripple" in an otherwise quiet series of 0s, for example, is due to a slight misadjustment of On and Off clock overlap. Some overshoot is evident following an isolated bit (this overshoot contributes much of the amplitude noise in the pseudo-random bit patterns); this is caused by the LC tank circuits formed by the transmitter's output capacitance and bond-wire inductance, as confirmed by SPICE simulations. This effect is probably unavoidable in conventional packaging, but can be overcome almost entirely by terminating the transmitter as well as the receiver. Our future signaling chips will have both ends of the transmission line terminated. A second phenomenon that contributes significant noise is reflection off the capacitance at the receiver. These reflections are reflected again at the (high-impedance) transmitter, causing intersymbol interference at the receiver. Simulations suggest that on-chip transmitter termination will very effectively remove these reflections.

Two design "features" of the transmitter also contributed to signaling problems. First, the transmitter has a clocked (On-clock) current tail transistor (this circuit structure was the only one we could find at the time that would deliver the necessary switching speed). When the Off-clock turns on, well in advance of the time when the DAC cell is supposed to transmit its data bit, charge is injected into the output from the common source node. In our signalling system, this effects introduces an unintentional signal onto the line at about 15% of the amplitude of the actual signal. Second, and more seriously, the gating function within the filter changes the strength by completely turning off one or two of the three drivers in a DAC. The result is that, when equalization is turned on, the output signal is not truly differential. This has the unfortunate effect of sending a common-mode signal down the line, where various non-linearities transform the common-mode signal into a differential (noise) signal. A new transmitter design will take care of both of these problems.

7.4 On-Chip Samplers

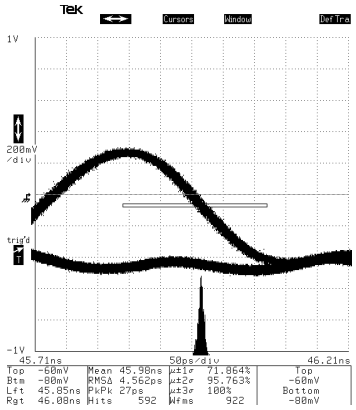
Figure 14a shows a graphical display of data from a sampler run in which two of the transmitter clocks and the output differential pair are measured. For comparison, an HSPICE simulation of the same waveforms are shown in

7. Experimental Results

7.1 Transmitter Timing Jitter

Measurements of the transmitter's timing jitter are shown in Figure 12. These (and all of the other measurements in this section) were performed using a Tektronix 11801A digital sampling oscilloscope. For transmitter jitter measurements, the transmitter was connected through a short PC-board transmission line to a discrete resistor termination.

(a) A sequence with a single 1 embedded in a stream of 0s. Peak-to-peak jitter at the trailing edge is 27 psec; RMS jitter is 4.5 psec.



(b) A psuedo-random bit sequence generated by the transmitter's LFSR. Peak-to-peak jitter is 91 psec; RMS jistter is 16.5 psec.

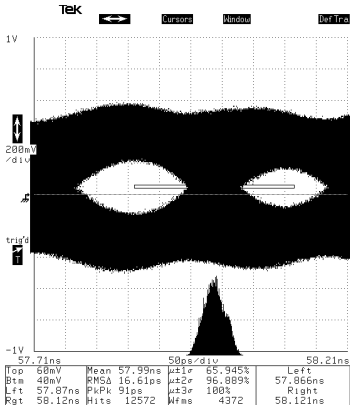


Figure 12: Transmitter timing jitter measured with a transmitter driving a short transmission line terminated with discrete resistors.

Figure 12a shows jitter at the trailing edge of an isolated 1 in a string of 0s. This measurement is indicative of the stability of any one output of the transmitter's clock generator. Single-edge jitter is only about 4.5psec RMS, which is quite low compared to other reported jitter measurements for replica-biased DLLs. However, these measurements are on a chip that has no other active circuitry generating substrate and power supply noise. In an actual application we would expect the single-edge timing jitter to be considerably larger.

Figure 12b shows a histogram of jitter at one particular data cell boundary for a pseudo-random sequence of bits generated by the transmitter's LFSR. Jitter is about three times larger than for the single-edge case. Note that the data eye for the right-hand bit is smaller than the previous data cell. The timing generator in our transmitter exhibits a systematic timing error from cell to cell of about ±10-15psec. We believe this is a result of two effects. First, the buffer that converts the small-swing signals within the DLL to full-swing clocks does not quite preserve the symmetry of the DLL internal signals, and since we are using both clock polarities from each tap of a 180º DLL to operate the transmitter, these asymmetries introduce offsets. Second, the layout of the timing generator and transmitter places slightly different loads on various clock outputs. The first problem can be mostly eliminated with an improved buffer design that we are using in current projects, but which was not available when this transmitter was designed. The second problem can be avoided by much more careful layout that integrates timing circuitry and output drivers into an array of absolutely identical units.

7.2 Transmitter Equalization

Figure 13 shows the results of an experiment on the effectiveness of transmitter equalization. In this experiment, the transmitter drives a short PC-board transmission line, 1m of #30 twisted-pair line, another short PC-board line, and the terminator. Each of the traces in the figure is the voltage across the differential pair at the terminator. Figure 13a shows an isolated 1 in a string of 0s with equalization turned off. Attenuation is about 0.7 with a corresponding reduction in eye height, and the width of the eye is reduced from the nominal 250psec to about 150psec. Figure 13b shows the same bit pattern with equalization turned on, and weights in the filter RAM set to 4 (out of 7) for unequal successive bits; eye width is now much closer to the nominal bit-cell width. Figures 13c and 13d show a pseudo-random bit pattern with equalization turned off (c) and on (d). Equalization recovers a recognizable eye, but attenuation in this 1m line is high enough that this probably represents the limit of the technique at its present state of development. For these experiments we set all of the weights (except the first) in the filters to the same value; with only observation of eye patterns, there was no improvement in the pseudo-random sequence eye patterns with further

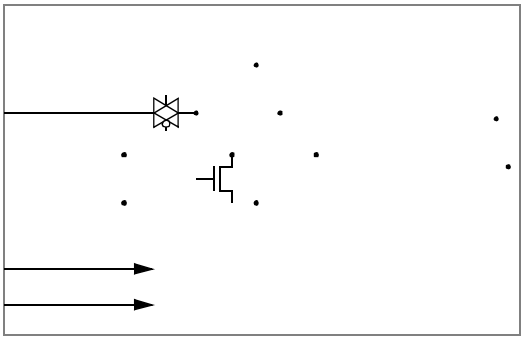


Figure 10: Schematic of on-chip voltage sampler.

A printed circuit board, shown in Figure 11, was built to evaluate the operation of the experimental signaling chips. Up to three chips can be installed on the board. One chip has its transmitter and receiver connected by a minimum-length transmission line; the others can be interconnected by 1, 2, or 3 meter PCB traces or by external coaxial or twisted-pair cables. All transmitter outputs and receiver inputs have a resistive probe brought out to SMA connectors for connection to an oscilloscope. A 400 MHz clock from an external signal generator is gated, buffered and distributed to all chips with discrete ECLinPS logic. ECL counters and delay lines allow positioning the trigger signal for the on-chip digital and analog samplers. Oscilloscope trigger outputs at the 400MHz clock rate and at fclk/8 are provided; the former is useful for generating eye diagrams; the latter corresponds to the period of the transmitter's pattern RAM. A 12-bit DAC generates a reference voltage for the analog voltage samplers. Error indications from the receiver on each chip are accumulated in 10 bit counters. The chips' serial scan chains and control signals for the test board logic are connected to a host computer through an optically-isolated standard PC parallel port.

Figure 11: Photo of test board; three of the experimental 4Gb/s signaling chips are mounted on the left side of the board.

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