

# **CLASS-E HIGH-EFFICIENCY RF/MICROWAVE POWER AMPLIFIERS: PRINCIPLES OF OPERATION, DESIGN PROCEDURES, AND EXPERIMENTAL VERIFICATION**

Nathan O. Sokal, IEEE Life Fellow  
Design Automation, Inc.  
4 Tyler Road  
Lexington, MA 02420-2404  
U. S. A.

## **ABSTRACT**

**Class-E power amplifiers [1]-[6] achieve significantly higher efficiency than for conventional Class-B or -C. Class E operates the transistor as an on/off switch and *shapes the voltage and current waveforms* to prevent *simultaneous* high voltage and high current in the transistor; that minimizes the power dissipation, especially during the switching transitions. In the published low-order Class-E circuit, a transistor performs well at frequencies up to about 70% of its frequency of good Class-B operation (an unpublished higher-order Class-E circuit operates well up to about double that frequency). This paper covers circuit operation, improved-accuracy explicit design equations for the published low-order Class E circuit, optimization principles, experimental results, tuning procedures, and gate/base driver circuits. Previously published analytically derived design equations did not include the dependence of output power ( $P$ ) on load-network loaded  $Q$  ( $Q_L$ ); as a result, the output power was 38% to 10% less than expected, for  $Q_L$  values in the usual range of 1.8 to 5. This paper includes an accurate new equation for  $P$  that includes the effect of  $Q_L$ .**

## 1. "WHAT CAN CLASS E DO FOR ME?"

Typically, Class-E amplifiers [1]-[6] can operate with power losses smaller by a factor of about 2.3, as compared with conventional Class-B or -C amplifiers using the same transistor at the same frequency and output power. For example, a Class-B or -C power stage operating at 65% collector or drain efficiency (losses = 35% of input power) would have an efficiency of about 85% (losses = 15% of input power) if changed to Class E ( $35\%/15\% = 2.3$ ). Class-E amplifiers can be designed for narrow-band operation or for fixed-tuned operation over frequency bands as wide as 1.8:1, such as 225-400 MHz. (If harmonic outputs must be well below the carrier power, *any amplifier* other than Class A or push-pull Class AB cannot operate over a band wider than about 1.8:1 with only one fixed-tuned harmonic-suppression filter.) Harmonic output of Class-E amplifiers is similar to that of Class-B amplifiers. Another benefit of using Class E is that the amplifier is *a priori* designable; explicit design equations are given here. The effects of components and frequency variations are defined *a priori* [4, Figs. 5 and 6] and [7], and are small. When the amplifier is built as designed, it works as expected, without need for "tweaking" or "fiddling."

## 2. PHYSICAL PRINCIPLES FOR ACHIEVING HIGH EFFICIENCY

Efficiency is maximized by minimizing power dissipation, while providing a desired output power. In most RF and microwave power amplifiers, the largest power dissipation is in the power transistor: the *product* of transistor voltage and transistor current *at each point in time* during the RF period, integrated and averaged over the RF period. Although the transistor must sustain high voltage during *part* of the RF period, and must also conduct high current during *part* of the RF period, the circuit can be arranged so that *high voltage and high current do not exist at the same time*. Then the product of transistor voltage and current will be low *at all times* during the RF period. Fig. 1 shows conceptual "target" waveforms of transistor voltage and current that meet the high-efficiency requirements. The

transistor is operated as a switch. The voltage-current product is low throughout the RF period because:

1. "*On*" state: The voltage is nearly zero when high current is flowing, *i.e.*, the transistor acts as a low-resistance "on" switch during the "on" part of the RF period.
2. "*Off*" state: The current is zero when there is high voltage, *i.e.*, the transistor acts as an "off" switch during the "off" part of the RF period.

*Switching transitions:* Although the designer makes the on/off switching transitions as fast as feasible, a high-efficiency technique must accommodate the transistor's practical limitation for RF and microwave applications: the transistor switching times will, unavoidably, be appreciable fractions of the RF period. We avoid a high voltage-current product during the switching transitions, *even though the switching times can be appreciable fractions of the RF period*, by the following two strategies:

3. The rise of transistor voltage is *delayed until after the current has reduced to zero*.
4. The transistor voltage returns to zero *before the current begins to rise*.

The timing requirements of 3 and 4 are fulfilled by a suitable load network (the network between the transistor and the load that receives the RF power), to be examined shortly. Two additional waveform features reduce power dissipation:

5. The transistor voltage at turn-on time is nominally zero (or is the saturation offset voltage  $V_o$  for a bipolar junction transistor, hereafter "BJT"). Then the turning-on transistor does not discharge a charged shunt capacitance ( $C_1$  of Fig. 2), thus avoiding dissipating the capacitor's stored energy of  $(C_1 V^2/2)$ ,  $f$  times per second, where  $V$  is the capacitor's initial voltage at transistor turn-on and  $f$  is the operating frequency. ( $C_1$  comprises the transistor output capacitance and any external capacitance in parallel with it.)
6. The slope of the transistor voltage waveform is nominally zero at turn-on time. Then the current injected into the turning-on transistor by the load network rises smoothly from zero at a controlled moderate rate, resulting in low

$i^2R$  power dissipation while the transistor conductance is building-up from zero during the turn-on transition, even if the turn-on transition time is as long as 30% of the RF period.

*Result:* The waveforms *never* have high voltage and high current *simultaneously*. The voltage and current switching transitions are *time-displaced from each other*, to accommodate transistor switching transition times that can be *substantial fractions of the RF period*, e.g., turn-on transition up to about 30% of the period and turn-off transition up to about 20% of the period.

The low-order Class-E amplifier of Fig. 2 generates voltage and current waveforms that approximate the conceptual "target" waveforms in Fig. 1; Fig. 3 shows the actual waveforms in that circuit. Note that those actual waveforms meet all six criteria listed above and illustrated in Fig. 1. Unpublished higher-order versions of the circuit approximate more closely the target waveforms of Fig. 1, making the circuit even more tolerant of component parasitic resistances and nonzero switching transition times.

*Differences from conventional Class B and C:* The load network is not intended to provide a conjugate match to the transistor output impedance. The load-network design equations come from the solution of a set of simultaneous equations for the steady-state periodic time-domain response, of a network containing non-ideal inductors and capacitors, to periodic operation of a non-ideal switch at the load-network input port, at frequency  $f$ , to provide (a) an input-port voltage of zero value and zero slope at transistor turn-on time, (b) a first-order approximation to a time delay of the voltage rise at transistor turn-off, and (c) a nearly sinusoidal voltage across the load resistance  $R$ , delivering a specified RF power  $P$  from a specified dc supply voltage  $V_{CC}$ .

The transistor's operating locus on the  $(I_d, V_{ds})$  plane is not a tilted straight line (resistance) or a tilted ellipse (resistance + reactance). The operation during the "on" state of the switch is a nearly vertical line whose lower end is at the origin  $(0, 0)$ ; the "off" state of the

switch is a horizontal line whose left end is at the origin. By design, the operating locus avoids the remainder of the  $(I_d, V_{ds})$  plane, the region of *simultaneous* high voltage and high current, *i.e.*, of high power dissipation and consequent reduced efficiency; that region is where conventional Class B and C circuits operate.

### 3. ANALYTICAL AND NUMERICAL DERIVATIONS OF DESIGN EQUATIONS

Analytical derivations of design equations for the circuit of Fig. 2 can be made only by assuming that the current in  $L_2$ - $C_2$  is sinusoidal. That assumption is strictly true only if the load network has infinite loaded  $Q$  ( $Q_L$ , defined as  $2\pi f L_2/R$ )<sup>1</sup>, and yields progressively less-accurate results for  $Q_L$  values progressively lower than infinity. ( $Q_L$  is a free-choice design variable<sup>2</sup>, subject to the condition  $Q_L \geq 1.7879$  (obtained from exact numerical analysis [4], [6]) to be able to obtain the nominal<sup>3</sup> switch-voltage waveform, for the usual choice of the switch “on” duty ratio<sup>4</sup>  $D$  being 50%.) The amplifier's output power  $P$  depends primarily (derivable analytically) on the collector/drain dc-supply voltage  $V_{CC}$  and the load resistance  $R$ , but secondarily (not derivable analytically) on the value chosen for  $Q_L$ . Previously published analytically derived design equations did not include the dependence of  $P$  on  $Q_L$ . As a result, the output power is 38% to 10% less than had been expected, for  $Q_L$  values in the usual range of 1.8 to 5. This paper includes an accurate new equation for  $P$  that includes the effect of  $Q_L$ . Similar restrictions apply to the analytical derivations of design equations for  $C_1$ ,  $C_2$ , and  $R$ . However, the needed component values can be found by numerical methods. Table I gives normalized exact numerical solutions for output power (hence the needed value of  $R$ ),  $C_1$ , and  $C_2$ , for eight values of  $Q_L$  over the entire possible range of 1.7879 to infinity, for the usual choice of  $D = 50\%$ .

**TABLE I. DEPENDENCE OF OUTPUT POWER,  
 $C_1$ , AND  $C_2$  ON LOADED  $Q$  ( $Q_L$ )**

$Q_L$	$PR/(V_{CC} - V_o)^2$	$C_1 2\pi fR$	$C_2 2\pi fR$
infinite	0.576801	0.18360	0
20	0.56402	0.19111	0.05313
10	0.54974	0.19790	0.11375
5	0.51659	0.20907	0.26924
3	0.46453	0.21834	0.63467
2.5	0.43550	0.22036	1.01219
2	0.38888	0.21994	3.05212
1.7879	0.35969	0.21770	infinite

The design equations in the next section are continuous mathematical functions fitted to those eight sets of data. (Having the numerical values of Table I, readers can derive other mathematical functions to fit the data, if they wish, to substitute for the equations given below.)

Kazimierczuk and Puczko [5] published a tabulation similar to Table I here (using a different mathematical technique, but the two sets of tables agree well; see Section 5, below), but they did not include continuous-function design equations based on their tabular data. As a result, a designer using [5] can produce an accurate design at any chosen *tabulated* value of  $Q_L$ , but the designer lacks accurate design information for use at values of  $Q_L$  *in-between* the tabulated values. Avratoglou and Voulgaris [8] gave an analysis, and numerical solutions as graphs, but no tables of computed values and no design equations fitted to the numerical results. Precise design values cannot be read from the graphs.

To be able to make accurate circuit designs and *a priori* design evaluations *at any arbitrary value* of  $Q_L$ , the designer needs design equations comprising continuous mathematical functions, rather than a set of tabulated values as in Table I or [5]. The equations should

give accurate results, and should be simple enough to be easy for the designer to manipulate. Such equations are given below for lossless components, in (4) through (10). The losses and the resulting collector or drain efficiency are accounted for in summary form in (1) and (2) below. The losses are given individually in [2], [4], [9], [10], and unpublished notes; the author intends to publish equations for all individual components of power loss and the resulting collector/drain efficiency. Briefly: Calculate  $R$  from (6) or (6a), using for  $P$  the desired output power divided by the expected collector/drain efficiency (see (2) below for collector/drain efficiency). Then the needed load resistance  $R_{load}$  is

$$R_{load} = R - [ESR_{L2} + ESR_{C2} + 1.365 R_{on} + 0.2116 ESR_{C1}] \quad (1)$$

where  $R_{on}$  is the "on" resistance of the transistor.  $R_{on}$  is a generic term that represents  $R_{DS(on)}$  of a MOSFET or a MESFET, or  $R_{CE(sat)}$  of a BJT. The expected collector/drain efficiency is approximately

$$\eta_C = R_{load} / [R_{load} + ESR_{L2} + ESR_{C2} + 1.365 R_{on} + 0.2116 ESR_{C1}] - (2\pi A)^2 / 12 - 0.01 \quad (2)$$

where  $A = (1 + 0.82/Q_L)(t_f/T)$ ,  $t_f$  is the 100%-to-0% fall time of the assumed linear fall of the collector/drain current at transistor turn-off,  $T = 1/f$  is the period of the operating frequency  $f$ , and "0.01" allocates about 1% loss of efficiency for the power losses in the dc and RF resistances of the dc-feed choke  $L_I$  (substitute a different numerical value, if you wish).

#### 4. EXPLICIT DESIGN EQUATIONS

The explicit design equations given below yield the low-order lumped-element Class-E circuit that operates with the nominal waveforms of Fig. 3. (Distributed-element circuits are discussed briefly at the end of Section 9.) In the equations below,  $V_{CC}$  is the dc supply voltage,  $P$  is the power delivered to the total effective circuit resistance lumped into a single resistor  $R$  (see (1) above),  $f$  is the

operating frequency,  $C_1$ ,  $C_2$ ,  $L_1$  (dc-feed choke), and  $L_2$  are the load network shown in Fig. 2, and  $Q_L$  is the network loaded Q, chosen by the designer as a trade-off among competing evaluation criteria.<sup>2</sup> In a nominal-waveforms circuit operating with the usual choice of  $D = 50\%$ , the minimum possible value of  $Q_L$  is 1.7879 (the circuit can work well with lower values of  $Q_L$ , but the transistor-voltage waveform will be off-nominal: larger than zero at the transistor turn-on time); the maximum possible value of  $Q_L$  is less than the network's unloaded Q. The design procedure is as follows:

$$V_{CC} \leq [BV_{CEV} / 3.56] [\text{chosen safety factor} < 1] \quad (3)$$

The chosen safety factor (*e.g.*, 0.75) allows for not exceeding the transistor's breakdown voltage ( $BV_{CEV}$ ) by a higher-than-nominal peak voltage (in this example, up to  $1/0.75 = 133\%$  of nominal) that could result from off-nominal load impedance and component tolerances. Choose  $V_{CC}$  as determined by the transistor's  $BV_{CEV}$  or the available power-supply voltage. The relationship among  $P$ ,  $R$ ,  $Q_L$ ,  $V_{CC}$ , and the transistor voltage-saturation offset voltage  $V_o$  is least-squares fitted to the data in Table I, over the entire range of  $Q_L$  from 1.7879 to infinity, within a deviation of  $\pm 0.15\%$ , by a second-order polynomial function of  $Q_L$ :

$$P = [(V_{CC} - V_o)^2 / R] [2/(\pi^2/4 + 1)] f(Q_L) \quad (4)$$

$$= [(V_{CC} - V_o)^2 / R] [0.576801] [1.001245 - 0.451759/Q_L - 0.402444/Q_L^2] \quad (5)$$

Hence

$$R = [(V_{CC} - V_o)^2 / P] [0.576801] [1.001245 - 0.451759/Q_L - 0.402444/Q_L^2] \quad (6)$$

Alternatively, a third-order polynomial in  $Q_L$  gives a closer least-squares fit to the data, to within  $-0.0089\%$  to  $+0.0072\%$ :

$$P = [(V_{CC} - V_o)^2 / R] [0.576801] [1.0000086 - 0.414395/Q_L - 0.577501/Q_L^2 + 0.205967/Q_L^3] \quad (5a)$$

Hence

$$R = [(V_{CC} - V_o)^2/P] [0.576801] [1.0000086 - 0.414395/Q_L - 0.577501/Q_L^2 + 0.205967/Q_L^3] \quad (6a)$$

The *effective* dc-supply voltage is the actual voltage, less the transistor voltage-saturation offset voltage, hence  $(V_{CC} - V_o)$ .  $V_o$  is zero for a field-effect transistor. For a BJT,  $V_o$  is of the order of 0.1 V at low frequencies, and up to a few volts (depending on the transistor fabrication) at frequencies higher than about  $f_T/10$ .

The design equations for  $C_1$  and  $C_2$  that fit the data in Table I are given below. The last terms in (7), (8), and (9) are adjustments to the expressions fitted to the Table-I data, to account for the small effects of the nonzero susceptance of  $L_1$ . The numerical coefficients in those last terms depend slightly on  $L_1$  and  $Q_L$ ; those dependencies will be the subject of a planned future article. For the example case of  $Q_L = 5$  and the usual choice of  $X_{L1}$  being 30 or more times the unadjusted value of  $X_{C1}$ , the adjustments for the susceptance of  $L_1$  add 2% or less to the unadjusted value of  $C_1$  and subtract 0.5% or less from the unadjusted value of  $C_2$ .

$$C1 = [1/(2\pi f R)] (\pi^2/4 + 1) (\pi/2) [0.99866 + 0.91424/Q_L - 1.03175/Q_L^2] + [0.6/(2\pi f)^2 L_1] \quad (7)$$

$$= [1/34.2219 f R] [0.99866 + 0.91424/Q_L - 1.03175/Q_L^2] + 0.6/(2\pi f)^2 L_1 \quad (8)$$

$$C2 = [1/(2\pi f R)] [1/(Q_L - 0.104823)] [1.00121 + 1.01468/(Q_L - 1.7879)] - [0.2/(2\pi f)^2 L_1] \quad (9)$$

Finally,  $L_2$  is determined by (a) the designer's choice<sup>2</sup> for  $Q_L$  and (b) the value of  $R$  from (3) or (3a):

$$L_2 = Q_L R / 2\pi f \quad (10)$$

Equations (4) through (9) are more accurate than the older versions in [1], [2], [4], and [6].

## 5. ACCURACY OF DESIGN EQUATIONS

The maximum deviations of (5) from the tabulated values in Table I are  $\pm 0.15\%$ ; those of (5a) are  $-0.0089\%$  and  $+0.0072\%$ ; those of (7) and (8) are  $\pm 0.13\%$ ; and those of (9) are  $\pm 0.072\%$ . Kazimierczuk and Puczko [5] give tables of numerical data (similar to Table I here), obtained by a Newton's-method numerical solution of a system of analytical circuit equations they derived, and other useful numerical and graphical data. The tabulated values of  $P$  in [5] are within  $-0.13\%$  to  $+0.47\%$  of the values obtained from the continuous function (3) above. Those differences include (a) the error in the fitting of the continuous function in (3) to the discrete values in Table I ( $\pm 0.15\%$ ) and (b) the differences (if any) between the numerical results of [5] and of Table I here. Those two sets of tabulated values can be compared directly at only their two values of  $Q_L$  in common: infinity (identical results) and 1.7879 ([5] has the same capacitance values and 0.28% lower  $P$ ). The independently computed sets of data here and in [5] agree well (a maximum difference of about 0.3%), giving confidence in the validity of both.

## 6. HARMONIC FILTERING AND ASSOCIATED CHANGES TO DESIGN EQUATIONS

The power in (5) or (5a) is the total output power, at the fundamental and harmonic frequencies. Most of the power is at the fundamental frequency. The strongest harmonic is the second, with a voltage or current amplitude at  $R$  of  $0.51/Q_L$ , relative to the fundamental. For example, with  $Q_L = 5.1$ , the second-harmonic power is -20 dBc (1% of the fundamental power) without any filtering. Even-order harmonics can be canceled with a push-pull circuit, if desired. In that case, the

strongest harmonic is the third, at an amplitude of  $0.080/Q_L$  relative to the fundamental, hence -36 dBc (0.025% of the fundamental power) without filtering, for the same example  $Q_L$  of 5.1 . Sokal and Raab [11] give the harmonic spectrum as a function of the chosen  $Q_L$ .<sup>5</sup>

If the circuit includes a low-pass or band-pass filter between  $R$  and the  $C_2$ - $L_2$  branch instead of being a direct connection as in Fig. 2, the fractions of the output power contained in each of the harmonics will decrease, according to the transmission function of the filter at the harmonic frequencies. As a small side-effect, the total output power and the waveforms of switch voltage and  $C_2$ - $L_2$  current will change slightly, requiring small changes to the numerical coefficients in (6) through (9) above, and in Table I and [5]. New sets of numerical values can be calculated quickly with the help of a computer program such as HEPA-PLUS [7], described briefly in Sections 7 and 8 below, and available from the author's employer.

## 7. OPTIMIZING EFFICIENCY

The highest efficiency is obtained by minimizing the *total* power dissipated while the amplifier is delivering a desired output power. That can be done by modifying the waveforms slightly away from the nominal ones shown in Fig. 3, allowing *some* of the components of power dissipation to increase, while having *other* components of power dissipation *decrease by larger amounts*. For example, allowing the minimum of the voltage waveform to be at about 20% of the peak voltage, instead of at zero, increases the  $C_1$ -discharge power loss, but it reduces the rms/average ratio of the current waveform and the peak/average ratio of the voltage waveform. Both of those effects can be exploited to obtain a specified output power with a specified safe peak transistor voltage, with lower rms currents in the transistor,  $L_1$ ,  $L_2$ ,  $C_1$ , and  $C_2$ . That reduces their  $i^2R$  dissipations. If their series

resistances are large enough, the decrease in their  $i^2R$  power losses can outweigh the increase of  $C_1$ -discharge power loss.

The power loss in the transistor  $R_{on}$  and in discharging a partially charged  $C_1$  are not functions of the design frequency ( $C_1$  is inversely proportional to frequency, so the product  $f(C_1V^2/2)$  is independent of frequency). For given types of C or L components, losses in capacitor ESRs (including that in the transistor's  $C_{out}$ ) increase with design frequency, inductor core losses increase, and inductor winding losses decrease.

The optimum trade-off depends on the specific combination of parameter values of the types of components being considered in a particular design. (It does not vary appreciably from one unit to another of a given design.) No *a priori* explicit analytical method yet exists for achieving the optimum trade-off among all of the components of power loss. Optimization is a numerically intensive task, too difficult to do by explicit analytical methods. But computerized optimization is practical. For example, running on an IBM-PC-compatible computer with a Pentium III/667-MHz processor, a commercially available program HEPA-PLUS [7], developed specifically for high-efficiency power amplifiers, designs a nominal-waveforms Class-E amplifier in a time too short to observe, simulates the circuit in 0.008 seconds, and optimizes the design automatically, according to user-specified criteria, in about 2.4 seconds. The program uses double-precision computation for accuracy and robustness, yielding the circuit voltage and current waveforms and their spectra, dc input power, RF output power, and all components of power dissipation.

## **8. EFFECTS OF NON-IDEAL COMPONENTS**

Many of the non-idealities of the circuit components can be included in an analytical solution if the circuit is operating with the nominal switch-voltage waveform, but the task becomes progressively more difficult as one attempts to include more of those effects simultaneously, and

becomes impossible if the circuit is not operating at the nominal-waveforms conditions. The HEPA-PLUS computer program [7], mentioned above, simulates an expanded version of the circuit of Fig. 2 in any arbitrary operating condition (nominal or non-nominal waveforms). It includes all important "real-world" non-idealities of the transistor, the finite-Q power losses of all inductors and capacitors, and parasitic wiring inductances in series with  $C_1$  and in series with the transistor. Details are available from the author's employer.

## **9. APPLICABLE FREQUENCY RANGE IS ABOUT 3 MHz TO 10 GHz (as of 1999)**

The Class-E amplifier can operate at arbitrarily low frequencies, but below about 3 MHz, one of the three types of switching-mode Class-D amplifier might be preferred because it can provide as good efficiency as the Class-E, with about 1.6 times as much output power per transistor, but with the possible disadvantage that transistors must be used in pairs, *vs.* the single Class-E transistor. Class E is preferable to Class D at frequencies higher than about 3 MHz, for its higher efficiency, easier driving of the transistor input port, and less-detrimental effects from parasitic inductance in the output-port circuit. The upper end of the useful frequency range for the low-order Class E is the frequency at which the achievable turn-off switching time is of the order of 17% of the RF period. In a Class-B amplifier, the turn-off transition time is 25% of the period. Therefore a low-order Class-E circuit will work well with a particular transistor at frequencies up to about  $17\%/25\% = 70\%$  of the frequency at which that transistor works well in a Class-B amplifier. (Unpublished higher-order Class-E circuits can operate efficiently at frequencies up to about double that of the low-order version.) Class-E circuits have been made successfully at frequencies up to 10 GHz [42]. Several microwave designers have reported achieving remarkably high efficiency by driving the amplifier into

saturation and using a favorable combination of series inductance to the load resistance [13] or fundamental and harmonic load impedances [14]-[20]. (The authors of [13]-[20] found the favorable tuning condition by using an automatic tuner and/or a circuit-simulation program to make an exhaustive search over the multi-dimensional impedance space to discover a favorable combination of circuit-element values, rather than by using *a priori* explicit design equations.) Secchi [13] and Mallet *et al* [14] provided oscillograms of their drain-voltage and collector-voltage waveforms. Inspection of the  $V_{ds}$  waveform in [13, Fig. 2] shows a nominal Class-E waveform with  $R_{DS(on)} = (2.7 \text{ V}) / (0.688 \text{ A}) = 3.9 \text{ ohms}$ . The waveforms in Fig. 2(b) of [14] are Class E, but with an unusually small conduction angle. Probably higher output power could be obtained by increasing the conduction angle and modifying the load-network impedance accordingly. This author does not know the operating mode of [15]-[20]; very likely those amplifiers are distributed-elements versions (see below) of Class E, achieved empirically.

*Distributed vs. lumped elements:* High-efficiency waveforms similar to those in Figs. 1 or 3 can be generated with lumped and/or distributed elements. At a given frequency, the choice depends on the available components and the trade-offs among their sizes, costs, quality factors, and parasitic effects. [12], [21]-[23], [41], and [42] were transmission-line versions of Class E, operating at 10, 8.35, 5, 2, 1, and 0.5 GHz. The 5-, 2-, and 1-GHz circuits were described as having been designed *a priori* by explicit design procedures, worked as expected, and were operated and measured without making any experimental adjustment.

## 10. EXPERIMENTAL RESULTS

Table II summarizes representative reported Class-E performance (as of 1999), from 44 kW PEP at 0.52-1.7 MHz to 1.41 W at 8.35 GHz and 100 mW at 10 GHz.

**TABLE II. EXAMPLE CLASS-E POWER AMPLIFIERS**

Freq./Power	Transistor	Collector/Drain Efficiency/PAE	Organization	Approx. Year/Ref. No.
0.52-1.7 MHz/44 kW PEP	push-pull MOSFETs	95%	Broadcast Electronics, Inc.	1992/[34]
14 MHz/110 W	Internat'l Rectifier IRF540	92%	Design Automation, Inc.	1986/[36]
13.56, 27.12 MHz/2 kW	MOSFET	90%	Dressler Hochfrequenztechnik	1993
13.56 MHz/3 kW, 5.5 kW	MOSFET	?	Adv'd Energy Industries, Inc.	1992-1997
27.12 MHz/22 W	Internat'l Rectifier IRF510	89-92%	Design Automation, Inc.	1991/[37]
145 MHz/2.58 W	Siliconix VMP4 MOSFET	96.5/81.3%*	École Polytech. Féd. Lausanne	1980/[32]
300 MHz/30 W	push-pull BJTs	89%	Harris RF Communications	1992/[39]
450 MHz/14.96 W	combine 4 modules using Motorola MRF873 BJT	89.5%	City Univ. of Hong Kong	1997/[30]
500 MHz/0.55 W	Siemens CLY5 GaAs MESFET	83/80%	Univ. of Colorado	1995/[23]
840 MHz/1.24 W	GaAs MESFET	79/77%	S. C. Cripps	<1999/[40]
850 MHz/1.6 W	GaAs MMIC	62.3% PAE	M/A-COM	1994/[26]
1 GHz/0.94 W	Siemens CLY5 GaAs MESFET	75%/73%	Univ. of Colorado	1995/[22, 21]
2.45 GHz/1.27 W	Fujitsu FLC30 GaAs MESFET	72% PAE	RCA David Sarnoff Res. Ctr.	1981/[13]
2.45 GHz**/210 mW	Raytheon RPC3315 MESFET	77/68/71%*	Design Automation, Inc.	1979/[33]
5 GHz/0.61 W	Fujitsu FLK052WG MESFET	81/72%	Univ. of Colorado	1996/[12, 23]
8.35 GHz/1.41 W	Fujitsu FLK202MH-14 MESFET	64/48%	Univ. of Colorado	1999/[41]
10 GHz/100 mW	Alpha Ind. AFM04P2 MESFET	74/62%	Univ. of Colorado	1999/[42]

\*Overall effy =  $P_{out}/(P_{dc} + P_{input-drive})$       \*\*1/20 scaled-frequency model at 122.5 MHz; see text in References list at [33].

## 11. TUNING PROCEDURE

Fig. 3 shows the nominal Class-E transistor-voltage waveform in the low-order circuit of Fig. 2: at the transistor's turn-on time, the waveform has zero slope, and has zero voltage for a FET or  $V_{CE(sat)}$  for a BJT. An actual circuit, or a circuit in the HEPA-PLUS computer program [7], can be brought from an off-nominal condition to that nominal-waveform condition by adjusting  $C_1$ ,  $C_2$  and/or  $L_2$ , and the load resistance  $R$  if  $R$  is not already the value that will provide the desired output power. The desired value of  $R$  is obtained from (6) or (6a) after having applied the allowance for parasitic resistances discussed in the last paragraph of Section 3 above.<sup>6</sup>

After adjusting the antenna tuner or the load-impedance-transforming network (located between the antenna or other load and the right-hand end of  $L_2$  in Fig. 2) so as to provide an input-port resistance of  $R$ , there might be residual series inductive and/or capacitive reactances in series with  $R$ . The series inductive reactance adds to the reactance of  $L_2$ , and the series capacitive reactance adds to the reactance of  $C_2$ . Then the amplifier would operate with an off-nominal  $V_{CE}$  waveform, and possibly an off-nominal value of output power, because the effective values of  $L_2$  and  $C_2$  would differ from the design values. To correct for that, the reactances of  $L_2$  and  $C_2$  should be reduced by the amounts of the residual inductive and capacitive series reactances of the input-port impedance of the tuner or impedance-transforming network. The following text and figures explain how to make those adjustments to the circuit, if needed, *without needing to know, a priori, the values of those residual series reactances*. The text is in terms of a BJT; for a FET, substitute " $V_{DS}$ " for " $V_{CE}$ ."

The circuit parameters were chosen, via equations (2) through (10), to meet a chosen set of requirements. The circuit will operate with the nominal Class-E waveform, while delivering the specified output power at the specified frequency, if the chosen parameter values are installed in the actual hardware. The possible need for tuning results from (a)

tolerances on the components values (normally not a problem, because Class E has low sensitivity to component tolerances) and (b) the possibility of unknown-value inductive and capacitive reactances being inserted in series with  $R$  (hence in series with  $L_2$  and  $C_2$ ), after the load resistance has been transformed to the chosen value of  $R$ . Those series reactances require that the reactances of  $L_2$  and  $C_2$  be reduced by the amounts of the unknown inserted inductive and capacitive series reactances. But how to do that when those inserted reactances are unknown?

Fig. 4 shows a  $V_{CE}$  waveform for an amplifier with off-nominal tuning, with the waveform features labeled for subsequent reference in the text. If we know *a priori* how changes of  $L_2$  and  $C_2$  will affect that waveform, we can adjust two parameters ( $L_2$  and  $C_2$ ) so as to meet two criteria at the operating frequency: (a) achieve the nominal  $V_{CE}$  waveform of Fig. 3 and (b) deliver the specified value of output power.

Fig. 5 shows how  $L_2$  and  $C_2$  affect the  $V_{CE}$  waveform. We know also that increasing  $L_2$  reduces the output power, and vice versa. With the preceding information, and with (a) an oscilloscope displaying the  $V_{CE}$  waveform and (b) a directional power meter indicating the power being delivered to the load, we can adjust  $L_2$  and  $C_2$  so as to fulfill simultaneously the two desired conditions (nominal waveform and desired output power) *even if the inductive and capacitive reactances in series with  $R$  are unknown*.

If  $C_1$  (comprising the transistor output capacitance and the external capacitor connected in parallel with it) is within about 10% of the intended value,  $C_1$  will normally not need adjustment. But in case of a possible large deviation from the design value,  $C_1$  can also be adjusted so as to achieve the nominal  $V_{CE}$  waveform, using the information in Fig. 5 about the effects of  $C_1$  on the  $V_{CE}$  waveform. In that case, the three components  $C_1$ ,  $C_2$ , and  $L_2$  can be adjusted so as to achieve three conditions simultaneously at the operating frequency: desired output power, transistor voltage of  $V_{CE(sat)}$  just before transistor turn-on, and zero slope of the  $V_{CE}$  waveform just before turn-on. The following diagrams and text explain how to adjust  $C_1$ ,  $C_2$ ,  $L_2$ , and  $R$  (if desired) to

adjust the shape of the  $V_{CE}$  waveform.

Changes in the values of the load-network components affect the  $V_{CE}$  waveform as follows, illustrated in Fig. 5:

Increasing  $C_1$  moves the trough of the waveform upwards and to the right.

Increasing  $C_2$  moves the trough of the waveform downwards and to the right.

Increasing  $L_2$  moves the trough of the waveform downwards and to the right.

Increasing  $R$  moves the trough of the waveform upwards ( $R$  is not normally an adjustable circuit element).

Knowing these effects, you can adjust the load network for nominal Class-E operation by observing the  $V_{CE}$  waveform. (Depending on the settings of the circuit component values, the zero-slope point and/or the negative-going jump at transistor turn-on might be hidden from view, as in some of the waveforms in Fig. 6. If that occurs, the locations of those features on the waveform can be estimated by extrapolating from the part of the waveform that can be seen.) The adjustment procedure is as follows:

1. Set  $R$  to the desired value or accept what exists.
2. Set  $L_2$  for the desired  $Q_L = 2\pi fL_2/R$  or accept what exists.
3. Set the frequency as desired.
4. Set the duty ratio ( $T_{on}/T$  in Fig. 4) to the desired value (usually 50%), with  $V_{CC}$  set to approximately 20% of the intended final value. If the transistor turn-on is visible on the  $V_{CE}$  waveform (as in Fig. 4), measure the duty ratio. Otherwise, observe the  $V_{BE}$  waveform and assume that turn-on occurs when the positive-going edge of  $V_{BE}$

reaches +0.8 V and turn-off occurs when the negative-going edge of  $V_{BE}$  reaches 0 V. (The preceding voltage values are for a silicon NPN transistor at room temperature. For other types of transistors, make appropriate modifications to the voltage values.)

5. Observe the trough of the  $V_{CE}$  waveform:
  - A. At the zero-slope point: What is the voltage relative to  $V_{CE(sat)}$ ? More positive, more negative, or equal?
  - B. At transistor turn-on: What is the slope? Positive, negative, or zero?

If these points are unobservable because they lie below the zero-voltage axis, the voltage at zero slope is “more negative.” Estimate the slope at turn-on by extrapolation of the waveform.

If the voltage at zero slope is unobservable because transistor turn-on occurs before zero slope is reached, the slope at turn-on is “negative.” Estimate the voltage at zero slope by extrapolation of the waveform.

If you cannot estimate the  $V_{CE}$  or the slope by extrapolation, assume that  $V_{CE}$  is “equal” or that the slope is “zero.”

6. Adjust  $C_1$  and/or  $C_2$  as shown in Fig. 5, and in expanded form in Fig. 6.
7. If  $V_{CC}$  is now the desired value, go to Step 8. If  $V_{CC}$  is less than the desired value, increase  $V_{CC}$  by up to 50% and readjust the duty ratio,  $C_1$ , and  $C_2$  as needed. (The  $V_{CC}$  increase will decrease the effective value of the voltage-dependent  $C_{CB}$ , causing the effective value of  $C_1$  to be reduced. Therefore  $C_1$  will need to be increased slightly.)
8. For a final check of the adjustments, increase  $C_1$  slightly to generate an easily visible marker of transistor turn-on: the small negative-going step of  $V_{CE}$ . Verify that the duty ratio is the desired value (usually 50%) and that the waveform slope is

zero at turn-on time. Now return  $C_I$  to the value that brings the waveform to  $V_{CE(sat)}$  at turn-on time (and also eliminates the marker).

## 12. GATE- AND BASE-DRIVER CIRCUITS

A simplistic view of the driver stage is that its design is much less important than the design of the output stage, because the power level at the driver stage is much lower than that at the output stage, by a factor equal to the power gain of the output stage, typically a factor of about 10 to 100. That simplistic view is not correct, because the output transistor will not operate as intended if its input is not driven properly. If the output transistor does not operate as intended, the output stage will not operate as intended, either. The resulting output-stage performance might or might not be acceptable. The output-stage transistor will operate properly as a switch, as intended, if its input port (Gate-Source of a FET or Base-Emitter of a BJT) is driven properly by the output of its driver stage. The driver stage must provide the output specified below. Symbols for FETs are used below; you can convert to BJT symbols if you wish.

1. Enough "off" bias during the "off" interval to maintain the drain or collector current at an acceptably small value. If you are willing to tolerate a power loss of  $x$  fraction of the normal dc input power due to non-zero "off"-state current, the drain or collector current during the "off" interval can be up to  $I_{D(off)} = x I_{DD} [1/(1 - D)]$ , where  $I_{DD}$  is the dc current drawn from the  $V_{DD}$  dc drain-voltage supply, and  $D$  is the output-transistor's "on" duty ratio (usually 0.50, but it can be any value you choose and provide for in the choice of  $R$ ,  $L$ , and  $C$  values in the load network).  
Example: If you are willing to tolerate 1% additional power consumption from the  $V_{DD}$  voltage supply caused by the non-zero "off"-state current, if  $I_{DD}$  is 5 A, and if  $D$  is

the usual value of 0.50, you can tolerate an "off"-state drain current of 0.01 [5 A]  $[1/(1 - 0.50)] = 0.1 \text{ A} = 100 \text{ mA}$ . That's easy. For example, the International Rectifier IRF540 (rated 100 V, 28 A) is specified for 0.25 mA maximum at  $V_{GS} = 0$  and  $V_{DS} = 80 \text{ V}$ , at  $T_J = 150 \text{ C}$ , a factor of 400 smaller than the 100 mA you are willing to accept in this example.

2. Enough "on" drive during the latter 3/4 of the "on" interval to maintain a low-enough  $R_{on}$ . You can choose what is "low-enough" for your purposes; refer to the last three sentences of Section 3. Why "the latter 3/4 of the 'on' interval": The current  $i(t)$  during the first 1/4 of the "on" interval is small enough that  $[i(t)]^2 R_{on}(t)$  can be acceptably small for a fairly high  $R_{on}(t)$  because the small  $i(t)$  during the first 1/4 of the "on" interval causes an even smaller  $[i(t)]^2$  (the square of a small number is even smaller than the number before squaring).
3. Enough turn-off drive to turn-off the drain or collector current from 100% to 0% in a fall-time  $t_f$  fast enough to make the turn-off power dissipation an acceptably small fraction of the output power. That fraction is  $(2\pi A)^2/12$ , where  $A = (1 + 0.82/Q_L)(t_f/T)$  and  $T = 1/f$  is the period of the operating frequency  $f$ . Choose the acceptable fraction of the output power to be dissipated during the non-zero turn-off switching time. Then calculate the required drain-or collector-fall time  $t_f$  that must result from the "enough turn-off drive." Then provide sufficient turn-off drive to accomplish your chosen objective, according to the characteristics of the chosen output transistor. (That is the subject of an intended future publication.) For example, if you are willing to have the turn-off power dissipation ( $P_{diss,turn-off}$ ) be 6% of the output power, and if  $Q_L = 3$ , the allowable value for

$$t_f/T = \sqrt{[12 P_{diss,turn-off}/P] / [2\pi (1 + 0.82/Q_L)]}$$

is  $\sqrt{[12 (0.06)] / [2\pi (1 + 0.82/3)]} = 0.106$ , *i.e.*,  $t_f$  can be as large as 10.6% of the period.

4. Enough turn-on drive to turn-on the output transistor fast enough to make an acceptably small power dissipation during the turn-on switching. That has never been a problem with all of the drivers I have seen. Most driver circuits turn the transistor "on" and "off" with about the same switching times. If the more-important turn-off switching time is fast enough, the accompanying turn-on switching time will be more than fast enough.

The input-port characteristics of BJTs, MOSFETs, and MESFETs are enough different that different types of driver circuits should be used to drive those three different types of transistors.<sup>7</sup> I intend to publish one or more future articles that discuss in detail driver circuits that meet criteria 1-4 above, for MOSFETs, MESFETs, and BJTs. A brief summary of driving a MOSFET or a MESFET follows. The polarity descriptions assume N-channel or NPN; reverse the polarity descriptions for P-channel or PNP.

The best gate-voltage drive is a trapezoid waveform, with the falling transition occupying 30% or less of the period. (Trade-off: The shorter the turn-off transition time, the smaller will be the power dissipation in the output transistor during turn-off switching, but the larger will be the power consumption of the driver stage. For both MOSFETs and MESFETs, the optimum drive minimizes *the sum* of the output-stage power dissipation and the driver-stage power consumption.) The upper level of the drive waveform should be safely below the MOSFET's gate-source maximum voltage rating, or the MESFET's gate-source voltage at which the gate-source diode conducts enough current to cause either of two undesired effects: (a) metal migration of the gate metalization at an undesirably rapid rate (making the transistor operating lifetime shorter than desired) or (b)

enough power dissipation to reduce the overall efficiency more than the efficiency is increased by the lower dissipation in the lower  $R_{DS(on)}$  that results from a higher upper level of the drive waveform. The lower level of the trapezoid should be low enough to result in a satisfactorily small current during the transistor's “off” state, discussed in requirement 1 above.

A sine-wave is a usable (but not optimum) approximation to the trapezoid waveform described above. To obtain an output-transistor “on” duty ratio of 50% (usually the best choice, but a larger or smaller duty ratio can be used if appropriate component values are used in the load network), the zero-level of the sine-wave should be positioned slightly above the FET's turn-on threshold voltage.

A better approximation is to remove the part of the sine-wave that goes below the  $V_{GS}$  value that ensures fully “off” operation, replacing it with a constant voltage at that  $V_{GS}$  value. This reduces the input-drive power by slightly less than 50%, almost doubling the power gain of the output stage. A planned future article will discuss in detail a simple circuit that generates such a waveform.

## ACKNOWLEDGEMENTS

The author thanks Prof. Alan D. Sokal of the Physics Department, New York University, for many helpful discussions and for producing the numerical solutions in Table I and the initial set of equations that fit the data in Table I; John E. Donohue, formerly of Design Automation, Inc., for computing the coefficients of  $f(Q_L)$  in (4) to fit the data in Table I, yielding (5) and (6); and Dr. Richard Redl of ELFI S.A., for computing the improved-accuracy functions in (5a), (7), and (9) that fit the  $P$ ,  $C_1$ , and  $C_2$  data of Table I.

The first version of this text was “Class E RF Power Amplifiers,” published in *QEX* magazine, Jan./Feb. 2001, Issue No. 204, pp. 9-20, copyright 2000, American Radio Relay League, Inc. (“ARRL”). That

article added significant new information to text taken from “Class-E High-Efficiency Power Amplifiers, from HF to Microwave,” presented by this author at the IEEE International Microwave Symposium, June 1998, Baltimore, Maryland, U.S.A., and “Class-E Switching-Mode High-Efficiency Tuned RF/Microwave Power Amplifier: Improved Design Equations,” presented by this author at the IEEE International Microwave Symposium, June 2000, Boston, Massachusetts, U.S.A. The texts of those presented papers are included in the printed and CD-ROM versions of the *Proceedings* of those conferences, copyright 1998 and 2000, respectively, by IEEE. The author thanks IEEE for permission to use the previously published material. A short summary of this material was presented at the AACD 2001 conference in Noordwijk, The Netherlands, April 24-26, 2001. The full text was published as a chapter in pp. 269-301 of the book that was the conference record: *Analog Circuit Design — Scalable Analog Circuit Design, High-Speed D/A Converters, RF Power Amplifiers*, Kluwer Academic Publishers, Dordrecht, The Netherlands, 2002, ISBN 0-7923-7621-8. That book chapter was an edited version [including correction of a typographical error in (1)], of the *QEX* publication. This text contains updates (February 2006) to the chapter of the Kluwer book. The author thanks ARRL and Kluwer for their permissions to re-use the previous material, with kind permission from Springer Science and Business Media, of which Kluwer is now a part.

## FOOTNOTES

<sup>1</sup>Most papers on the Class E amplifier of Fig. 2 (including this one) define  $Q_L$  as  $2\pi f L_2/R$ . A few papers, *e.g.*, [3], define  $Q_L$  as  $1/(2\pi f C_2 R)$ . Kazimierczuk and Puczek [5], to their credit, give *both* values in their tabulations, as  $Q_L$  and as  $Q_L$ , respectively.

<sup>2</sup>The choice of  $Q_L$  involves a trade-off among operating bandwidth (wider with low  $Q_L$ ), harmonic content of the output power [11] (lower with high  $Q_L$ ), and power loss in the parasitic resistances of the load-network inductor  $L_2$  and capacitor  $C_2$  (lower with low  $Q_L$ ).

<sup>3</sup>The nominal switch-voltage waveform has zero voltage and zero slope at the time the switch will be turned on. [1]-[4], and papers by other authors, referred to that nominal waveform as the “optimum” waveform, a misnomer. That waveform is “optimum” for yielding high efficiency in the case of a switch with negligibly small series resistance. But if the switch has appreciable resistance, the efficiency can be increased by moving away slightly from the nominal waveform, to a waveform whose voltage at the switch turn-on time is of the order of 20% of the peak voltage. No analytical optimization procedure yet exists, but the circuit can be optimized numerically, by a computer program such as HEPA-PLUS [7], discussed briefly in Sections 7 and 8.

<sup>4</sup>Beware: A few publications define  $D$  as the fraction of the period that the switch is *off*.

<sup>5</sup>Updates to [11]: (a) Delete the column in Table I for  $Q_L = 1$  because  $Q_L$  must be  $\geq 1.7879$  to obtain the nominal Class-E collector/drain-voltage waveform in the circuit described in [1]-[6], when the switch duty ratio  $D$  is 50%. (b) In (2), change the factor 1.42 to 1.0147; the factor 2.08 to 1.7879; and the factor 0.66 to 0.773. (c) Recalculate the numerical values of  $I_n/I_1$ , using (2) with the revised factors.

<sup>6</sup>The 1997 two-part *QST* article [43] by Eileen Lau (KE6VWU) *et al*, about 300-watt and 500-watt 40-metre transmitters, discussed tuning in Part 2, but without a description of how to adjust the load-network components values to obtain the nominal Class-E voltage waveform, as is included in Section 11 here.

<sup>7</sup>In the early 1980s, I made a driver circuit that would drive a BJT or a MOSFET interchangeably, with no change needed in the driver or in the power-amplifier’s input circuit. That driver was used in a Class-E demonstrator circuit, so that a person evaluating Class-E technology could insert *any* type of transistor for test purposes, be it an NPN BJT or an N-channel MOSFET, and observe that the changes of power-amplifier output power and efficiency were almost unnoticeably small, when inserting any of thirty transistors of different type numbers and manufacturers, some BJT and some MOSFET. Some of those people, accustomed to working with conventional Class-C power amplifiers, were astonished when they witnessed the results of that test.

## REFERENCES

- [1] N. O. Sokal and A. D. Sokal, "High-efficiency tuned switching power amplifier," *U. S. Patent 3,919,656*, Nov. 11, 1975 (now expired). [Includes a detailed technical description.]
- [2] \_\_\_\_\_, "Class E — a new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-

- 10, no. 3, pp. 168-176, June 1975. [The text of [1] cut to half-length; retains the most-useful information. Text corrections are available from N. O. Sokal.]
- [3] F. H. Raab, "Idealized operation of the Class E tuned power amplifier," *IEEE Trans. Circuits and Systems*, vol. CAS-24, no. 12, pp. 725-735, Dec. 1977.
- [4] N. O. Sokal and A. D. Sokal, "Class E switching-mode RF power amplifiers – low power dissipation, low sensitivity to component tolerances (including transistors), and well-defined operation," *Proc. 1979 IEEE ELECTRO Conference, Session 23*, New York, NY, 25 April 1979; reprinted in *R.F. Design*, vol. 3, no. 7, pp. 33-38, 41, July/Aug. 1980. [Includes plots of efficiency vs. frequency with  $Q_L$  as a parameter and efficiency vs. variations of all circuit parameters.]
- [5] M. K. Kazimierczuk and K. Puczko, "Exact analysis of Class E tuned power amplifier at any  $Q$  and switch duty cycle," *IEEE Trans. Circuits and Systems*, vol. CAS-34, no. 2, pp. 149-159, Feb. 1987.
- [6] N. O. Sokal, "Class E high-efficiency switching-mode power amplifiers, from HF to microwave," *1998 IEEE MTT-S International Microwave Symposium Digest*, June 1998, Baltimore, MD, CD-ROM IEEE Catalog No. 98CH36192 and also *1998 Microwave Digital Archive, IEEE Microwave Theory and Techniques Society*, CD-ROM IEEE Product # JP-180-0-081999-C-0.
- [7] HEPA-PLUS computer program, available from the author's employer, Design Automation, Inc., 4 Tyler Rd., Lexington, MA 02420-2404, U.S.A.
- [8] Ch. P. Avratoglou and N. C. Voulgaris, "A new method for the analysis and design of the Class E power amplifier taking into account the  $Q_L$  factor," *IEEE Trans. Circuits & Systems*, vol. CAS-34, no. 6, pp. 687-691, June 1987.
- [9] F. H. Raab and N. O. Sokal, "Transistor power losses in the Class E tuned power amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, no. 6, pp. 912-914, Dec. 1978.
- [10] N. O. Sokal and R. Redl, "Power transistor output port model for analyzing a switching-mode RF power amplifier or resonant converter," *RF Design*, June 1987, pp. 45-48, 50-53.
- [11] N. O. Sokal and F. H. Raab, "Harmonic output of Class-E RF power amplifiers and load coupling network design," *IEEE J. Solid-State Circuits*, vol. SC-12, no. 1, pp. 86-88, Feb. 1977. [Text corrections are available from N. O. Sokal.]
- [12] E. W. Bryerton, W. A. Shiroma, and Z. B. Popovic', "A 5-GHz high-efficiency Class-E oscillator," *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 12, Dec. 1996, pp. 441-443. [300 mW to external load at 5 GHz at 59% conversion efficiency (remaining RF output from transistor was used for input-drive to oscillator).]
- [13] F. N. Sechi, "High efficiency microwave FET amplifiers," *Microwave J.*, Nov. 1981, pp. 59-62, 66. [Several "saturated Class B and Class AB" amplifiers at 2.45 GHz, using several types of GaAs MESFETs: 0.97 W at 71% PAE, 1.2 W at 72% PAE, 1.27 W at 72% PAE. The  $V_{ds}$  waveform in Fig. 2 is a low-order Class-E waveform with apparently  $R_{DS(on)} = (2.7 \text{ V})/(0.688 \text{ A}) = 3.9 \text{ ohms}$ . All drain-current waveforms are sinusoidal; that seems to be inconsistent with the non-sinusoidal drain-voltage waveforms. Perhaps the bandwidth of the current-

- sensing instrumentation was sufficient to display only the fundamental component of the probably non-sinusoidal current waveforms.]
- [14] A. Mallet, D. Floriot, J. P. Viaud, F. Blache, J. M. Nebus, and S. Delage, "A 90% power-added-efficiency GaInP/GaAs HBT for L-band and mobile communication systems," *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 3, pp. 132-134, March 1996. [Fig. 1 is well-annotated with the HBT parameter values, but it omits values for  $C_{be}$  and  $C_{bc}$ .]
- [15] S. R. Mazumder, A. Azizi, and F. E. Gardiol, "Improvement of a Class-C transistor power amplifier by second-harmonic tuning," *IEEE Trans. MTT*, vol. MTT-27, no. 5, pp. 430-433, May 1979. [800 mW output at 865 MHz, 53.3% collector efficiency, coupled-TEM-bar circuit. In a similar paper at the 9th European Microwave Conference, Sept. 1979, the same authors reported 64% collector efficiency at 800 mW output at 850 MHz.]
- [16] J. J. Komiak, S. C. Wang, and T. J. Rogers, "High efficiency 11 watt octave S/C-band PHEMT MMIC power amplifier," *Proc. IEEE 1997 MTT-S International Microwave Symp.*, Denver, CO, June 8-13, 1997, IEEE Catalog No. 0-7803-3814-6/97, pp. 1421-1424. [17 W at 5.1 GHz, 54.5% PAE, harmonic tuning]
- [17] J. J. Komiak, L. W. Yang, "5 watt high efficiency wideband 7 to 11 GHz HBT MMIC power amplifier," *Proc. IEEE 1995 Microwave and Millimeter-Wave Monolithic Circuits Symp.*, Orlando, FL, May 15-16, 1995, IEEE Catalog No. 95CH3577-7, pp. 17-20.
- [18] W. S. Kopp and S. D. Pritchett, "High efficiency power amplification for microwave and millimeter frequencies," *1989 IEEE MTT-S Digest*, IEEE Catalog No. CH2725-0/89/0000, pp. 857-858.
- [19] Bill Kopp and D. D. Heston, "High-efficiency 5-watt power amplifier with harmonic tuning," *1988 IEEE MTT-S Digest*, pp. 839-842. [12 FETs in parallel produced (from Table 3) 5.27 W output (apparently 0.27 W of that is lost in power-combining network) at 10 GHz with 35.3% PAE (Abstract says 5 W at 36% PAE). Exhaustive search for best combination of impedance vs. frequency. Built with distributed elements.]
- [20] L. C. Hall and R. J. Trew, "Maximum efficiency tuning of microwave amplifiers," *1991 IEEE MTT-S Digest*, IEEE Catalog No. CH2870-4/91/0000, pp. 123-126. [Circuit simulations of optimum design found by exhaustive search of 12-dimensional parameters-space; the resulting design appears to be higher-order Class E with 3rd-harmonic resonator (Class F3).]
- [21] T. Mader, M. Markovic', Z. B. Popovic', and R. Tayrani, "High-efficiency amplifiers for portable handsets," *Conference Record, IEEE PIMRC'95* (Personal, Indoor, & Mobile Radio Communications), Sept. 1995, Toronto, Ontario, Canada, IEEE publication 0-7803-3002-1/95, pp. 1242-1245. [Class E, 0.94 W at 1 GHz, at 75% drain efficiency, 73% PAE, Siemens CLY5 GaAs MESFET]
- [22] T. B. Mader and Z. B. Popovic', "The transmission-line high-efficiency Class-E amplifier," *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 9, Sept. 1995, pp. 290-292. [0.94 W at 1 GHz at 75% drain efficiency, 73% PAE; 0.55 W at 0.5 GHz at 83% drain efficiency, 80% PAE; Siemens CLY5 GaAs MESFET]

- [23] T. B. Mader, "Quasi-optical Class-E power amplifiers," PhD thesis, 1995, Univ. of Colorado, Boulder, CO. [Class E with transmission lines: 0.55 W at 0.5 GHz at 83% drain efficiency, 80% PAE from Siemens CLY5 MESFET; 0.61 W at 5 GHz at 81% drain efficiency, 72% PAE from Fujitsu FLK052WG MESFET; four of the latter into a quasi-optical power combiner gave 2.4 W at 5.05 GHz at 74% efficiency, 64% PAE.]
- [24] T. Sowlati, C. A. T. Salama, J. Sitch, G. Rabjohn, and D. Smith, "Low voltage, high efficiency GaAs Class E power amplifiers for wireless transmitters," *IEEE J. Solid-State Circuits*, vol. 30, no. 10, pp. 1074-1080, Oct. 1995; same authors and almost-identical title and text in *Proc. IEEE GaAs IC Symposium*, Philadelphia, PA, Oct. 18-19, 1994, IEEE Catalog No. 0-7803-1975-3/94, pp. 171-174. [24 dBm = 0.25 W output at 835 MHz, at >50% power-added efficiency using integrated impedance-matching networks (PAE would be 75% with hybrid matching networks), from a 8.4-mm<sup>2</sup> GaAs IC at 2.5 Vdc]
- [25] T. Sowlati, Y. Greshishchev, C. A. T. Salama, G. Rabjohn, and J. Sitch, "Linear transmitter design using high efficiency Class E power amplifier," *Conference Record, IEEE PIMRC'95* (Personal, Indoor, & Mobile Radio Communications), Sept. 27-29, 1995, Toronto, Ontario, Canada, IEEE publication 0-7803-3002-1/95, pp. 1233-1237. [24 dBm = 251 mW at 835 MHz, 65% PAE]
- [26] J. Imbornone, R. Pantoja, and W. Bosch, "A novel technique for the design of high efficiency power amplifiers," European Microwave Conference, Cannes, France, Sept. 1994. [32.1 dBm = 1.6 W output at 850 MHz, at 62.3% power-added efficiency, from a 18-mm<sup>2</sup> GaAs IC (output stage and driver stage) with high-*Q* lumped elements, at 5 Vdc. Simulated  $V_{ds}$  and  $I_d$  waveforms for optimized output stage are Class E with  $V_{turn-on}/V_{pk} = 4.9 \text{ V}/27.4 \text{ V} = 18\%$ , as discussed in Section 7.]
- [27] K. Siwiak, "A novel technique for analyzing high-efficiency switched-mode amplifiers," *Proc. RF Expo East '90*, Nov. 1990, pp. 49-56. [higher-order Class E with 3rd-harmonic resonator (Class F3)]
- [28] C. Duvaud, S. Dietsche, G. Pataut, and J. Obregon, "High-efficient Class F GaAs FET amplifiers operating with very low bias voltages for use in mobile telephones at 1.75 GHz," *IEEE Microwave and Guided Wave Letters*, vol. 3, no. 8, pp. 268-270, Aug. 1993. [higher-order Class E with 3rd-harmonic resonator (Class F3)]
- [29] R. M. Porter and M. L. Mueller, "High power switch-mode radio frequency amplifier method and apparatus," *U. S. Patent 5,187,580*, Feb. 16, 1993. [Class E with substantial voltage at turn-on, as in Section 4 here.]
- [30] Y-O Tam and C-W Cheung, "High efficiency power amplifier with travelling-wave combiner and divider," *Int. J. Electronics*, vol. 82, no. 2, pp. 203-218, 1997. [Class E 450 MHz/5 W with 89.4% collector efficiency. The outputs of four such amplifiers were combined with a traveling-wave power-combiner, yielding 14.96 W output at 89.5% collector efficiency.]
- [31] J. E. Mitzlaff, "High efficiency RF power amplifier," *U. S. Patent 4,717,884*, Jan. 5, 1988. [1.6 W at 76% drain efficiency at 840 MHz. At least 1.5 W output with [at least?] 74% efficiency over 50-MHz band centered at 840 MHz (6% band).

Described as Class F. Appears to be high-order Class E with lumped and transmission-line resonators. Shows transistor voltage and current waveforms for three "prior-art" circuits, but not for the circuit covered by this patent. Detailed explanation of how to synthesize load network to produce desired input-port impedance vs. frequency.]

- [32] M. Kessous and J.-F. Zürcher, "Amplificateur VHF en classe E utilisant un transistor à effet de champ (FET) VMOS de puissance" (VHF Class E amplifier using VMOS power FET), *AGEN-Mitteilungen* (Switzerland), no. 30, pp. 45-49, Oct. 1980. [2.58 W output at 145 MHz at 96.5% drain efficiency, 81.3% total efficiency =  $P_{out}/(P_{dc} + P_{input-drive})$ , using Siliconix VMP-4 MOSFET]
- [33] N. O. Sokal, "Design of a Class E RF power amplifier for operation at 2.45 GHz, and tests on a scaled-frequency model at 122.5 MHz" [1/20 frequency], Oct. 1979, unpublished report of Design Automation, Inc. Project 4198. [Used Raytheon RPC3315 GaAs MESFET intended to be used at 2.45 GHz. Initial test with frequency scaled-down by factor of 20, all inductors and capacitors (including transistor capacitances and expected wiring parasitic inductances) scaled-up by factor of 20, and all resistances, voltages, and currents at intended final values. 210 mW output, 77% drain efficiency, 24 mW input drive, 9.4 dB power gain, 71% overall efficiency =  $P_{out}/(P_{dc} + P_{drive})$ , 68% PAE.]
- [34] D. W. Cripe, "Improving the efficiency and reliability of AM broadcast transmitters through Class-E power," National Association of Broadcasters annual convention, May 1992, 7 pp.
- [35] S. Hinchliffe and L. Hobson, "High power Class-E amplifier for high-frequency induction heating applications," *Electronics Letters*, vol. 24, no. 14, pp. 886-888, July 7, 1988. [>550 W at 3-4 MHz at >92% efficiency across the band, 450 W at 3.3 MHz at 96% efficiency from 104 Vdc, IRF450 MOSFET.]
- [36] R. Redl and N. O. Sokal. "A 14-MHz 100-watt Class E resonant [dc/dc] converter: principles, design considerations and measured performance," Power Electronics Conf., San Jose, CA, Oct. 1986. [Class E dc/dc converter had 87% drain efficiency at 100 W dc output. IRF540 RF power stage supplied estimated 105 W at 91.4% efficiency because of estimated 5 W loss in coupling transformer and rectifier associated with 100-W dc load.]
- [37] N. O. Sokal and Ka-Lon Chu, "Class-E power amplifier delivers 24 W at 27 MHz, at 89-92% efficiency, using one transistor costing \$0.85," *Proc. RF Expo East*, Tampa, FL, Oct. 1993, pp. 118-127, and presented at RF Expo West, San Jose, CA, March 1993 but not in *Proc.* [International Rectifier (89%) and Harris Semiconductor (92%) IRF510 SMPS MOSFET; Harris device slightly larger die, lower  $R_{DS(on)}$ , and higher efficiency. Silicon-gate  $R_g$  (about 1-2 ohms, but never specified by vendor) was borderline-acceptable at 27.12 MHz for  $i_g^2 R_g$  input-drive power.  $P_{drive}$  varies as  $f^2$ ; it would have been quite acceptable at 13.56 MHz.]
- [38] N. O. Sokal and I. Novak, "Tradeoffs in practical design of Class-E high-efficiency RF power amplifiers," *Proc. RF Expo East*, Tampa, FL, Oct. 1993, pp. 100-117, and presented at RF Expo West, San Jose, CA, March 1993, but not in *Proc.*

- [39] P. J. Poggi, "Application of high efficiency techniques to the design of RF power amplifier and amplifier control circuits in tactical radio equipment," *Proc. MILCOM'95*, San Diego, CA, Nov. 5-8, 1995, pp. 743-747.
- [40] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, Norwood, MA, 1999, ISBN 0-89006-989-1, pp. 170-177. [Fig. 6.19 on p. 176: GaAs MESFET, 840 MHz, 79% efficiency at 1.24 W output, 15 dBm (31.6 mW) input, power gain =  $1.24 \text{ W}/0.0316 \text{ W} = 39.2 = 15.9 \text{ dB}$ .]
- [41] M. D. Weiss, M. H. Crites, E. W. Bryerton, J. F. Whitaker, and Z. Popovic', "Time-domain optical sampling of switched-mode microwave amplifiers and multipliers," *IEEE Trans. MTT*, vol. 47, no. 12, pp. 2599-2604, Dec. 1999.
- [42] M. D. Weiss and Z. Popovic', "A 10 GHz high-efficiency active antenna," *1999 IEEE MTT-S International Microwave Symposium Digest*, June 13-19, 1999, Anaheim, CA, file TU4B\_5.PDF on CD-ROM IEEE Catalog No. 99CH36282C.
- [43] E. Lau (KE6VWU), K-W Chiu (KF6GHS), J. Qin (KF6GHY), J. Davis (KF6EDB), K. Potter (KC60KH), and D. Rutledge (KN6EK), "High-efficiency Class-E power amplifiers – Part 1," *QST*, vol. 81, no. 5, pp. 39-42, May 1997, and "... Part 2," vol. 81, no. 6, pp. 39-42, June 1997.

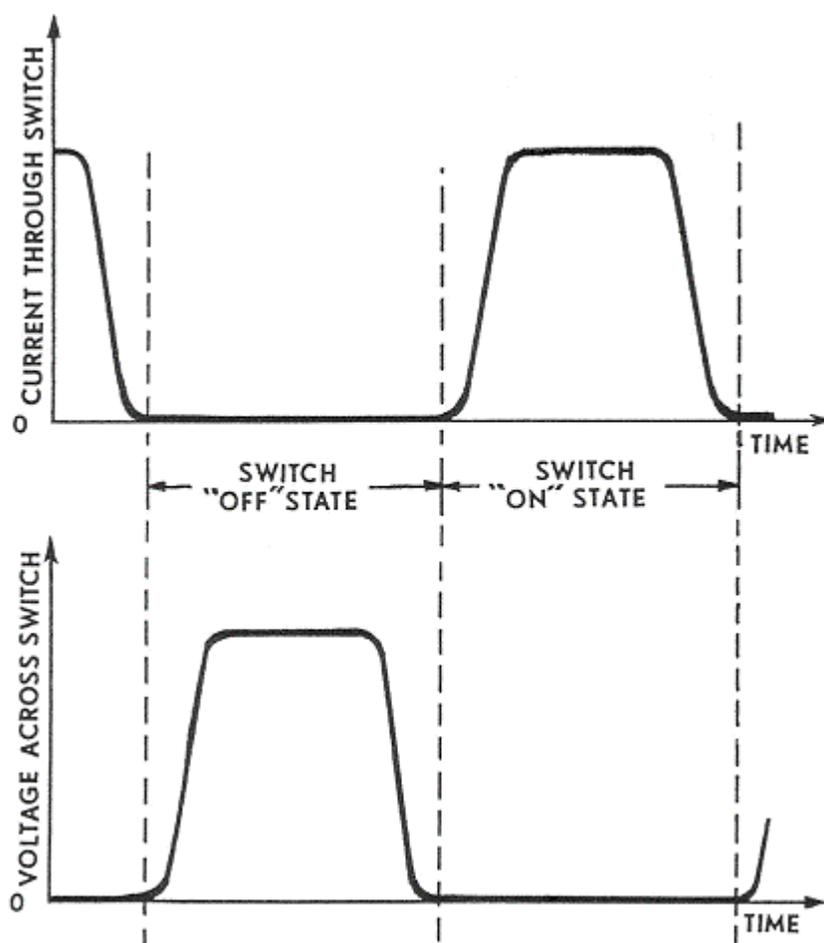


Fig. 1. Conceptual "target" waveforms of transistor voltage and current.

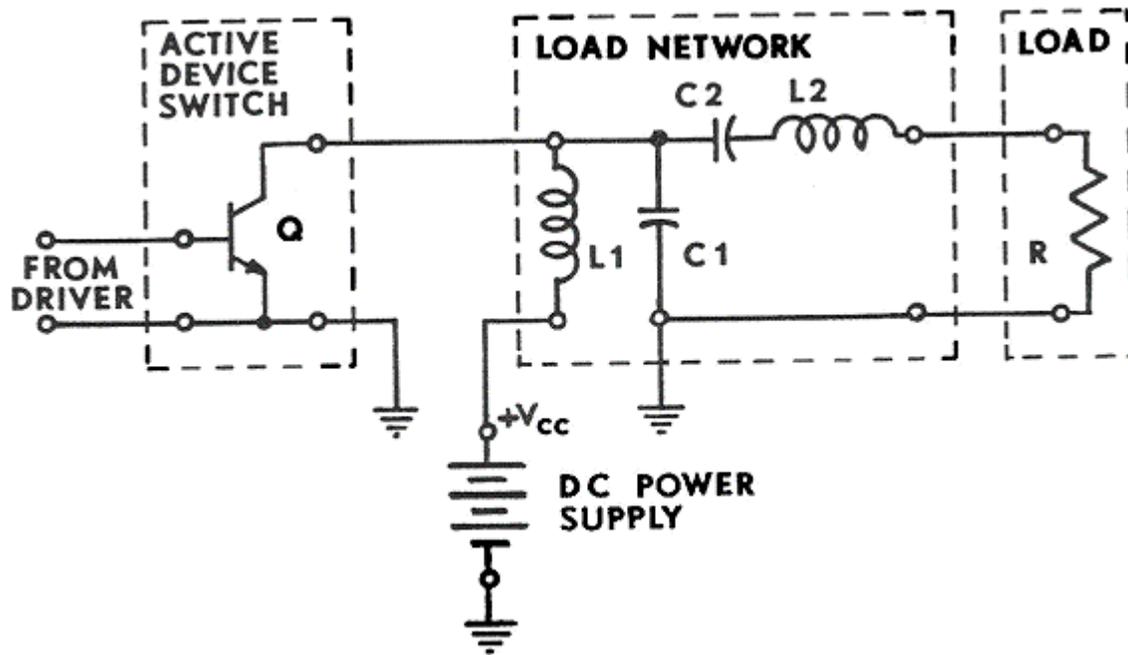


Fig. 2. Schematic of low-order Class-E amplifier.

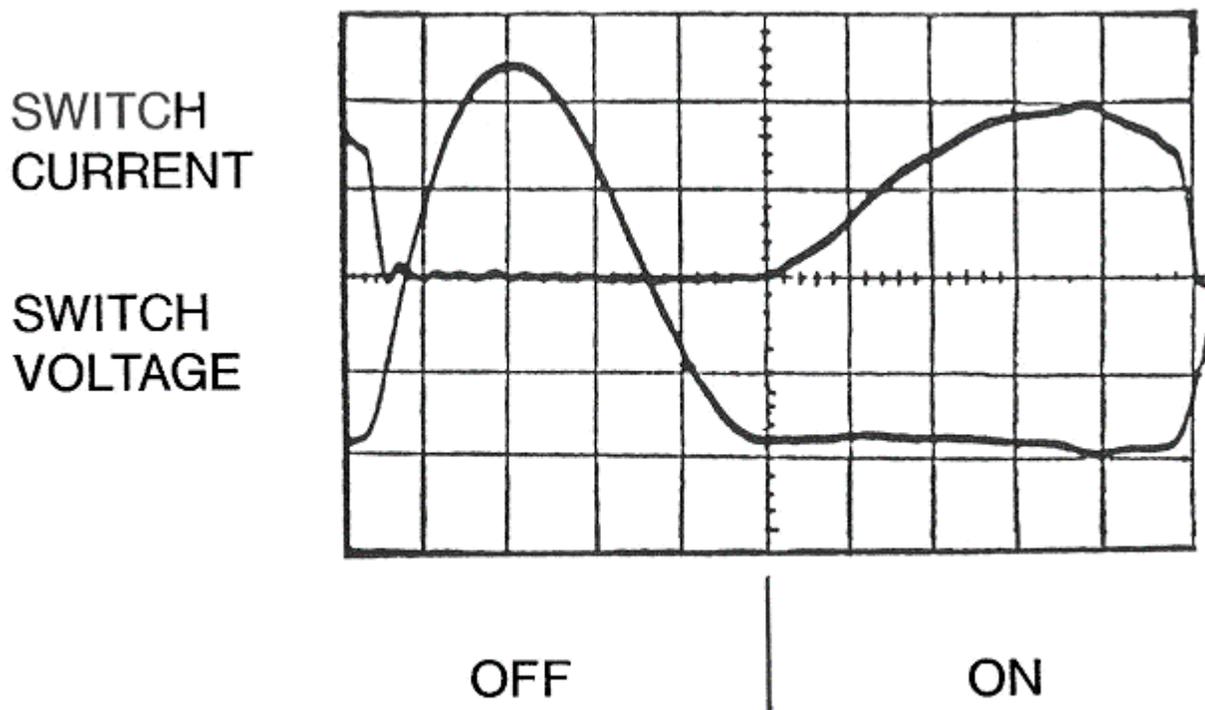


Fig. 3. Transistor voltage and current waveforms in low-order Class-E amplifier.

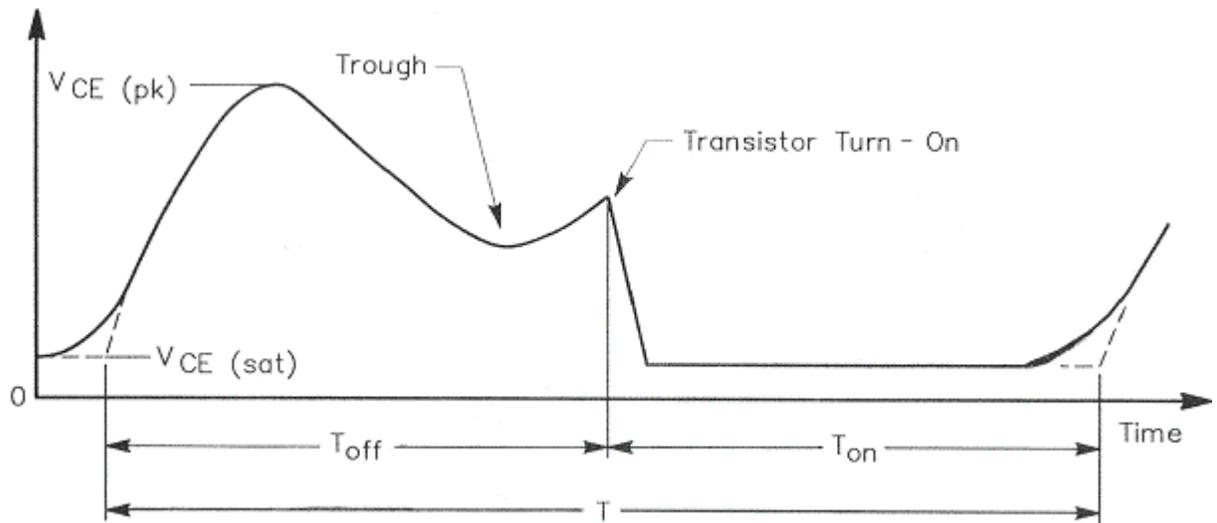


Fig. 4. Typical off-nominal transistor-voltage waveform, showing transistor turn-off, turn-on at nonzero voltage and nonzero slope, and waveform “trough.”

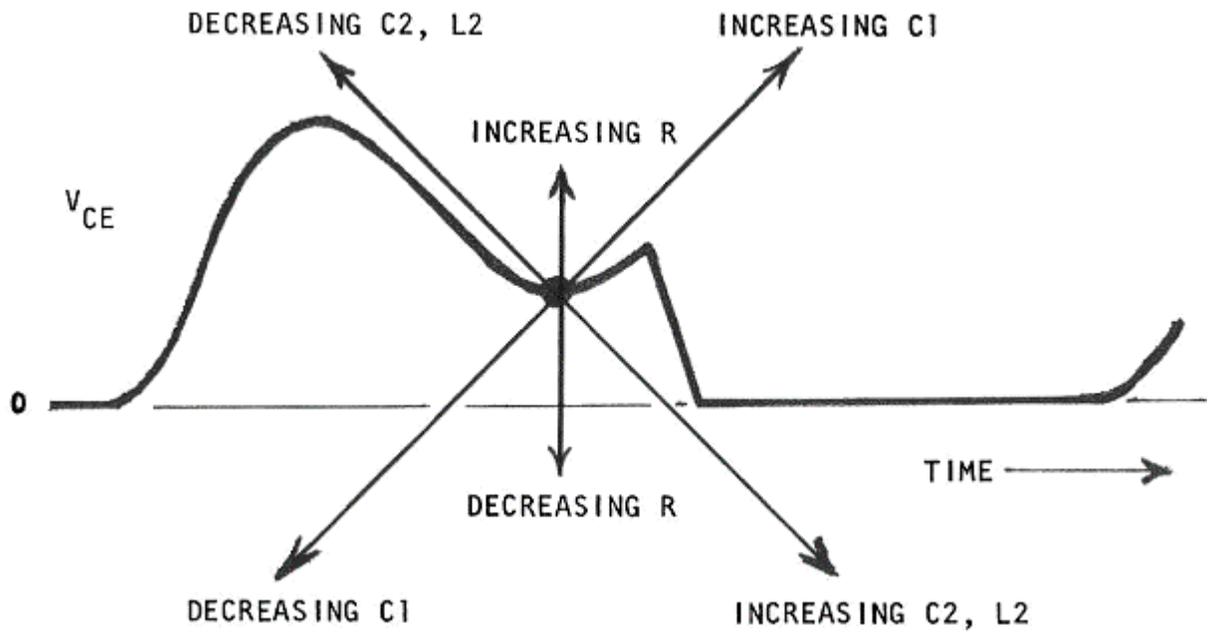


Fig. 5. Effects of adjusting load-network component values.

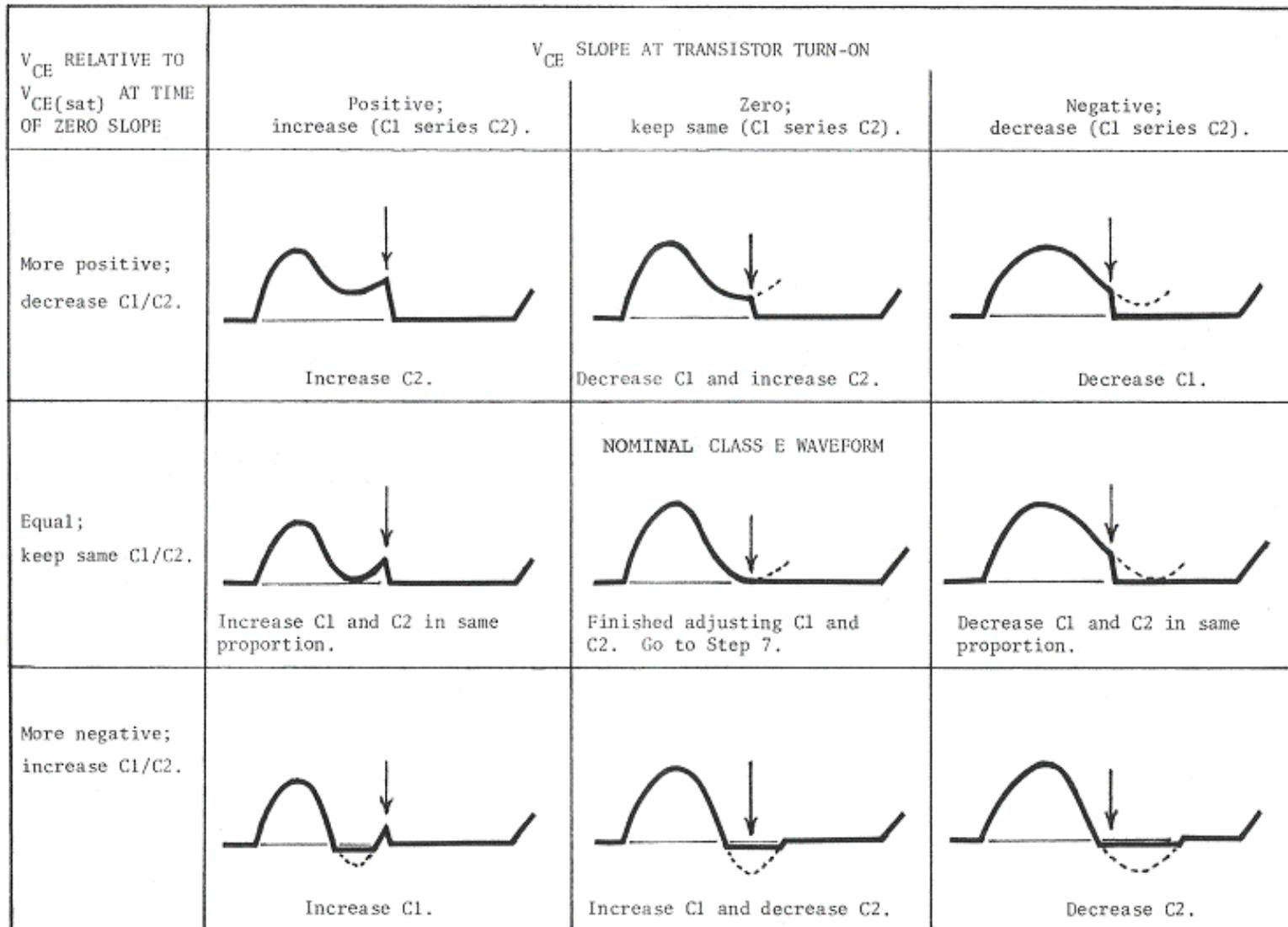


Fig. 6. C1 and C2 adjustment procedure. The vertical arrow indicates the time of transistor turn-on.