A Merged Process for Thick Single-Crystal Si Resonators and BiCMOS Circuitry

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Abstract— **A simple process has been developed which combines thick single-crystal Si micromechanical devices with a bipolar complimentary metal–oxide–semiconductor (BiCMOS) integrated circuit process. This merged process allows the integration of Si mechanical resonators as thick as 11 μm with any integrated circuit process with the addition of only a single masking step. The process does not require the use of Si on insulator wafers or any type of wafer bonding. The Si resonators were etched in an inductively coupled plasma source which allowed deep trenches to be fabricated with high aspect ratios and smooth sidewall surfaces. Clamped-clamped beam Si resonators that were 500 μm long, 5 μm wide, and 11 μm thick have been fabricated and tested. A typical resonator had a resonance frequency of 28.9 kHz and a maximum amplitude of vibration at resonance of 4.6 μm in air. The average measured resonance frequency across a 4-in-diameter Si wafer was within 0.5% of that predicted by theory. Working NMOS transistors were fabricated and tested on the same chip as the resonator with measured threshold voltages of 0.6 V and an output conductance of 2.0$\times$10^{-5} Ω^{-1} for a gate voltage of 4 V. [420]**

Index Terms— **CMOS, deep etching, etch-diffusion, frontside-release, MEMS, silicon resonator.**

I. Introduction

THE advantages of using single-crystal Si as a mechanical material have long been recognized [1]. Its strength and high intrinsic quality factor make it attractive for micromechanical resonant devices. It is readily available as an integrated circuit (IC) substrate and can be processed using methods developed by the IC industry. Thick Si devices also can have advantages over thinner ones for many applications. When capacitive transduction is used to drive or sense motion in a micromechanical device, large capacitive plates with small gaps between them are desired to increase capacitance so that high sensitivity can be achieved. For laterally resonant devices, this translates into a thick structure. Thick structures can also be advantageous for inertial sensing applications where large masses are required to respond to small inertial forces.

One of the obstacles in the production of single-crystal Si micromechanical devices has been the ability to integrate electrical circuitry with the micromechanics using a simple fabrication process. Integration of circuitry with micromechanics can provide a number of advantages for many sensing and signal processing applications. Often the output of micromechanical devices is a very small electrical signal. The difficulty in reading out a small output signal can limit the sensitivity or signal to noise ratio in many devices. This signal is usually buffered or amplified so that it can then be processed by the rest of the electronic system. When the signal processing is done on a separate chip from the micromechanics, the signal must travel through bond pads, bond wires, and external packaging structures which have large parasitic capacitances associated with them. This further limits the signal which can be read out. However, if the signal processing circuitry can be included on the same chip as the micromechanical structure, smaller signals can be amplified and conditioned, and even converted to digital signals so that when they are passed off chip, they are not degraded significantly by off chip parasitics.

A number of technologies have been developed which integrate micromechanics and electrical circuitry. Many use surface micromachined polycrystalline Si micromechanical elements due to this material's availability, often used as transistor gates, in electrical circuitry [2]–[5]. The use of thin polycrystalline Si layers provides flexibility in geometry, transducer axis selection, anchoring, and number of structural layers. However, the use of polycrystalline Si brings with it some limitations in design. Polycrystalline Si is typically deposited at relatively high temperatures. As such, when it cools down to room temperature, stress gradients developed in the film due to mismatches in thermal expansion coefficient can cause a released micromechanical device to bend. Therefore, deposition conditions must be carefully selected and monitored in order to produce a polycrystalline film with low stress. Also, film thicknesses are typically limited to a few micrometers due to the long deposition times. However, recent work has demonstrated that thick polycrystalline Si films can be grown in acceptable times with useful properties [6].

There are various processes used to fabricate single-crystal Si micromechanical devices but most are difficult to integrate with circuit processes, or expensive Si on insulator (SOI) starting wafers are required [7]–[12]. There have been a number of successful efforts to integrate single-crystal Si micromechanical structures with circuitry and all have several advantages and drawbacks [13]–[15]. In this work, a merged process has been developed through which single-crystal Si laterally resonant devices have been integrated with BiCMOS circuitry with the addition of only a single masking step. This process has many advantages over other processes including the use of standard (100) Si starting wafers as opposed to

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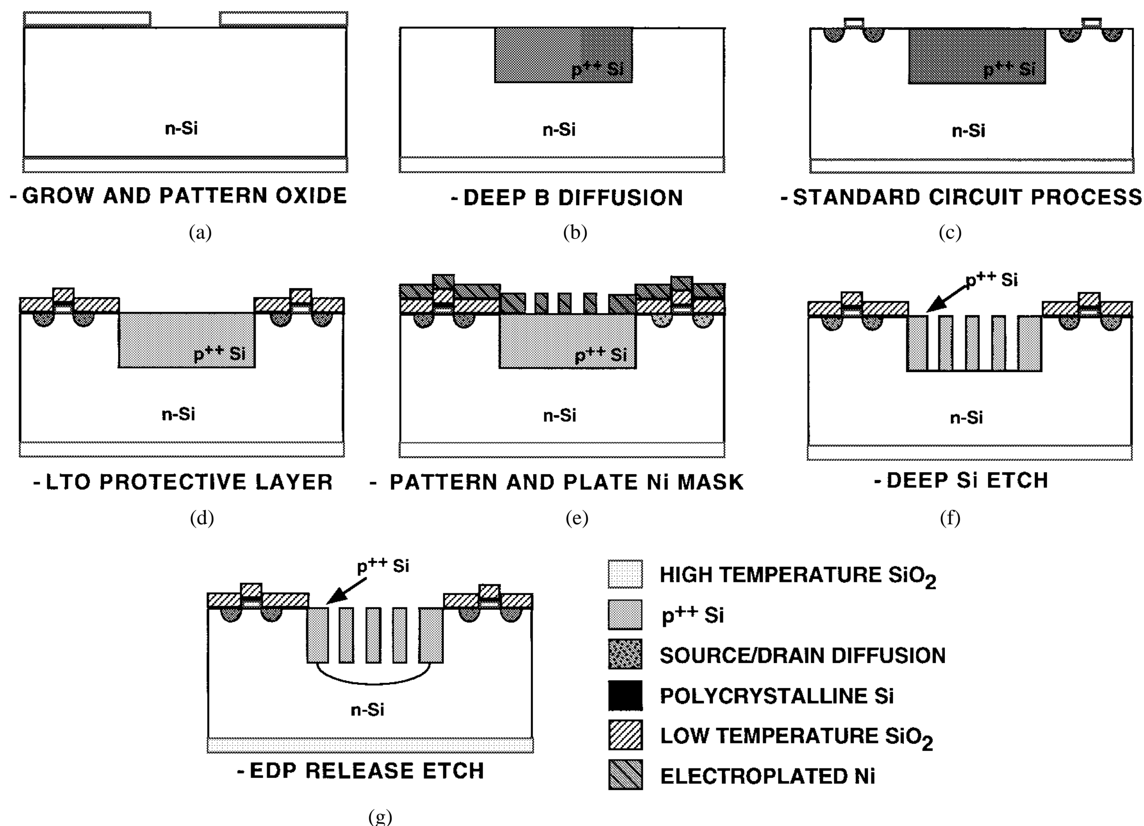


Fig. 1. Schematic of the merged process used to fabricate the thick single-crystal Si resonators and BiCMOS circuitry.

expensive SOI starting wafers. Also, this process requires no wafer bonding, no backside processing or backside alignment of the micromechanical structure, and no electrochemical etch stop for the release etch in ethylenediamine pyrocatechol (EDP).

II. Experiment

Fig. 1 shows a schematic of the process flow used to fabricate the resonators integrated with circuitry. First a thermal oxide is grown on an n-Si wafer to be used as a mask for the subsequent long diffusion [Fig. 1(a)]. The B diffusion is ~11 μm deep and will form the micromechanical structure and serve as an etch stop for the EDP release [Fig. 1(b)]. The diffusion used in this work was the isolation diffusion from the bipolar part of the circuit process. This diffusion can be used as long as the doping concentration is made high enough ($>7 \times 10^{19}$ cm^{-3}) to serve as an etch stop in the EDP release etch but will result in an increased collector-to-substrate capacitance ($C_{\rm CS}$) [16]. If a CMOS circuit process were used or a minimization of $C_{\rm CS}$ is important, a long B diffusion would be added before the beginning of the CMOS circuit process. This diffusion defines the thickness of the structure, which is limited to about 15 μm for practical diffusion times. Next, conventional circuit processing is done [Fig. 1(c)]. Since all that has been done is a diffusion, the starting condition of the wafers for the circuit process is planar. The circuit process used in this work is a BiCMOS process with a 3-μm gate length, two levels of polycrystalline Si, and one metal layer. Although bipolar devices were available and functional, only MOS devices were utilized in the fabricated transimpedance amplifier. Following the circuit fabrication, a 1.2-μm-thick low-temperature oxide (LTO) layer is deposited on top of the circuit for passivation as well as to protect it from the subsequent EDP release etch [Fig. 1(d)]. This layer is patterned and dry etched half way through the LTO layer to partially open the contact pads. These pads will be completely opened using a blanket dry etch at the end of the process. Following the LTO layer, a 25/5 nm Ti/Ni plating base is evaporated over the entire wafer. A 2.8-μm-thick photoresist is then patterned on top of the plating base which will serve as a plating mold. Next 2 μm of Ni is electroplated through the mold and the mold is then removed. The plated Ni serves as a dry etch mask for the deep Si etch which follows [Fig. 1(e)]. The dry etch is done in an inductively coupled plasma (ICP) source with 250-W source power and 70-W stage power at 5 mTorr with 20 sccm of Cl_2 flow and a source to sample distance of 6 cm [17]. This dry etch must go completely through the B layer so that separate B doped elements are formed. There is no danger of dry etch induced damage to the circuit, because during the deep dry etch, there are many layers protecting the circuit, such as the Ni mask and the LTO layer beneath it. The Ni mask is then removed in boiling HCl [Fig. 1(f)].

The samples are then etched in EDP for about 20 min in order to undercut the B doped structures and release the micromechanical devices [Fig. 1(g)] [18]. The EDP solution selectively etches the lightly doped Si and electrical contact to the wafer is not needed during the wet etch. Also, since

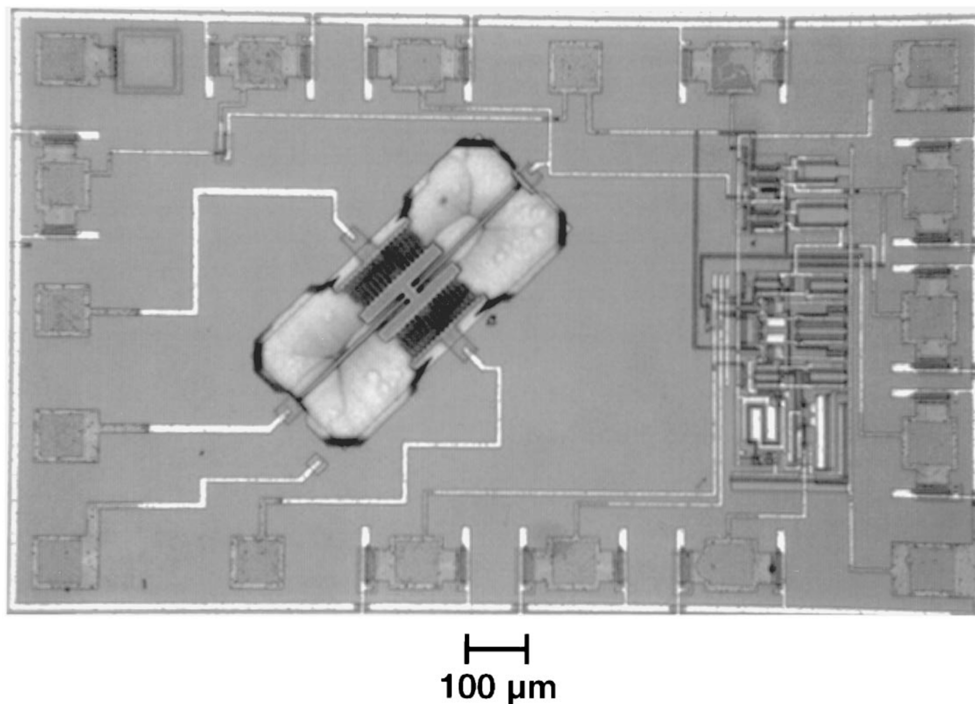


Fig. 2. Photograph of the die containing an 11-μm-thick Si resonator and a CMOS transimpedance amplifier.

the circuitry is protected from the EDP solution by the LTO, no special fixtures or waxes are required to hold the wafers during etching. Although an EDP release etch was used in these experiments, any Si etchant which is selective to heavy B doping can be used [19]. Release of the structure can be achieved by etching of Si with alkali hydroxide etchants such as KOH. KOH is easier to handle than EDP but contains alkali ions which can be detrimental to MOS transistors. Quaternary ammonium compounds which are free of alkali ions have also be used to etch Si with good etch characteristics. A B etch stop has been reported in a tetramethyl ammonium hydroxide (TMAH) solution and an etch ratio of 1:40 has been achieved between heavily and lightly B doped Si [20]. Using the above process, clamped-clamped beam resonators were fabricated with on chip transimpedance amplifiers. The devices were resonated and their resonance characteristics were measured both optically and electrically.

III. Results and Discussion

A. Process Integration

Fig. 2 shows a die photo of the resonator integrated with the transimpedance amplifier. There are two important points to note about the order of steps in this merged fabrication process. Thermal concerns are often a limiting factor when micromechanics are to be integrated with circuitry. In other processes with polycrystalline Si micromechanical structures, deposition and annealing temperatures of polycrystalline Si are typically higher than conventional Al metallization can withstand. Therefore, processing of mechanical polycrystalline Si layers must be done before the Al metallization steps. In the process developed in this work, the B diffusion used to form the micromechanical structure here is a long high-temperature step and therefore must be done before Al interconnects are formed on the wafer. Also, if the transistor junctions are already formed, this diffusion would diffuse them much further, which would ruin the transistors. Therefore, it is advantageous to perform the long B diffusion before any circuit processing has been done. Another concern when integrating micromechanics and circuitry is topography. Micromechanical structures often have large steps compared to circuit features and these steps can be hard to conformally protect with thin films. In the process presented here, the deep dry etch forms deep trenches in the Si wafer. It is difficult to obtain uniform photoresist coatings in deep trenches and even if adequate films are obtained, complete removal of the photoresist from the high aspect ratio trenches is difficult. Unless the trenches are somehow filled or encapsulated and planarized, the circuit processing would be difficult with these large steps. Therefore, the dry etch is done after the circuit processing. The two limitations of the high-temperature B diffusion and the deep trenches determine that the circuit processing should be done after the diffusion and before the deep dry etch to keep the merged process simple.

The resonator on the left side of the die shown in Fig. 2 was rotated at a 45° angle relative to the manhattanized circuit layout. The reason for this rotation is to shorten the EDP release etch. If the resonator was not rotated, the etch rate of Si in EDP would slow down at the (111) planes and then proceed to undercut the resonant elements at a very slow rate. Resonators can still be released without rotation, at the expense of a longer release etch time. However, if the resonators are rotated 45°, the EDP can undercut the resonant elements at a faster rate since the slow etching planes do not run parallel to the resonators. This way, large resonant elements can be undercut in short periods of time. These resonators

were fully released with only a 10 min EDP etch. On the right side of Fig. 2 is the transimpedance amplifier and on the periphery of the chip are electrostatic discharge protected bond pads for outside electrical connection to the circuit and micromechanical structure.

The gap between the released Si resonator and the substrate can be arbitrarily varied by changing the EDP release etch time. In most cases, a large gap between the resonator and substrate is desirable. The voltage difference between the moveable resonator and the substrate can cause static displacement of the resonator which can affect device operation. A large gap decreases the coupling of energy between the substrate under the resonator and the resonator itself. For surface micromachined devices operated in air, the quality factor of the resonator is often limited by energy dissipation due to Couette or Stoke's type damping between the structure and the substrate [21]–[23]. This is due to the small gap often created when a thin sacrificial layer is used. Since the gap can be made much larger in this work, the quality factor in air of these devices is probably not limited by Couette or Stoke's type damping beneath the structure, but rather, may be limited by damping in between the thick plates of the comb structure.

B. Si Etching in an Inductively Coupled Cl_2 Plasma

One of the enabling steps in this process is the deep Si etch used to etch through the B doped Si layer and define the micromechanical structure. High-density plasma sources allow high aspect ratio trenches to be etched easily and reliably [24]. The plasma etch system used for dry etching consists of an ICP source and a radio frequency (RF) powered electrode. Power was inductively coupled into the plasma through a four-turn solenoid type copper coil with input power from 0 to 2000 W at 2 MHz. The RF powered stage coupled energy into the plasma at 13.56 MHz with power available from 0 to 500 W. This stage power serves to bias the wafer and accelerate ions to the wafer surface causing anisotropic etching. The RF power or the self induced dc bias ($|V_{\rm dc}|$) on the wafer can be controlled. The ICP source to sample distance was fixed at 6 cm. Gas flows were regulated with mass flow controllers, and the chamber pressure was controlled by a throttled 1500 l/s turbomolecular pump. All dry etching of Si was done at room temperature and no cryogenic cooling of the wafer was necessary.

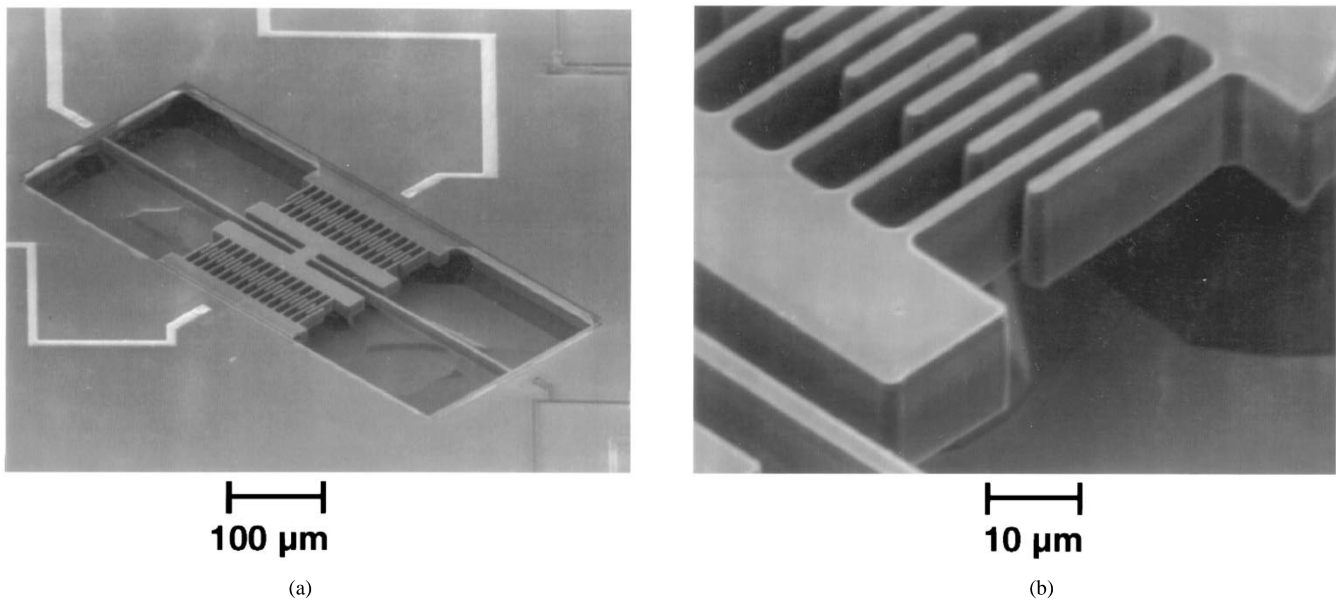
An optimized etch condition was developed in order to etch Si trenches with minimum feature sizes of 1 μm and depths $>$50 μm. A source power of 250 W, stage power of 70 W, and $|V_{\rm dc}|$ of 176 V at 5 mTorr with 20 sccm Cl_2 flow was used. Chlorine etching of Si relies on an ion assisted reaction for etching to proceed. The chlorine etch species will not spontaneously etch Si so that very little undercutting is expected. The etching only proceeds when directional ions bombard a layer of adsorbed $SiCl_x$ species on the surface of the Si. This bombardment provides the energy for the etch products to desorb and for etching to proceed. When Si is etched in a Cl_2 plasma at low pressure, passivation or polymerization of sidewalls is not needed to achieve a vertical etch profile.

A number of high-density plasma systems can be used to etch the thick Si resonators. An ECR source has been used previously to etch deep trenches with high aspect ratios and vertical profiles [25]. In addition, commercially available high-density ICP systems have been optimized to etch deep trenches in Si [26]–[28]. Most of these processes rely on cycling between etching with fluorine containing plasmas and depositing or coating sidewalls with polymers. High selectivity to a SiO_2 or photoresist mask was achieved. The use of passivation of sidewalls can limit the etching of narrow trenches. For narrow trenches, sidewall coatings can plug the trenches, preventing etching, and making the process hard to control. Also, processes which rely on passivation of sidewalls typically are performed at higher pressures ($>$10 mTorr). This makes microloading or aspect ratio dependant etching effects worse, due to the difficulty in transporting etch species and products in and out of high aspect ratio trenches. On the other hand, the metal mask used in this work adds one additional masking step to the circuit process, but it allows high aspect ratio resonant elements to be formed with small gaps, vertical profiles, smooth sidewalls, and minimal microloading effects. If a photoresist or SiO_2 mask could be used, the merged process can be further simplified since the circuit passivation mask could be used to define the micromechanical structure and no additional masking steps other than the circuit steps are required.

C. Resonator Characteristics

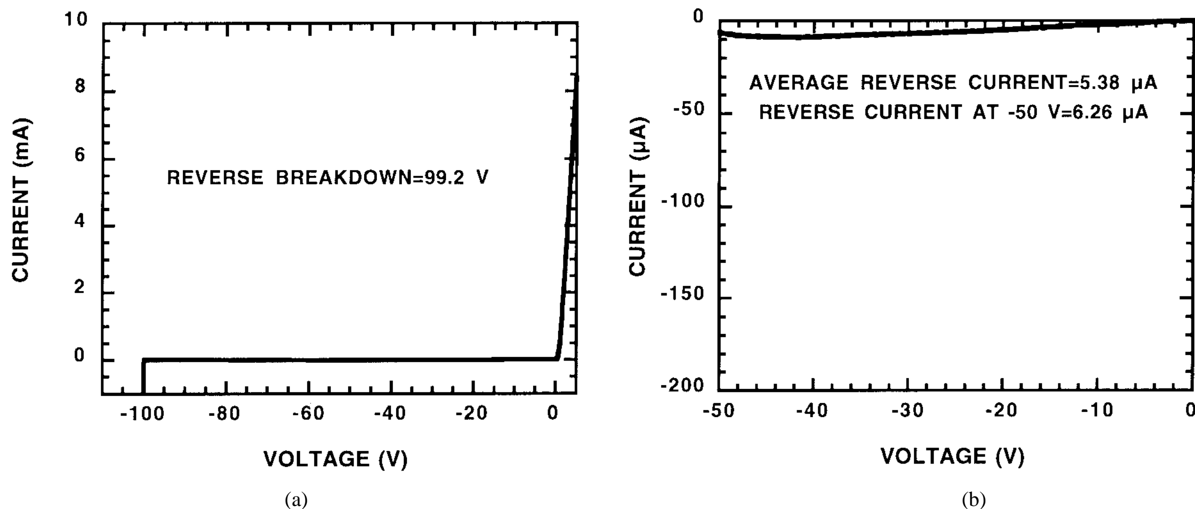
A clamped-clamped beam micromechanical resonator was fabricated using this merged process as shown in Fig. 3(a). The beam is 500 μm long, 5 μm wide, and 11 μm thick. Motion is driven and sensed using capacitive-comb transducers with 3-μm-wide fingers and 3-μm-wide gaps. The resonant elements are released from the substrate by etching in EDP and the Al metal lines connecting the resonator to the circuit can also be seen. A close-up of the resonator is shown in Fig. 3(b). The high aspect ratio achievable by dry etching can be seen between the comb fingers. Also, a very smooth surface is obtained on all sidewalls. The deep Si etching in a Cl_2 plasma provides a very smooth surface and the EDP etch further smoothes the surface of the B doped Si [29].

The Si resonant elements must be isolated from the substrate so that potentials can be applied between the different micromechanical elements. This is another major challenge in the integration of single-crystal Si structures on a conventional Si substrate. In this work, p-n diode isolation is used so that current will not flow from the resonator into the substrate [30]–[32]. The diode is formed between the heavily doped p^{++} micromechanical structure and the lightly doped n^- substrate. As long as this diode is kept reverse biased, only leakage currents will flow to the substrate and large voltages can be placed across the micromechanical structure. The diode characteristics are shown in Fig. 4 for the resonator integrated with circuitry on the die shown in Fig. 2. There are a few very important parameters of this diode which affect the performance of the device. The reverse breakdown voltage limits the magnitude of the dc voltage which can be placed



(a) (b)

Fig. 3. Micrographs of (a) 11-μm-thick, 500-μm-long, 5-μm-wide clamped-clamped beam resonator with metal lines contacting the resonator to the circuitry and (b) close-up of the electrostatic comb drive showing the high aspect ratio gaps between fingers etched in the inductively coupled plasma source.



(a) (b)

Fig. 4. Characteristics of the diode formed between the heavily B doped resonator and the lightly doped substrate. (a) Forward and reverse characteristic showing a breakdown voltage of −99.2 V and (b) average reverse current of 5.38 μA.

across the drive and sense ports of the resonator. Fig. 4(a) shows that the diode breaks down at −99.2 V, which is typical of the diodes fabricated with this process. This allows large dc biases to be placed across the drive and sense ports of the resonator.

Another important diode parameter is the reverse leakage current. While the diodes are reverse biased, a dc leakage current will flow across the junction. This is undesirable and will consume power, so low reverse currents are required. Fig. 4(b) shows that the reverse current for these diodes is 6.26 μA at a −50-V dc bias with an associated power consumption of $\sim$300 μW. One last consideration is the junction capacitance inherent in a p-n junction diode. This capacitance may limit high-frequency performance of the resonators. However, since the devices are strongly reverse biased with large negative voltages and the doping in the lightly doped substrate is low, the depletion region should be large and junction capacitance should be relatively low. The capacitance of the junction isolating a typical resonator anchor was calculated to be 2.82 fF. Since the junctions are exposed on the surface of the devices, this may lead to undesirable characteristics such as leakage currents across the exposed junction as well as instability, low reproducibility, and added breakdown mechanisms. These junctions can be passivated easily by growing a thin oxide on the structure or using one of the many thin films being investigated for passivation of micromechanical structures [31].

Although we have used p-n junction isolation in this work, this merged process is not limited to this isolation scheme. The use of the junction isolation provides excellent anchoring of the resonator through a continuous single-crystal Si substrate. That is, there is no interface between dissimilar materials other

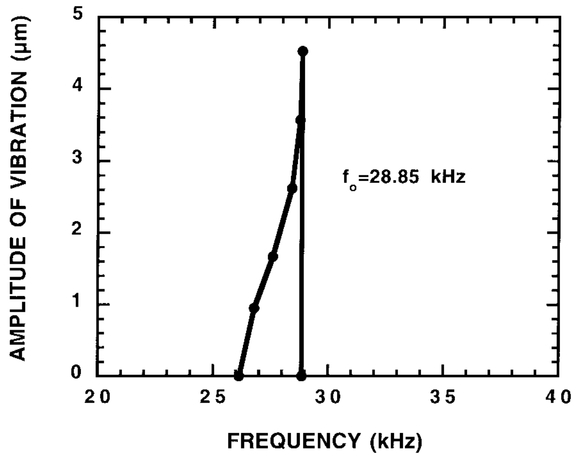


Fig. 5. Resonance characteristics of the resonator from Fig. 2 measured optically in air with a 50 V dc bias and a 10 $V_{p\text{-}p}$ ac excitation.

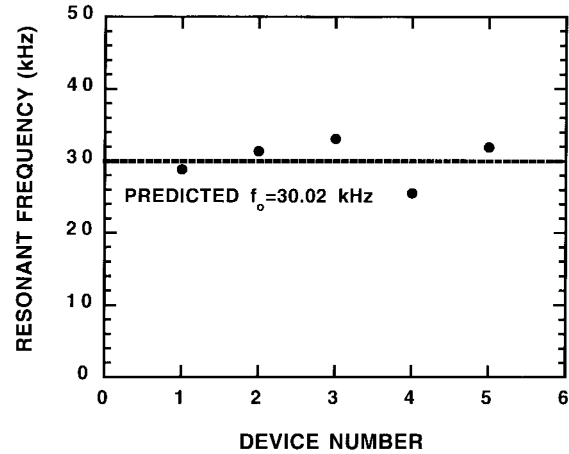


Fig. 6. Proximity of measured resonance frequency to that predicted by conventional beam theory for five different samples.

than B doped Si and lightly P doped Si which may decrease temperature sensitivity of the resonant structure. However, the drawbacks of junction isolation as mentioned above may make other isolation methods more desirable for certain applications, such as high-frequency micromechanical resonators for signal processing. In this case, a single masking step can be added to the merged process to obtain dielectric isolation. A trench can be etched in the Si at the beginning of the process and refilled with a dielectric [33], [34]. This would isolate the resonator from the substrate as well as provide mechanical anchoring of the resonator to the substrate.

The resonance characteristics of the resonators have been measured both optically and electrically. Fig. 5 shows the resonance characteristics of the clamped-clamped beam resonator measured optically in air. A dc bias of 50 V was placed across the comb drive and an ac excitation of 10 $V_{p\text{-}p}$ was used to drive the structure into resonance. The resonance frequency was 28.85 kHz and the maximum amplitude of vibration at resonance was 4.6 μm. The ac signal was scanned from low to high frequencies for these measurements. The vibration amplitude drops off quickly after resonance because the resonator was overdriven. A large amplitude of vibration was desired in order to measure the vibration with minimal errors. Therefore, the highest driving voltages possible without pull-in were used. The resonance characteristics were also measured electrically using an HP4195 network analyzer. Since the output signal was measured as a current, low driving voltages could be used. A 25-V dc bias and a 1.26-$V_{p\text{-}p}$ ac voltage were used to drive the resonator. A symmetric resonance curve was measured when the driving voltages were reduced and the vibration amplitude was measured electrically with the network analyzer.

A number of devices were measured in order to determine the reproducibility of the process. The resonance frequency of five typical resonators is shown in Fig. 6 and compared to a theoretical calculation. A predicted resonance frequency of 30.02 kHz was calculated from the geometry of the resonator and material constants

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k}{m}} \tag{1}$$

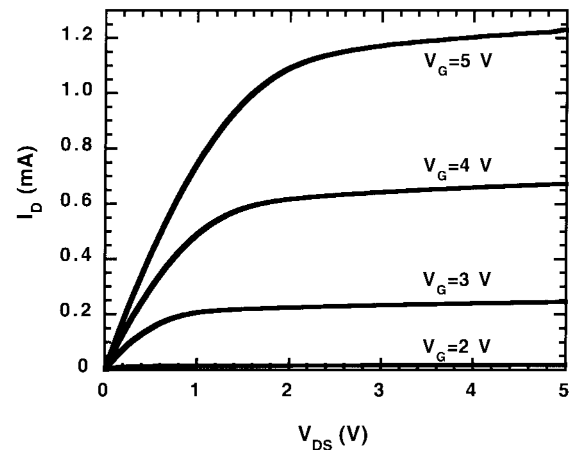


Fig. 7. I–V curve for an NMOS transistor measured after all micromechanical processing. The threshold voltage was 0.6 V and the transistors had a V_A of 40.8 V.

where k is the spring constant and m is the mass of the resonator. A Young's modulus of 150 GPa and a Si density of 2330 kg/m^3 was assumed. The mass of the resonator based on the designed device dimensions was 4.31×10^{-10} kg. All the measured devices had resonance frequencies close to that predicted by the calculations. The average resonance frequency across a 4-in-diameter Si wafer was within 0.5% of the predicted frequency. This indicates that the dimensions of the resonators can be tightly controlled and are uniform across a 4" wafer.

D. Integrated Circuit Performance

The performance of the circuitry was measured after all processing was finished in order to determine if the processing of the micromechanical structure had any effect on circuit performance. A current-voltage (I–V) curve measured using an HP4145 semiconductor parameter analyzer for an n-channel metal–oxide–semiconductor (NMOS) transistor is shown in Fig. 7. The transistor had a threshold voltage of 0.6 V, a channel length modulation parameter (λ) of 0.0245 V^{-1} and $\mu_n C_{\rm ox}$ was measured to be 89.3 μA/V^2. The output conductance of the transistor was 2.0×10^{-5} Ω^{-1} for a gate voltage

of 4 V. The p-channel metal–oxide–semiconductor (PMOS) devices had a threshold voltage of -0.8 V and $\mu_p C_{\rm ox}$ was measured to be 17.9 μA/V^2. The threshold voltage did not shift following the micromechanical structural processing. Bipolar devices were measured to be functional as well. The processing of the resonator should not affect the circuitry because there are no high-temperature steps after circuit fabrication. In addition, the circuit is protected from all subsequent processing by an LTO layer.

The transimpedance amplifier was designed to detect the output motional current of the resonator, where the current is converted into an output voltage via multiplication with a shunt-shunt feedback MOS resistor. To insure good performance of the detection circuitry, the main amplifier block is comprised of the frequently used simple five-transistor operational amplifier with a feedback resistor [35]. The robustness and stability of the detection circuitry is enhanced by using a biasing scheme which allows the user to manually set the dc bias values at various nodes of the circuit [36]. In order to minimize power consumption, the transistors in the amplifier block were designed to operate in the subthreshold regime with a bias tail current of < 250 nA. Matching problems of transistors in the subthreshold regime are alleviated by designing transistors with large dimensions so that uniform transistor characteristics can be easily obtained. For a 0- to 5-V rail-to-rail supply and a bias current of 250 nA, the power dissipated by the amplifier was calculated to be $\sim$1.25 μW. The simulated 3-dB frequency of the amplifier was 150 kHz.

IV. CONCLUSION

A simple process has been developed which integrates single-crystal Si resonators as thick as 11 μm with BiCMOS circuitry. The processing of the micromechanical structure adds only one additional masking step to the baseline circuit process. If SiO_2 or photoresist is used as the etch mask for the micromechanical structure instead of the Ni etch mask, the merged process can be further simplified so that no additional masking steps are required. Micromechanical devices have been fabricated with a 500-μm-long, 5-μm-wide, 11-μm-thick single-crystal Si clamped-clamped beam resonator and a CMOS transimpedance amplifier on the same chip. A deep Si etch in a Cl_2 plasma generated in an ICP source has been optimized so that high aspect ratio comb gaps can be fabricated with smooth sidewalls. A resonance frequency of 28.85 kHz and a maximum amplitude of vibration of 4.6 μm at resonance was measured in air both optically and electrically using a network analyzer. A number of devices were tested and their resonance frequencies were uniform and close to that predicted by simple theory. Circuit characteristics of CMOS transistors were measured and the processing of the micromechanical resonator had no deleterious effects on the devices.

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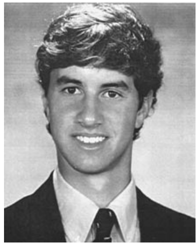

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