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A 78-Microwatt GSM Phase Noise-Compliant Pierce Oscillator Referenced to a 61-MHz Wine-Glass Disk Resonator

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***Abstract*— A 61-MHz Pierce oscillator referenced to a single polysilicon surface-micromachined wine-glass disk resonator has achieved phase noise marks of -119dBc/Hz at a 1-kHz offset and -139dBc/Hz at far-from-carrier offsets. When divided down to GSM's 13MHz, this corresponds to -132dBc/Hz at 1-kHz and -152dBc/Hz at far-from-carrier offsets, both of which satisfy GSM reference oscillator phase noise requirements. This Pierce oscillator achieves such performance using a single disk, not an array, while only consuming 78 microwatts of power, a reduction by a factor of ~4.5 compared with previous work. When power consumption is considered, this performance marks the best figure of merit at 1-kHz carrier offset among published on-chip oscillators to date. Such low phase noise and power consumption posted by a tiny MEMS device may soon become key enablers for low power "set-and-forget" autonomous sensor networks with substantial communication capability.**

Keywords*— *MEMS, oscillator, micromechanical, wine-glass disk, low phase noise, low power, resonator, RF MEMS.

I. Introduction

Reference oscillators based on high-Q MEMS resonators have recently become viable alternatives to traditional quartz versions. With resonator Q's exceeding 100,000, such oscillators have posted impressive phase noise performance, even achieving marks that meet the challenging GSM specification using a mechanically-coupled resonator array-composites occupying only 0.1mm^2 of area and consuming only 350μW of power [1]. While such devices offer compelling savings in power and space compared to quartz for cell phone applications, further reductions in these attributes are still desired for future autonomous wireless sensor networks [2], where nodes would be expected to operate and communicate for long periods without the luxury of replacing their power sources.

Pursuant to further reducing power and area consumption, this work introduces a 61-MHz Pierce oscillator referenced to a single polysilicon wine-glass disk resonator, cf. Fig. 1, reducing die area from 0.1mm^2 to 0.01mm^2, a factor of 10, compared with previous arrayed devices. Furthermore, even with this size reduction, the low noise figure of the improved amplifier design used here yields an oscillator with no degradation in phase noise performance even while total power consumption is lowered drastically. This Pierce oscillator design achieves measured marks of -119dBc/Hz at 1-kHz offset and -139dBc/Hz at far-from-carrier offsets, both of which satisfy GSM specifications

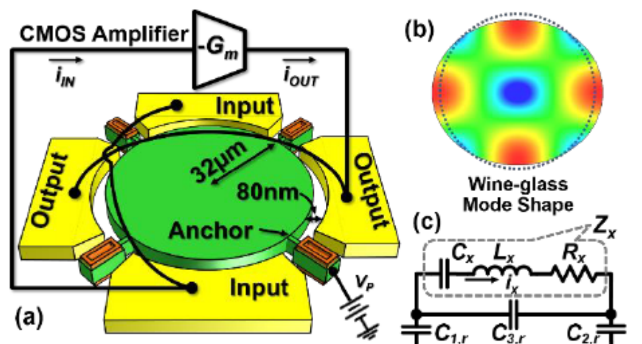

Fig. 1. Perspective-view schematic of (a) a micromechanical wine-glass disk resonator combined with a sustaining transconductance amplifier to form a Pierce oscillator, (b) resonator mode shape, and (c) equivalent electrical circuit.

(i.e., divided down to GSM's 13MHz, these correspond to -132 dBc/Hz at 1-kHz and -152dBc/Hz at far-from-carrier offsets) while consuming only 78μW power.

II. Resonator Operation and Modelling

The wine-glass disk resonator used in this work, depicted in Fig. 1(a), comprises a 3μm-thick, 32μm-radius polysilicon disk supported at quasi nodal points by four beams and surrounded by electrodes spaced only 80nm from its edges. To excite the resonator into motion, a bias voltage V_P is applied to the disk and an ac drive voltage to the input electrode. These voltages combine to produce a force across the input electrode-to-resonator gap that at resonance can excite the wine-glass (i.e., compound (2, 1)) mode shape, shown in Fig. 1(b), which comprises expansion and contraction of the disk along orthogonal axes. The frequency of resonance is defined [3]

$$f_{nom} = \frac{K}{R}\sqrt{\frac{E}{\rho(2+2\sigma)}} \quad (1)$$

where R is the disk radius, $K = 0.373$ for polysilicon structural material, and E, σ, and ρ are the Young's modulus, Poisson ratio, and density of the structural material, respectively.

In the electrical domain, the resonator behaves as the equivalent LCR tank shown in Fig. 1(c), where $C_{1,r}$, $C_{2,r}$, and $C_{3,r}$ are intrinsic and parasitic capacitors seen at the input and output nodes of the resonator. The dc-biased (V_P) vibrating electrode-

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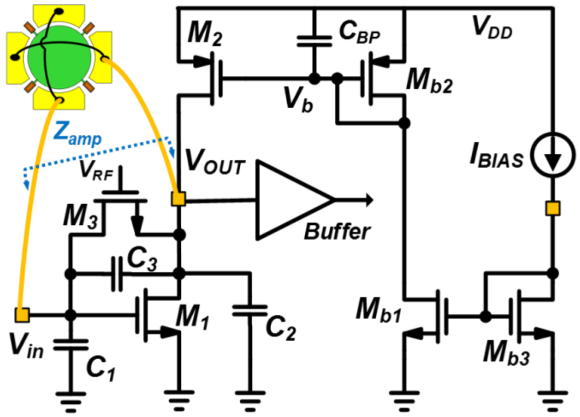

Fig. 2. Schematic of the CMOS amplifier used in the Pierce oscillator, including bias network and parasitic capacitance at input and output nodes.

to-resonator capacitors generate motional currents at each electrode proportional to the disk velocity. If the electrodes are placed as shown in Fig. 1, with the current directions indicated, the input and output currents are in-phase, and current flow can be modeled by a single motional current i_x through the *LCR* tank. The elements R_x, L_x, and C_x link to the mechanical properties of the resonator as follows [4]:

$$R_x = \frac{c_r}{Q\eta^2},\quad L_x = \frac{m_r}{\eta^2},\quad C_x = \frac{\eta^2}{k_r},\quad \eta = V_P\frac{\partial C}{\partial r} \qquad (2)$$

where c_r, m_r, and k_r are the damping, mass, and stiffness of the resonator, respectively, determined via equations given in [5], $\partial C/\partial r$ is the change in resonator-to-electrode capacitance per unit radial displacement.

III. Oscillator Design

As shown in Fig. 2, the Pierce oscillator topology used in this work combines a frequency selective resonator with a single trans-conducting gain device: in this case, the MOS transistor M_1. M_2 serves as a load transistor, while M_3 provides feedback to properly dc-bias transistor M_1. For oscillation to occur, two conditions must hold: 1) the gain around the loop must be larger than unity; and 2) the phase shift around the loop must be zero. Focusing first on the latter, transistor M_1 introduces 180° of phase shift between the input and output voltages. However, at resonance the phase shift across the wine-glass mode disk resonator is 0°, so an additional 180° is needed to satisfy criterion 2. To supply this, the resonator must operate in the inductive region and resonate with C_1, C_2, and C_3, which comprise the total parasitic capacitors from the resonator, the amplifier, and surrounding structures, e.g., bond pads, at the input and output nodes, as shown in Fig. 2.

A. Linear Analysis

At start-up the amplitude of oscillation is small, the whole circuit stays linear, and the impedance looking into the gate and drain of M_1 can be modeled using small signal equivalent circuits, c.f. Fig. 3. Here, impedances Z_1, Z_2, and Z_3 include all resistive and reactive components of devices M_1 (except its transconductance g_{m1}), M_2, and M_3, plus the resonator's parasitic capacitors.

The critical condition for oscillation occurs when Z_{amp} and Z_x sum to zero. For oscillation to start, $|\mathrm{Re}(Z_{amp})|$ must be larger than R_x. However, Z_1-Z_3 constrain the achievable $|\mathrm{Re}(Z_{amp})|$ to a maximum value as depicted by the red curve in Fig. 4, which is the theoretical plot of $|\mathrm{Re}(Z_{amp})|$ versus g_{m1} (bottom *x*-axis) and the required power consumption for V_{DD} of 2V (top *x*-axis). If the real part (resistances) of Z_1-Z_3 are large, then only the capacitors C_1, C_2, and C_3 remain, in which case the maximum value of $|\mathrm{Re}(Z_{amp})|$ becomes [6]:

$$\left|\mathrm{Re}(Z_{amp})\right|_{\max} = \frac{1}{2\omega C_3\left(1 + C_3\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\right)} \qquad (3)$$

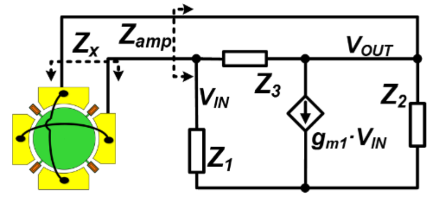

Fig. 3. The small signal equivalent circuits of the oscillator with impedances Z_1, Z_2, and Z_3, which include all the components of the transistors M_1 (except its transconductance g_{m1}), M_2, M_3, and the resonator's parasitic capacitance.

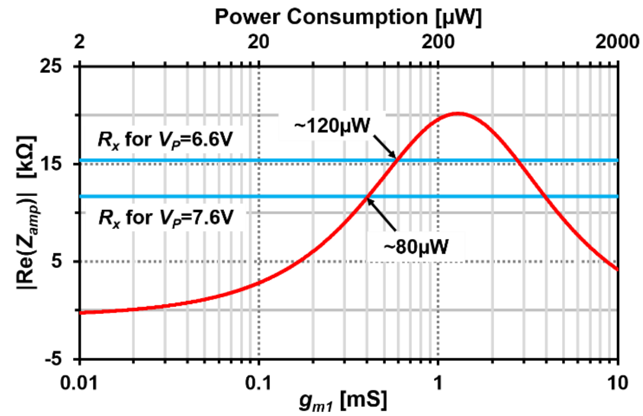

Fig. 4. Theoretical plot of $|\mathrm{Re}(Z_{amp})|$ vs. transconductance, g_{m1}, of the M_1 transistor and the required power consumption to achieve this g_{m1} with V_{DD}=2V. The blue lines correspond to calculated motional resistances of the resonator for different V_P's and indicate theoretical minimum powers required for oscillation.

If this value is smaller than R_x, no oscillation ensues, even if g_{m1} increases. From (3), there are two ways to increase $|\mathrm{Re}(Z_{amp})|_{\max}$: 1) raise the values of C_1 and C_2 at the cost of burning more power; and 2) reduce the input-to-output feedthrough capacitance C_3. The last of these reveals why self-sustained oscillation of a micromechanical resonator is possible using a Pierce circuit, despite its large motional resistance R_x. Indeed, the C_3 of a 61-MHz wine-glass disk resonator is on the order of 40-50fF, many times smaller than the 6pF in a typical 60-MHz quartz crystal, allowing $|\mathrm{Re}(Z_{amp})|_{\max}$ to exceed the disks R_x of 15kΩ. Interestingly, the C_3 of a wine-glass disk resonator is so small, and it allows a $|\mathrm{Re}(Z_{amp})|_{\max}$ greater than 20kΩ without the need to increase C_1 and C_2. In comparison, with C_3 =6pF, a typical quartz crystal cannot muster a $|\mathrm{Re}(Z_{amp})|_{\max}$ more than 118Ω, even with C_1 and C_2 as large as 14pF. Of course, the much smaller R_x =70Ω of a typical 60-MHz quartz crystal does not require that $|\mathrm{Re}(Z_{amp})|_{\max}$ be so large, but the needed C_1 and C_2 values are still on the order of 10pF. Since larger C_1 and C_2 demand higher transistor drive power, a MEMS-based Pierce oscillator circuit with a relatively small C_3 that in turn allows small

C_1 and C_2 should permit much lower power consumption. If the resonator R_x can be further lowered, e.g., by increasing its dc-bias voltage V_P, as illustrated in Fig. 4, the power consumption of a MEMS-based Pierce oscillator should shrink even more. Fig. 4 in fact shows that an increase in V_P by 1V decreases the oscillation power requirement by 33% (from 120μW to 80μW).

Once oscillation starts, the amplitude builds up exponentially from initial thermal noise with a time constant [7]

$$\tau = -\frac{2L_x}{\mathrm{Re}\{Z_{amp}\} + R_x} \qquad (4)$$

The total time required to reach steady-state oscillation depends on the time constant (4), the amount of noise in the system, and the initial energy impulse, the last of which can be tailored by an appropriate switch-on procedure at start-up.

B. *Pierce vs. Transimpedance Amplifier (TIA)*

The TIA used to instigate and sustain oscillation in previous work [1][5] comprised a fully differential CMOS amplifier biased by a common-mode feedback circuit that effectively canceled common-mode noise, especially low-frequency noise caused by vibration [8]. The Pierce oscillator presented here, however, with its single-ended Pierce topology, sacrifices this common-mode feedback to achieve lower noise-figure, hence lower phase noise, than previous TIA-based oscillators. This is made possible by 1) using only two active transistors compared to a minimum of four in the TIA; 2) using a very large shunt-shunt feedback MOS resistor, M_3, for biasing compared to the much smaller gain-setting resistor required by the TIA, where the larger the resistance, the smaller the current noise; and 3) using C_{BP}, at the cost of some area increase, between the gate of M_2 and V_{DD}, as shown in Fig. 2, to filter noise from bias transistors M_{b1}-M_{b3} and from V_{DD}. Per the last item, recall that the TIA of [5] relied on common-mode feedback to reject bias-derived noise, but note that the efficacy of this approach is only as good as the matching of its transistors.

Finally, the smaller transistor stack of the Pierce oscillator circuit allows it to operate at lower V_{DD}, hence lower power, without driving the two transistors into their triode regions.

IV. Experimental Verification

The wine-glass disk resonators used for testing were fabricated via a previously described three-polysilicon self-aligned stem small lateral-gap process [9]. Fig. 5 presents the scanning electron micrograph (SEM) of a fabricated 61-MHz wine-glass disk resonator along with a typical measured frequency response, where Q's of 130,000 in vacuum and motional impedances of 14kΩ with V_P=7V were common among devices.

The amplifier IC was fabricated in a 0.35μm CMOS technology. Although the entire die, shown in Fig. 6(a), occupies an area of 900μm×500μm, the actual sustaining amplifier with its biasing circuits only consumes about 60μm×45μm while the 44pF C_{BP} occupies about 200μm×100μm. The attenuation of noise at node V_b in Fig. 2—52dB in this case—depends on the pole, $g_{m,b2}/C_{BP}$, where $g_{m,b2}$ is the transconductance of diode-connected transistor M_{b2} in Fig. 2 and $1/g_{m,b2}$ is the resistance looking into M_{b2}. Therefore, for the same attenuation, the area of C_{BP}

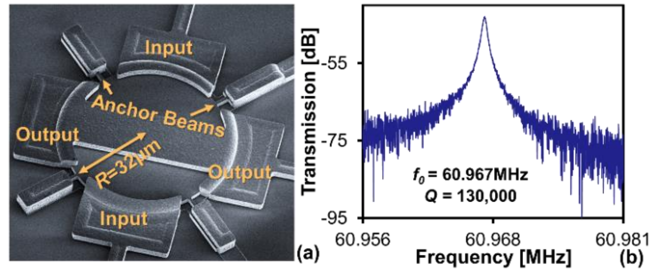

Fig. 5. (a) SEM of a fabricated wine-glass disk resonator and (b) the measured frequency response of the resonator used in this work.

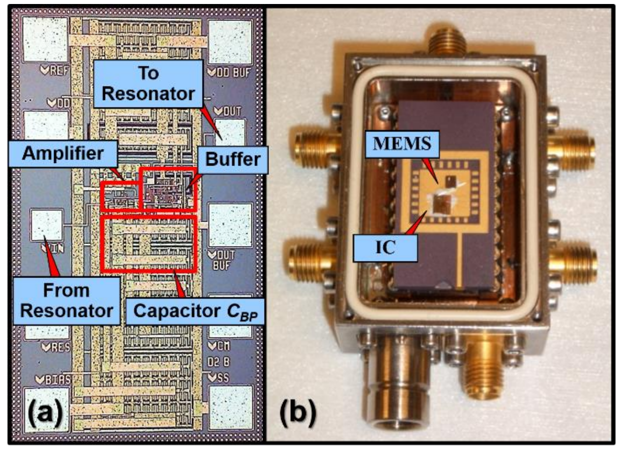

Fig. 6. (a) Die photo of custom-made IC. (b) Photo of the packaged oscillator in a custom-designed vacuum box.

can be reduced easily by 2 to 4 times by simply decreasing $g_{m,b2}$. The rest of the IC area is consumed by 1) an on-chip buffer used to drive 50-Ω measurement systems; 2) by-pass capacitors that further reduce noise on DC supply lines that would normally be distributed among other on-chip integrated circuits; and 3) multiple bond pads.

The amplifier die was bond-wired to the resonator and package, as shown in Fig. 6(b), to yield the oscillator under test. To maintain high (i.e., over 50,000) resonator Q, and thereby minimize phase noise [10], the MEMS-based oscillator must operate in a stable vacuum environment, provided via the custom-made miniature vacuum chamber, depicted in Fig. 6(b), that encloses a printed circuit board (PCB) board housing the MEMS/CMOS device package and provides electrical feed-throughs to allow connection to outside instrumentation. Power and bias voltages for the oscillator were provided by a custom low-noise analog supply board. The output of the oscillator was measured using an Agilent E5500 phase noise test setup configured to use a low-noise PLL.

When biased with sufficient V_P to provide positive loop gain, the inset of Fig. 7 shows the output waveform of the packaged MEMS oscillator operating in vacuum. Fig. 7 additionally presents measured phase noise data for the Pierce oscillator alongside data for a TIA oscillator employing the same MEMS resonator design. Here, the Pierce oscillator achieves -119dBc/Hz at 1-kHz offset and -139dBc/Hz at far-from-carrier offsets from its 61-MHz oscillation frequency. When divided down to GSM's 13MHz, this corresponds to -132dBc/Hz at 1-kHz and -152 dBc/Hz far-from-carrier, both of which satisfy GSM reference

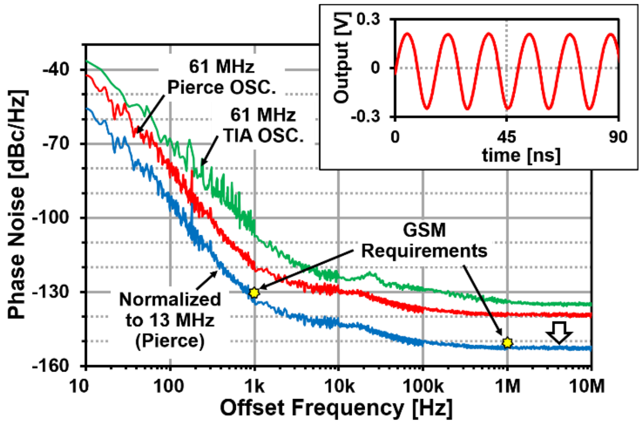

Fig. 7. Measured phase noise of 61-MHz oscillators comparing the new Pierce topology and an older TIA topology similar to [5], as well as the Pierce oscillator phase noise divided down to 13MHz for comparison to the GSM spec. Inset: the measured output waveform of the Pierce oscillator.

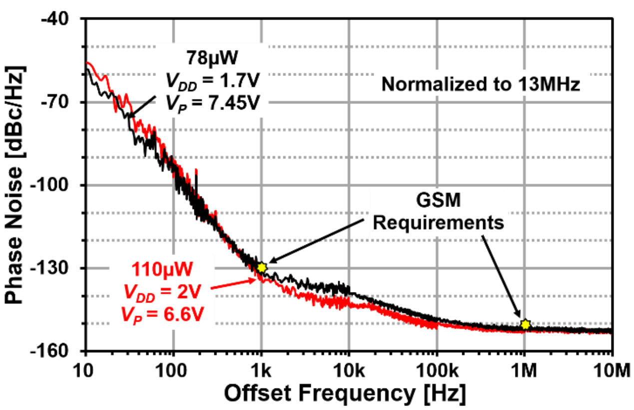

Fig. 8. Measured phase noise of the oscillator operating at two V_{DD} values. A reduction in V_{DD} and I_{BIAS} can be seen to decrease power consumption by 29% with only a modest decrease in phase noise performance.

oscillator phase noise requirements. This Pierce oscillator not only provides phase noise improvements of 9dB at 1-kHz offset and 7dB far-from carrier versus the TIA version of [5] using a similar single disk; it also reduces power consumption down to 78µW, which is ~4.5 times smaller.

Fig. 8 presents phase noise measurements for the Pierce oscillator that investigate the degree to which increases in resonator dc-bias V_P allow lower supply voltages, hence, lower power consumption. Here, a 0.85V increase in V_P allows V_{DD} and I_{BIAS} reductions that decrease overall power consumption from 110µW to 78µW, with very little degradation of phase noise.

For fair comparison of this work to other oscillators, a figure of merit (*FOM*) that accounts for the total power consumption required to achieve a given phase noise can be used:

$$FOM = 10\log\left(\mathcal{L}(\Delta f).\frac{P_{diss}}{1mW}\cdot\left(\frac{\Delta f}{f_0}\right)^2\right) \qquad (5)$$

where $\mathcal{L}(\Delta f)$ is the oscillator phase-noise at Δf offset frequency and P_{diss} is its total power consumption. Use of (5) yields Table I, where the present Pierce oscillator achieves the best *FOM* at 1kHz amongst any published on-chip oscillator to date.

TABLE I. PERFORMANCE COMPARISON

Device Type	**This work**	Wine-Glass array [1]	AlN [11]	FBAR [12]	Quartz [13]
f_{OSC} [MHz]	**61**	61	4.9	2000	10
Power [µW]	**78**	350	120	22	~1500
Normalized (13MHz) Phase Noise @ 1 kHz [dBc/Hz]	**-132**	-136	-130	-122	-135
FOM@1kHz [dB]	**-225**	-223	-221	-220	-211

V. CONCLUSIONS

The demonstration by this work of a 61-MHz capacitive-gap transduced wine-glass disk Pierce oscillator capable of meeting GSM specifications while using only 78µW of power marks a milestone for MEMS-based frequency control technology. Compared with previous TIA-based renditions, this oscillator reduces power and area consumption by 4.5 times and 10 times, respectively, and, to best of the author's knowledge, now posts the highest *FOM* of any published on-chip oscillator to date. That the small port-to-port feedthrough capacitance of the MEMS resonator is largely responsible for the *FOM* improvement is quite intriguing and suggestive of design approaches that might lead to further *FOM* increases. Whether or not such increases are achieved, the power reduction already achieved by the demonstrated oscillator while maintaining GSM-compliant phase noise performance already makes a very compelling case for application to future autonomous wireless sensor networks.

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