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A High-Q Tunable Micromechanical Capacitor With Movable Dielectric for RF Applications

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ABSTRACT

A high-Q, tunable, micromechanical capacitor has been realized using an IC-compatible, electroplated-metal, surface-micromachining technology and demonstrated with quality (Q-) factors in excess of 290—the highest reported to date for on-chip tunable capacitors at frequencies near 1 GHz. The key feature in this design that makes possible such high on-chip Q is the method for capacitive tuning, which in this design is based on moving the dielectric between the capacitor plates, rather than moving the plates themselves, as done in previous designs. One version of this design achieves a measured Q of 291 at 1 GHz (C=1.21pF) with a tuning range of 7.7% over 10V of control voltage, and an expected self-resonant frequency (SRF) of 19GHz. In another design, with a wider tuning range of 40% over 10V, a Q of 218 is achieved at 1 GHz (C=1.14pF).

I. INTRODUCTION

Micromechanical tunable capacitors constructed using MEMS technology have previously been demonstrated with Q's on the order of 60—a value that greatly exceeds those achievable by semiconductor diode counterparts fabricated via conventional IC technology [1-3]. Such micromechanical capacitors often consist of suspended top metal plates that can be electrostatically displaced (via applied voltages) over bottom metal plates to vary the capacitance between the plates. Because these capacitors can be constructed in low resistivity metal materials, they exhibit much larger Q's than their semiconductor diode counterparts, which suffer from greater losses due to excessive semiconductor series resistance. To date, micromechanical capacitors have been successfully applied towards the implementation of on-chip, high-Q LC tanks for use in low-phase noise, communications-grade voltage-controlled oscillators (VCO's) [3].

Recent advances in micromechanical tunable capacitor technology, however, are beginning to extend the application range of such devices beyond the initial focus on LC tanks for VCO's, towards the new challenge of tunable pre-select filters for multi-band reconfigurable wireless communication handsets. For this application, much higher Q's are required, on the order of 200 or more. Despite the use of metal in their construction, the Q of micromechanical capacitors to date is still limited by losses arising from the finite resistivity of their metal suspension beams, which often must be made long to attain stiffness values low enough to insure sufficiently low actuation voltages [2]. In effect, traditional micromechanical capacitor designs clearly exhibit a Q versus actuation voltage trade-off.

This work breaks the above trade-off by eliminating the need for lengthy top plate suspension beams. Specifically, rather than implement tunability using a movable top plate, the top plate is made stationary, and the dielectric between the metal plates is made movable. In effect, capacitive tuning is attained via a tunable-dielectric, realized via a movable dielectric plate suspended by dielectric beams that do not impact the Q of the device, and hence, allow Q's of up to 290 for this design.

II. TUNABLE-DIELECTRIC CAPACITOR STRUCTURE AND OPERATION

Figure 1 presents conceptual and perspective-view schematics of the new tunable capacitor design, identifying key components and specifying a preferred actuation voltage configuration. As shown, the structure features a bottom capacitor plate fixed to the substrate, and a top capacitor plate suspended above the former, but rigidly anchored to the substrate, and unable to move. Both plates are constructed of copper (Cu) to minimize their total series resistance, and thus maximize the device Q. A dielectric slab is suspended between the two plates and anchored to the substrate outside the two plates via spring structures. This dielectric is free to move, and can be electrostatically displaced to alter either the overlap between it and the capacitor plates, or the fringing fields between them. In the former case, when a DC bias is applied between the two plates, the charges on the capacitor plates exert an electrostatic force on the induced charges in the dielectric to pull the dielectric into the gap, as shown in Fig. 1(a). The waffle shape

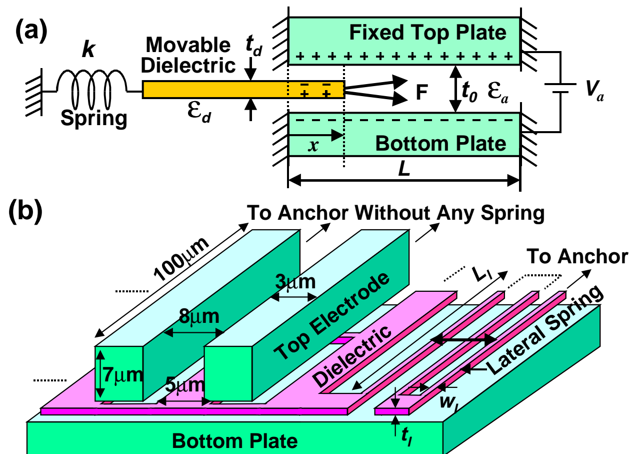

Figure 1. Micromachined tunable capacitor. (a) Conceptual schematic. (b) Actual structure designed with a lateral spring.

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of the structure shown in Fig. 1(b) (also in Fig. 5) is designed to minimize the travel distance (or the needed voltage) required for a given change in capacitance, and to provide etchant access paths during a sacrificial-layer etching step in the fabrication process.

Via use of a movable dielectric rather than a movable top capacitor plate (as done in previous designs [1,2]), the tunable micromechanical capacitor of this work benefits from the following key advantages: (1) Unlike its predecessors, the top capacitor plate in this design need no longer be suspended by lengthy springs that can add series resistance, and thus, lower the Q. Instead, a very thick top plate can be used without any suspension to lower series resistance and greatly increase the Q. (2) As governed by Eq. (1) of the next section, the tuning range in this design is set by the ratio of the dielectric thickness to the capacitive plate gap, and can be made quite large via proper design, without concern for pull-down phenomena that often limit previous movable-top-plate designs [1]. (3) No top-to-bottom plate electrical shortage can happen in this movable dielectric design.

III. TUNABLE-DIELECTRIC CAPACITOR DESIGN

Via appropriate electrostatic analyses, approximate analytical expressions for capacitance C as a function of displacement x and actuation voltage V_a for the tunable capacitor of Fig. 1 can be derived and summarized as follows:

$$C = \frac{\varepsilon_a L}{t_0} + \left[\frac{\varepsilon_a \varepsilon_d}{(\varepsilon_a - \varepsilon_d) t_d + \varepsilon_d t_0} - \frac{\varepsilon_a}{t_0} \right] x$$

$$= \frac{\varepsilon_a}{t_0} \left(L + \frac{a}{1-a} x \right) \quad (\text{if } \varepsilon_d >> \varepsilon_a ,\ a = \frac{t_d}{t_0}) \qquad (1)$$

$$\therefore \frac{C_{\max}(x = L)}{C_{\min}(x = 0)} \approx \frac{1}{1-a}, \text{ but } \frac{\varepsilon_d}{\varepsilon_a} \text{ at best}$$

If substitute $x_{eq} = \dfrac{\varepsilon_a a V_a^2}{2kt_0(1-a)}$ into Eq. (1),

$$C = \frac{\varepsilon_a}{t_0} \left[L + \frac{\varepsilon_a a^2}{2kt_0 (1-a)^2} V_a^2 \right] \qquad (2)$$

where ε_a and ε_d are dielectric constants of air and the dielectric, respectively, t_0 is the gap between two capacitor plates, t_d is the dielectric thickness, L is the length of the plate, k is the spring constant of the suspensions, and x_{eq} is the equilibrium position of the dielectric when the actuation voltage V_a is applied. The lateral stiffness of the single serpentine suspension k_l is given by

$$k_l = \left(\frac{w_l}{L_l} \right)^3 \times t_l E \times \frac{1}{3} \qquad (3)$$

where E is Young's modulus of the dielectric material and other variables are indicated in Fig. 1(b).

Although sufficient for first order design, the above equations do not account for fringing field capacitance, which can contribute significantly to the total capacitance change, especially in structures as complex as that of Fig. 1(b). Thus, the semiconductor device simulator MEDICI was used to fine tune capacitance versus voltage transfer functions for the tunable capacitors of this work. Figures 2 and 3 summarize typical capacitance vs. overlap/voltage design simulations for a device using a dielectric suspension with a spring constant of 0.187N/m.

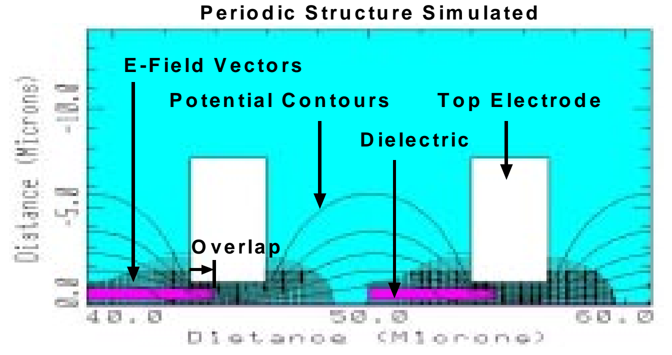

Figure 2. Electrostatic simulation result performed by MEDICI.

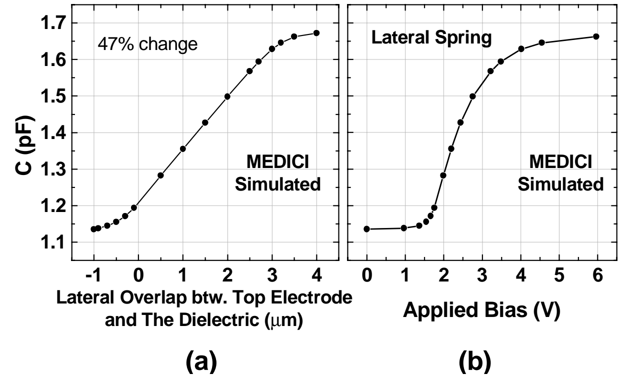

Figure 3. Capacitance change simulation by MEDICI with respect to (a) lateral overlap between top electrode and the dielectric (b) applied bias.

IV. FABRICATION

Figure 4 illustrates the fabrication process used for this work. The process begins with the thermal growth of 1μm of SiO_2 to serve as an isolation layer between eventual metal structures and the silicon substrate. Next, the bottom capacitor plate is formed by first evaporating 300Å/2000Å of a Cr/Cu seed layer, then electroplating 5 μm of copper (Cu) (for which the sheet resistance = 4.2mΩ/sq.). 3000Å of nickel (Ni) is then electroplated above the Cu (c.f., Fig. 4(a)) to serve as a buffer layer to prevent Cu contamination of etch chambers during subsequent RIE processes. Next, a 2000Å aluminum (Al) sacrificial layer is evaporated and patterned to form vias through which a subsequent PECVD nitride dielectric film adheres to the underlying Ni. The nitride film is patterned via RIE to form the movable dielectric plate (c.f., Fig. 4(b)), then submerged under 0.9μm of a second sacrificial Al film that defines the spacing between the dielectric plate and the eventual top metal plate. Due to the valley-like topography between the fingers of the etched dielectric, the deposition of 0.9μm of Al actually results in only a 0.3μm gap between the top plate and the dielectric when the two are engaged. After etching vias through the Al to define top plate anchors (c.f., Fig. 4(c)), the top plate is formed by first evaporating a thin Cr/Cu seed layer, then electroplating Cu through a defining photoresist mold to a thickness of 7μm—thick enough to insure that the top plate does not bend under applied actuation voltages. Finally, the two Al sacrificial layers are selectively etched to release the dielectric structure using a

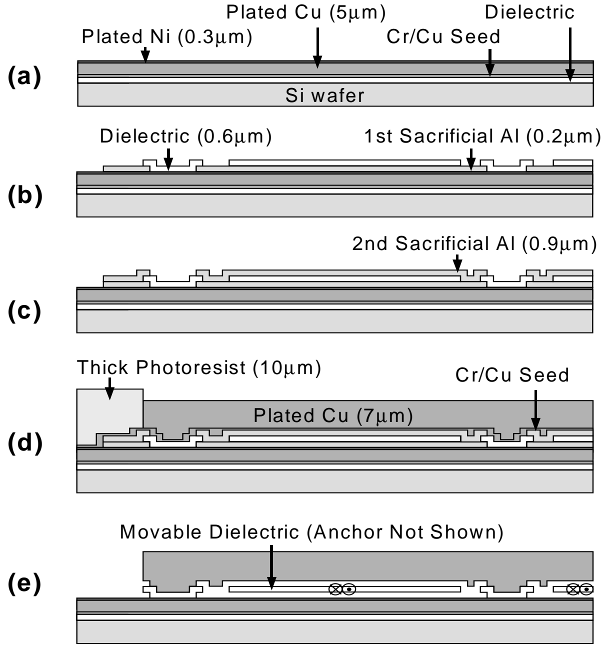

Figure 4. Simplified fabrication process.

$K_3Fe(CN)_6$/NaOH solution, which attacks Al, but leaves Cu and the nitride dielectric intact, yielding the final cross-section of Fig. 4(e). After release, a critical point dryer is often used to dry the structure to prevent stiction [4]. Since all of the process steps in this flow are done at ≤ 200°C, this process should be amenable to post-IC integration with transistor circuits.

Figure 5 presents the SEM for a fabricated device using a lateral serpentine support spring. Here, warping of the structure and its supports is clearly visible, indicating problems with dielectric film stress. Although portions of the dielectric were found to actually touch the top or bottom electrodes, creating undue friction forces that hinder lateral movements, voltage-induced movement of the dielectric was still observable under a microscope.

V. RESULTS AND DISCUSSION

To characterize device performance, RF measurements from 0.6 to 6GHz were made using an HP8753ES s-parameter network analyzer together with GSG-tipped Cascade Microtech microwave probes. Figures 6 and 7 present measured and modeled data summarizing the RF performance for the serpentine-spring device of Fig. 5, showing a very high Q of 291 at 1GHz (1.21pF), with a tuning bias of 0V. Using the circuit model of Fig. 6 to extend its reactance plot, the expected SRF for this device is 19GHz.

Figure 8 plots the tuning range of the fabricated device, which is smaller than expected by theory when assuming lateral motion of the dielectric (i.e., motion parallel to the substrate). At first, the smaller tuning range was attributed to frictional dragging caused by the aforementioned film stress problem. However, closer inspection of partial devices with flat dielectric plates (deposited under more optimal PECVD conditions) revealed that due to a design oversight, vertical motion, rather than lateral, was actually easier to induce. In particular, the widths of the serpentine suspension beams ended up larger than their thicknesses due to stress-based PECVD limitations, making the vertical spring constant of a

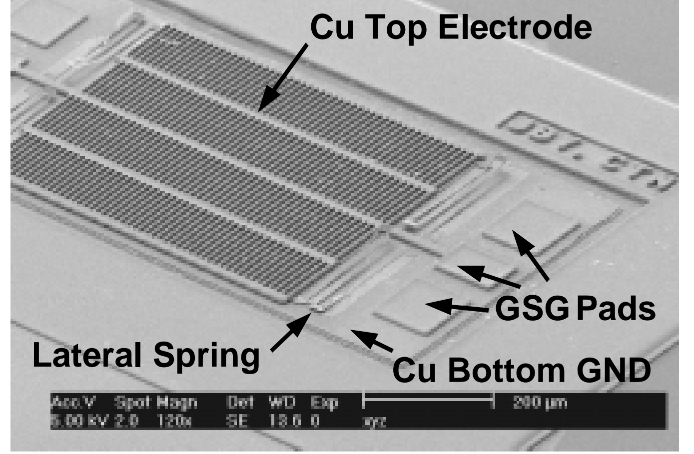

Figure 5. SEM photomicrograph of the fabricated device with a lateral spring.

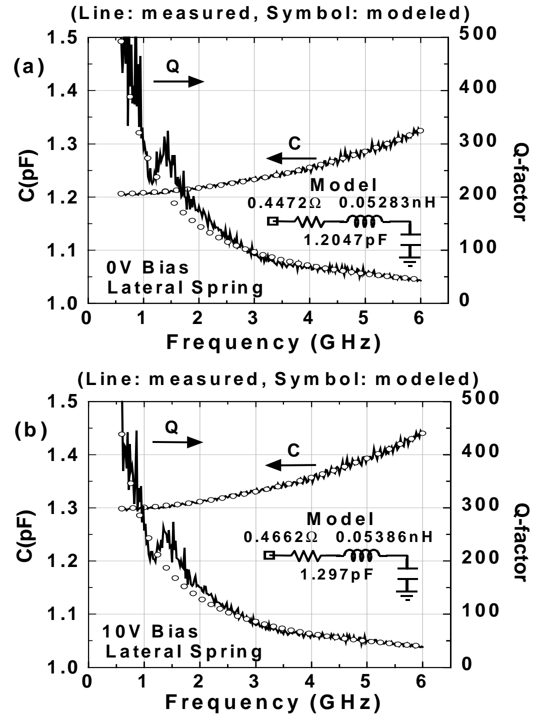

Figure 6. Measured and circuit-modeled RF characteristics of the fabricated device with a lateral spring (a) 0V bias (b) 10V bias.

single serpentine suspension k_v, given by

$$k_v = \left(\frac{t_l}{L_l}\right)^3 \times w_l E \times \frac{1}{3} \qquad (4)$$

more than 10 times smaller than its lateral spring constant. This, combined with the finite vertical electrostatic force that arises upon application of the actuation voltage V_a due to the asymmetrical dielectric-to-metal gaps above and below the dielectric plate (shown in Fig. 4(e)), makes vertical motion more likely than lateral. Future designs are planned to correct this.

In the meantime, although lateral motion was originally desired, Fig. 8 shows that vertical motion still offers a respectable amount of capacitance change due to fringing fields between the asymmetrical metal-to-dielectric gaps. The layout for the tunable capacitor fabrication run actually included devices specifically designed to move vertically, relying on only fringing fields to realize capaci-

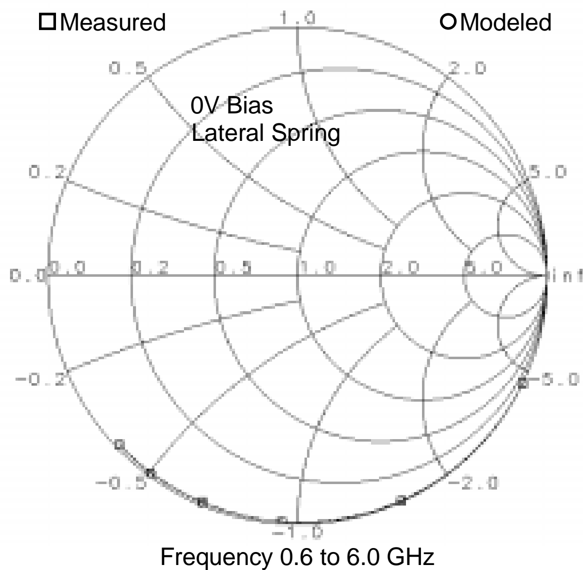

Figure 7. Smith chart showing measured and predicted S_{11} parameters of the fabricated device with a lateral spring (0V bias).

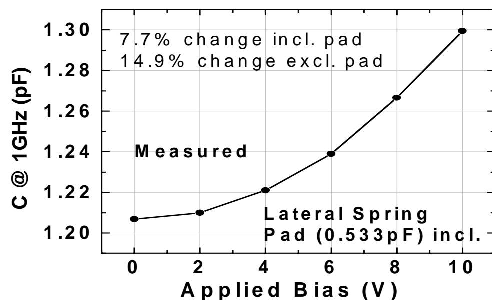

Figure 8. Measured capacitance versus actuation voltage of the fabricated device with a lateral spring.

tance changes. Figure 9 shows the device structure, SEM, and measured RF performance for this vertically-designed device. In the design stage, this device was not expected to perform as well as the lateral version. However, this device actually benefited from film stress, so was able to achieve a much wider tuning range, approaching 40%, with a quality factor of 218 at 1 GHz.

VI. CONCLUSIONS

Micromechanical capacitors utilizing an alternative design featuring a movable dielectric plate between stationary metal plates have been demonstrated with *Q*'s exceeding 290—the highest to date for any on-chip, tunable capacitor. When combined with on-chip (or off-chip) high-*Q* inductors [5], these tunable capacitors are expected to be useful for not only low-phase noise integrated VCO applications, but also for tunable, low-loss, RF filters and tunable matching networks, both key functions capable of enhancing the multi-band programmability of wireless communication handsets.

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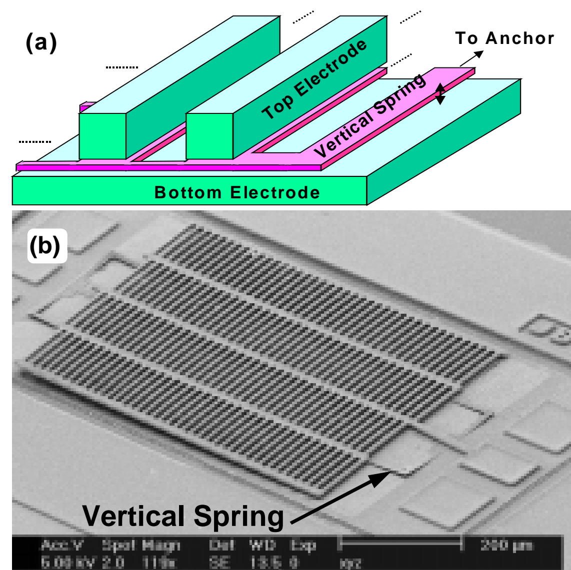

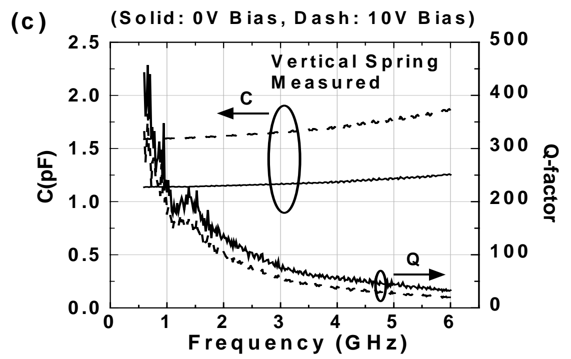

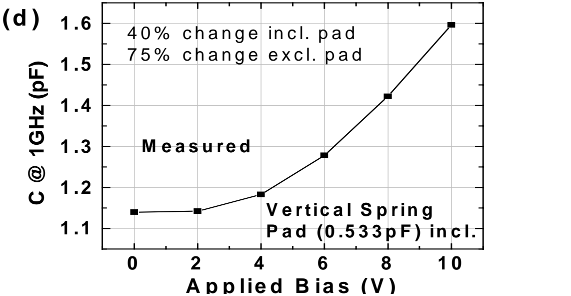

Figure 9. A tunable capacitor with a vertical spring. (a) Device structure. (b) SEM photomicrograph of the fabricated device. (c) RF characteristic for both 0V and 10V bias voltage. (d) Measured tuning characteristic.

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