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Silicide-Based Release of High Aspect-Ratio Microstructures

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ABSTRACT

A new method for releasing high aspect-ratio microstructures has been demonstrated that utilizes silicidation to form gaps between movable microstructures and their substrates in substantially faster times than conventional sacrificial layer-based release methods and with much less concern for stiction or attack of unintended layers. The key enabling element is the use of a self-sufficient chemical reaction (such as silicidation) to provide volume shrinkage that then induces a gap between surfaces involved in the reaction. Using this silicide-based approach, 260:1 aspect-ratio gaps have been released in less than 2 minutes, which is much shorter than the 40 minutes or more that would otherwise be required by wet-etching. This silicidation-based approach to releasing microstructures greatly increases the achievable lateral dimensions of etch hole-free suspended microstructures and stands to substantially lower the time and cost required to produce such structures.

1. INTRODUCTION

Release processes, whereby sacrificial material between two structural materials is removed to free them from one another, often comprise the most limiting and costly steps in MEMS fabrication. Such processes generally employ liquids or gases to etch and are fraught with numerous perils, including stiction [1]; the need for long release times governed by mass transport rates that lengthen as gap aspect-ratio increases [2]; the (ensuing) attack of unintended layers due to finite etchant selectivity; and the formation of etch by-products (e.g., bubbles, gunk) that remain in the gaps. These yield-limiting phenomena often force alterations in MEMS designs (e.g., release holes) that compromise the performance of applications employing high-aspect ratio gaps. Indeed, the set of affected applications is quite large, from inertial sensors that must incorporate mass-reducing etch holes into their proof masses to speed up the release process [3]; to sealed encapsulation chambers, many of which are achieved via cap-to-wafer bonding methods rather than more area-efficient film deposition strategies [4], since the latter often ending up requiring lengthy etches to release structures within the encapsulation; to GHz high-*Q* mechanical resonators [5], for which the size of the electrode-to-structure gap spacing needed to achieve low impedance and good power handling is limited nearly entirely by the release etch process.

This work erases such limits by introducing a new method for forming high aspect ratio gaps between movable (or immovable) structures that avoids etching and its associated drawbacks, entirely. Instead, the method here employs a self-sufficient silicide chemical reaction to provide volume shrinkage that then induces a gap between surfaces involved in the reaction. Using this silicide-based approach, 100×100μm^2 membranes with membrane-to-substrate gaps of only 385nm—a 260:1 lateral dimension-to-vertical gap aspect ratio—have been released in only 2 minutes, which is much shorter than the 40 minutes or more that would be required to wet-etch a 385nm sacrificial oxide under a membrane of sim-similar size. In addition, 32.5 nm gaps have been formed between a SiGe film and a silicon substrate, verifying the efficacy of this method for attaining sub-50nm gaps, such as needed for capacitive RF micromechanical resonators.

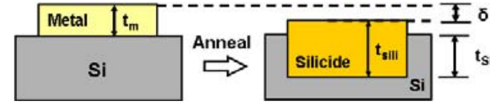

Table 1 Properties of common silicides

Silicide	Silicidation Temperature	t_{Si}	t_{sili}	Volume Shrinkage	δ
Ni_2Si	~250C	0.91	1.47	23.0%	0.44
NiSi	~400˚C	1.84	2.22	21.8%	0.62
$TiSi_2$	~850˚C	2.30	2.50	24.1%	0.8
PtSi	~500˚C	1.30	1.95	15.1%	0.35
$CoSi_2$	~750˚C	3.60	3.53	23.2%	1.07
$MoSi_2$	~750˚C	2.56	2.59	27.25%	0.97

t_{si} = nm of Si consumed per nm of metal (t_m=1)
t_{sili} = nm of silicide formed per nm of metal (t_m=1)
δ = nm of step height change per nm of metal (t_m=1)

2. SILICIDE-INDUCED GAPS

The key recognition behind the present work is that etching is not needed to form a gap. Rather, a gap can also form if a method is available for shrinking the volume of a submerged layer. If this method is a chemical reaction, as in this work, then it is preferable that it be self-sufficient such that all the reactants and the products of the reaction remain on the wafer. This self-sufficient property eliminates the need for diffusion paths so eliminates the root of the problem that plagues etch-based release processes. Moreover, this reaction should be fast and dry to enhance throughput and to avoid problems with stiction and bubble formation.

One reaction that satisfies the above criteria is silicidation [6], whereby silicon, the most commonly used material in CMOS and MEMS, reacts under elevated temperatures with a variety of metals to form silicides. Table 1 [6] lists properties of common silicides pertinent to volume shrinkage-based gap formation. Here, silicidation temperatures range from 250˚C to 850˚C depending on the types of metals and on the phases of silicides. The data also includes information gauging the amount of “volume shrinkage” afforded by a given silicidation reaction, assuming a starting metal sitting flush atop a silicon substrate, as illustrated in the schematic above Table 1.

Fig. 1(a) illustrates one method by which silicidation can be used to form a submerged gap. Here, 10nm of

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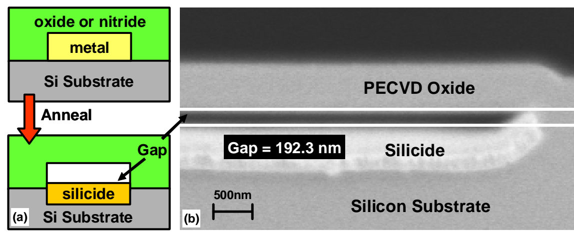

Fig. 1: (a) Process flow and (b) SEM cross-section of a 192nm air gap formed between oxide and silicide. Here, 200nm-Mo reacts with silicon but not oxide at the anneal temperature.

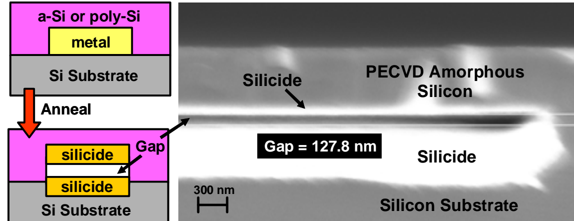

Fig. 2: Process flow and SEM cross-section of a 128nm air gap formed between amorphous silicon and silicide. Here, 150nm Mo forms silicides unevenly on both sides due to differences in single-crystal and amorphous Si silicidation behavior.

molybdenum (Mo) is sandwiched between silicon (Si) below and a capping layer of oxide above. Upon heating via rapid thermal annealing in a low oxygen environment, the Mo and Si react to form $MoSi_2$, whereby 10x2.56 =25.6nm of silicon is consumed to form 10x2.59 =25.9nm of $MoSi_2$. This means the step height changes from the 10nm original metal thickness to now only 25.9-25.6=0.3nm, leaving a 10-0.3=9.7nm gap between the top of the silicide and the bottom of the oxide cap.

The advantages of this silicide-based approach over etch-based release processes are numerous and include:

1) Greatly reduces the time needed for release, since the time required is governed by a single interface reaction time rather than by lateral transport rates;
2) Avoids damage to structures not involved in the release, which is an important limiting side-effect of sacrificial layer-based approaches, where the etchant used often has a finite selectivity to other surrounding layers, so attacks and removes them;
3) Avoids surface tension-based sticking or problems with bubble formation during release that commonly plague wet release approaches;
4) Allows the formation of gaps in sealed chambers, i.e., no need for access routes.

3. EXPERIMENTS

Fig. 1 and Fig. 2 summarize processes used for basic demonstration of silicide-induced gaps. In Fig. 1, 200nm of sputtered molybdenum is patterned by wet etching into strips, followed by 600nm of PECVD capping oxide deposited at 300˚C. After just one minute of annealing at 750˚C, a gap forms when volume shrinkage during silicidation pulls the silicided silicon surface away from the capping oxide. The rounding at the gap edges results from rounding of the original metal corners during isotropic wet etching. The gaps essentially take on the shape of the metal layer, and the shape of silicide is a mirror image of the metal relative to the silicon surface.

The process of Fig. 2 differs from that of Fig. 1 only in the use of a semiconductor top layer, where PECVD amorphous silicon is used instead of oxide. Otherwise, the silicidation procedure is essentially the same, except

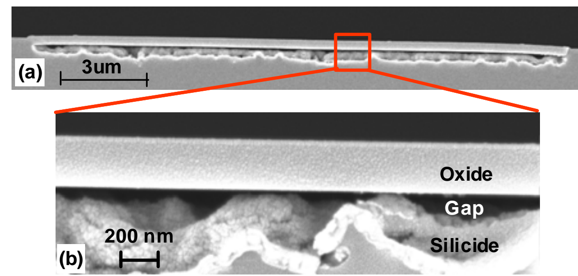

Fig. 3: SEM cross-section showing a roughened silicide surface caused by thin oxide at the silicon-metal interface.

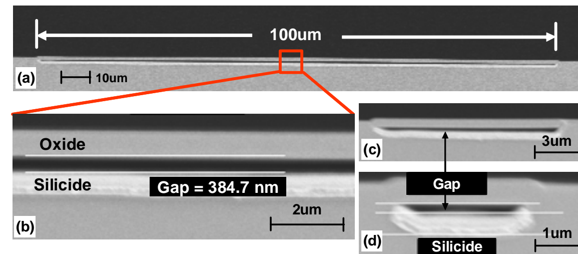

Fig. 4: SEM cross-sections of (a) a 100μm-wide 410nm-thick oxide diaphragm suspended 385nm above the substrate and (b) a zoom-in. The original Mo thickness was 400nm. (c) and (d): Smaller diaphragms released in the same annealing step.

that now silicides form on both the top and bottom surfaces of the gap. This process has the advantage of allowing a conductive semiconductor structural material, which is needed for electrostatic transduction. For applications where silicidation at the bottom of the conductive microstructure is not desired, e.g., due to stress imbalance issues, it can be prevented by depositing a thin layer of dielectric between the microstructure and the metal, similar to the thin side-wall spacers used in CMOS to prevent silicidation on the polysilicon gate [7]. For applications where sub-10nm dielectric layers can compromise device performance, such as capacitively transduced high-Q resonators and switches, conductive materials that do not react with metal at the silicidation temperatures can be used as structural layers. Some good candidates include silicon carbide, polycrystalline diamond, or metals with higher silicidation temperatures.

For repeatable and high quality silicide formation, the interface between the metal and semiconductor must be clean and native-oxide-free. To insure this, a buffered hydrofluoric acid (BHF) dip and slight *in-situ* sputter etch precede the actual metal sputtering step in the above processes. The importance of doing this is immediately apparent when oxide is present at the interface. In particular, when samples before metal deposition are shortly dipped in piranha instead of BHF with no sputter etch, and the same thermal annealing conditions applied, silicidation either does not happen or the silicide surface becomes very rough, as shown in Fig. 3.

To gauge the permissible temperature ceiling during process steps before and after the silicidation anneal, Mo-over-Si samples were heated in a conventional oven at 350˚C for 6 hours before and after the one minute 750˚C silicidation anneal, with no change in silicide step height versus a Mo-over-Si sample without extra thermal treatments. This confirms that microstructures can be released at the very end of a process as long as processing temperatures after metal deposition do not exceed the silicidation temperature. Moreover, once the silicide is formed, thermal processes generally do not change the

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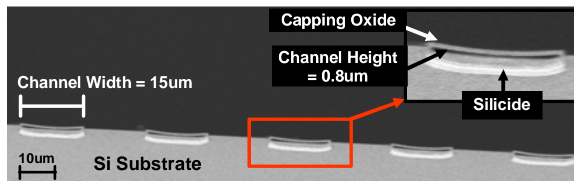

Fig. 5: Cross-sectional SEM of an array of oxide-capped micro-channels on a silicon substrate fabricated via silicide-induced release.

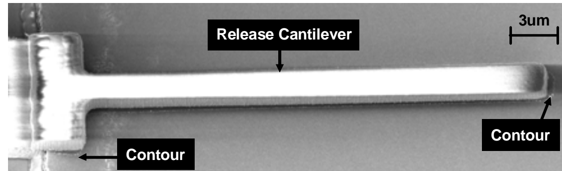

Fig. 6: SEM of a 1.2μm-thick oxide cantilever separated from the substrate by a silicide-induced gap.

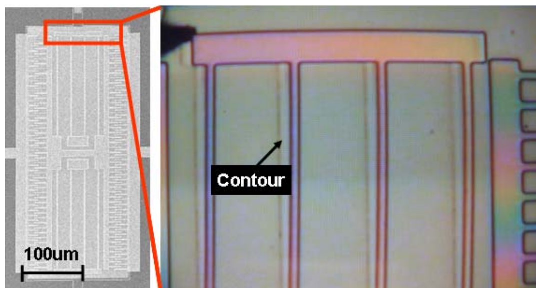

Fig. 7: SEM of a released folded-beam comb-driven structure with springs bent by a probe tip.

size of the gap.

More General Geometries

Mere patterning of the capping layer before the silicidation anneal yields suspended movable structures with more general geometries. Figs. 4-7 present images of various patterned oxide structures released via the described silicide approach, including a 100×100μm^2 membrane with a 260:1 lateral dimension-to-vertical gap aspect ratio and membranes with smaller sizes formed by the same one minute thermal anneal step (Fig. 4); an array of 15μm-wide, 0.8μm-high, 9mm-long micro-channels that attest to the repeatability of this approach (Fig. 5); a 20μm-long, 2μm-wide oxide cantilever (Fig. 6), and a folded-beam comb-driven resonator with springs bent by a probe, confirming that they are released (Fig. 7). Successful release of such compliant microstructures is possible because silicidation is a dry process, so does not suffer from stiction. In all cases, the release anneal takes no more than two minutes, and no etchant is consumed, making this approach much faster and cheaper than etch-based release methods.

Tiny Gaps.

Among the most powerful capabilities provided by silicidation is its ability to achieve tiny sub-50nm gaps, which are essential to vibrating RF micromechanical resonators using capacitive transduction. Fig. 8 shows a 32.5nm gap underneath a SiGe capping layer, achieved via a silicidation reaction between Mo metal and the underlying silicon substrate, with comparatively little reaction with the capping SiGe layer. The thirty seconds required for silicidation contrasts sharply with the 40+ minutes of wet-etching often required for small-gapped

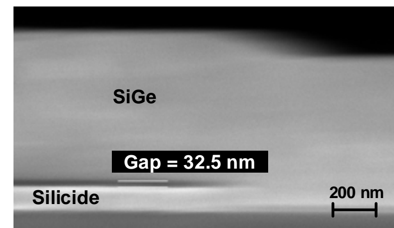

Fig. 8: SEM cross-section of a 32.5nm gap formed between a bottom $MoSi_2$ and a top SiGe capping layer. Even smaller gaps should be achievable via a thinner metal layer.

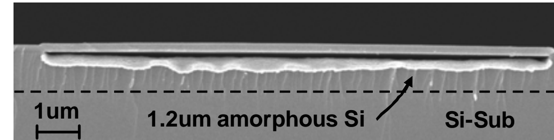

Fig. 9: A silicide-induced gap formed over a 1.2um PECVD amorphous silicon film deposited at 300˚C.

RF micromechanical resonators [5]. Indeed, release times required by etch-based release processes increase with gap aspect-ratio, while those needed for silicide-based release remain virtually the same. Clearly, the described silicide-based release process scales much better than etch-based counterparts. The smallest achievable gap is ultimately limited by the surface roughness of the silicide which is generally on the order of 10nm or less for nickel [8], titanium [9], and cobalt [10]. Gap spacings this small should be very helpful towards capacitively transduced resonators with the sub-50Ω impedances desired by conventional wireless circuits.

Although silicidation occurred with the silicon substrate and not the SiGe in this process, it should be noted that silicide-induced release is not limited to silicidation with single crystal silicon, but also works with amorphous and polycrystalline systems, and with semiconductor materials other than silicon, e.g., SiGe. For example, Fig. 9 presents a gap formed between a top oxide capping layer and a 1.2μm PECVD amorphous-silicon layer deposited at 300˚C. This confirms that the described silicide-based release process can be applied to MEMS/NEMS built atop CMOS or on substrates other than silicon, such as glass, as long as a thin layer of semiconductor is available. It also suggests methods by which silicide-based release can form lateral gaps, perhaps using PECVD and/or atomic layer deposition (ALD) methods to deposit conformal lateral semiconductor and metal films with well-controlled thicknesses at temperatures lower than the silicidation temperature.

4. APPLICATIONS

To demonstrate the use of silicide-induced gaps in a practical application, the three-mask process shown in Fig. 10 uses titanium (Ti) as a structural material and Mo as the siliciding metal to fabricate beam resonators. Here, Mo is sputter deposited after a short *in-situ* sputter etch to remove native oxide, then patterned using a commercial aluminum wet etchant (pre-mixed phosphoric and acetic acid mixture) at 50˚C. Next, 300nm of 300˚C PECVD oxide isolation liner is deposited and patterned via a BHF dip, followed by sputter deposition of 700nm of Ti structural material at 300˚C. The Ti is then dry etched via a Cl_2/BCl_3 plasma, with the etch stopping on the underlying Mo or oxide layer. The structure is finally released via a one minute rapid thermal anneal step. As shown in Fig. 10, $MoSi_2$ forms the ground plane/drive electrode for

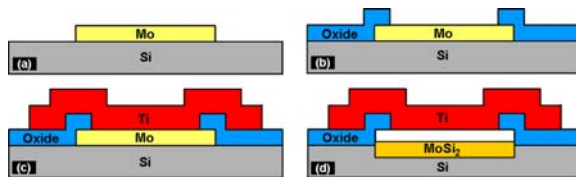

Fig. 10: Process flow yielding a titanium clamped-clamped beam released via silicidation: (a) Sputter and pattern molybdenum over silicon substrate; (b) deposit 300nm 300˚C PECVD oxide and remove over device areas and bond pads; (c) sputter and pattern 700nm titanium structural material; and (d) release via rapid thermal annealing at 750˚C.

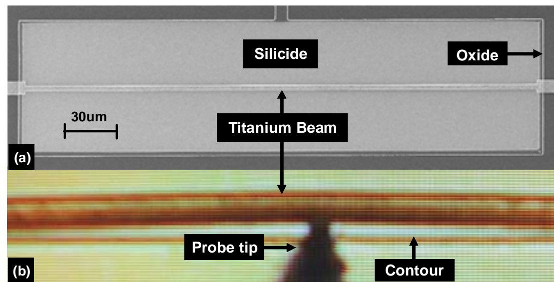

Fig. 11: (a) SEM of a 320μm-long, 3μm-wide, 700nm-thick titanium clamped-clamped beam using the process of Fig. 10. (b) Bending via a probe tip confirming release.

this clamped-clamped beam, and the oxide layer prevents the beam from shorting with the silicide.

Fig. 11 presents the SEM of a released 320μm-long, 3μm-wide Ti clamped-clamped beam displaced laterally by a probe tip. Fig. 12 further presents the mixing-measured [5] frequency characteristic (in vacuum) for a 20μm-long, 2μm-wide beam with 150nm electrode-to-resonator vertical gap spacing, confirming functionality of the beam and applicability of the silicide-based release process in an actual application.

5. CONCLUSIONS AND FUTURE WORK

By utilizing a volume shrinkage-based method for forming gaps between structural layers and thereby avoiding the need for etching, the silicide-based release process demonstrated in this work is cheaper, cleaner, and faster than conventional etch-based methods, as it requires no etching, consumes no chemicals, and has little dependence on mass transport processes. Using this method, structures with aspect-ratios exceeding 260:1 have been released in less than two minutes—substantially less than the 40 minutes otherwise required by an etch-based release process. Although this work features silicides based on Mo, it should be understood that any of the metals in Table 1 could also be used.

But the benefits of silicidation methods go far beyond mere release of high-aspect ratio gaps. In particular, the fact that silicidation is a heat-induced and self-sufficient reaction that does not require a diffusion path suggests the possibility for localized and post-package release without any need for release holes in the package structure. To expand upon this, Fig. 13(a) [11] presents one conventional approach to wafer-level encapsulation where release holes in the encapsulating cap are needed to allow release etchants to access a sacrificial layer that completely encases the structure under the cap. Since the diffusion paths are quite tortuous, the time required for release is generally quite long and etch by-products have difficulty diffusing out. On top of this, the need to seal the etch holes can compromise both the package and

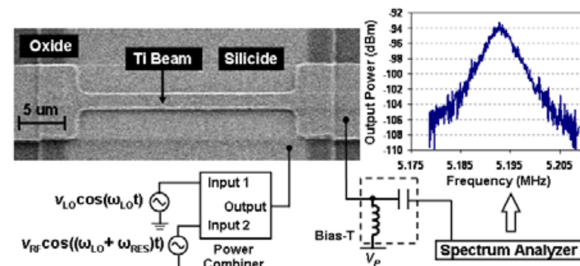

Fig. 12: Mixing measurement setup and measured resonant peak under vacuum for a Ti clamped-clamped beam released via silicidation, with Q=1,082. Here, P_{RF}=10dBm (network analyzer output), V_{LO}=10$V_{P\text{-}P}$, and V_P=20V.

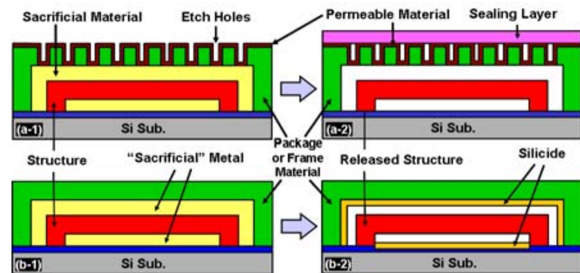

Fig. 13: Cross-sectional summaries of (a) a conventional thin-film package where (a-1) etch holes provide access for sacrificial material removal and (a-2) a deposition step is required to seal; and (b) a silicide-based release packaging method that obviates the need for etch holes and sealing that comprises (b-1) deposition and patterning of a proper succession of semiconductors and metals and (b-2) a short silicidation anneal.

device within (if the sealant also deposits on the device).

In contrast, silicidation (requiring no diffusion path) can form gaps submerged beneath the cap layer with no need for etch holes, as shown in Fig. 13(b). The packaging process would require just minutes of anneal time and would be local to areas with the right metal-semiconductor pairings. Efforts towards post-package and release of capacitive resonators are ongoing.

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