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FULLY MONOLITHIC CMOS NICKEL MICROMECHANICAL RESONATOR OSCILLATOR

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ABSTRACT

A fully monolithic oscillator achieved via *MEMS-last* integration of low temperature *nickel* micromechanical resonator arrays over finished foundry CMOS circuitry has been demonstrated with a measured phase noise of -95 dBc/Hz at a 10-kHz offset from its 10.92-MHz carrier (i.e., output) frequency. The use of a side-supported flexural-mode disk resonator-array to boost the power handling of the resonant tank is instrumental to allowing adequate oscillator performance despite the use of low-temperature nickel structural material. Because the fabrication steps for the resonator-array never exceed 50°C, the process is amenable to not only MEMS-last monolithic integration with the 0.35 μm CMOS of this work, but also next generation CMOS with gate lengths 65 nm and smaller that use advanced low-k dielectric material to lower interconnect capacitance.

1. INTRODUCTION

Oscillators referenced to high-*Q* vibrating micromechanical resonators have recently begun displacing quartz counterparts in low-end timekeeper applications [1][2], and research demonstrations that satisfy some high-end specifications (e.g., phase noise for GSM [3]) now encourage a possible expansion of the MEMS oscillator market into cell phone and other more demanding applications. To date, however, the MEMS-based oscillators being commercialized have not realized their potential for on-chip integration alongside transistor circuits. To remedy this, numerous integration approaches have been demonstrated, including modular ones that separate the transistor and MEMS process steps into modules, thereby facilitating incorporation of inevitable advancements in transistor or MEMS technologies [4][5][6][7]. Of the modular approaches, *MEMS-last* [6][7] is perhaps the most economical, since it ideally allows integration with *any* CMOS transistor foundry, which then permits the use of the lowest cost CMOS—something *MEMS-first* counterparts cannot always promise, since advanced CMOS foundries might hesitate to accept wafers pre-processed by a MEMS (or any outside) foundry. Despite these advantages, *MEMS-last* approaches are still encumbered with the need to keep their MEMS module temperatures below a ceiling value that continues to drop as transistor technologies advance.

This work substantially lowers the processing temperature required for *MEMS-last* integration from the 450°C of [7] to now only 50°C by using electroplated *nickel* structural material that retains resonator *Q*'s in the thousands. Using this process, a fully monolithic single-chip oscillator comprising a *nickel* micromechanical resonator array over finished foundry CMOS achieves a measured phase noise of -95 dBc/Hz at a 10-kHz offset from its 10.92-MHz carrier (i.e., output) frequency, which equates to a phase jitter < 1 ns. Because the fabrication steps for the resonator-array never exceed 50°C, the process is amenable to not only MEMS-last monolithic integration with the 0.35 μm CMOS of this work, but also next generation CMOS with gate lengths 65 nm and smaller that use advanced low-k (but low melting point ~300°C) dielectric material to lower interconnect capacitance [8].

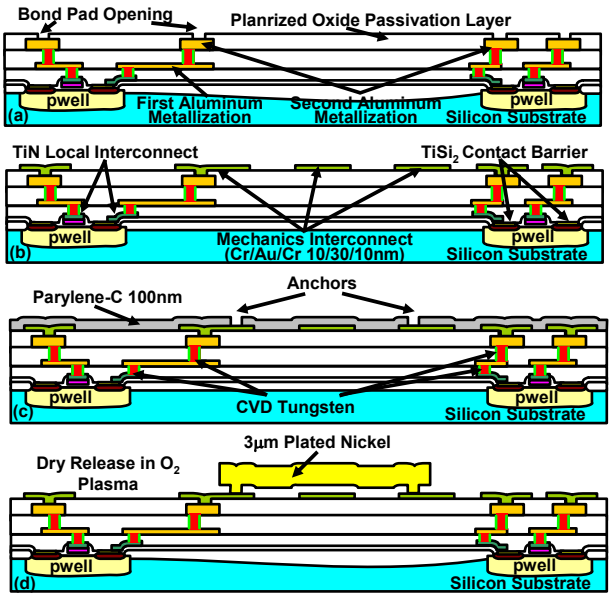

Fig. 1: Cross sectional fabrication process flow for the fully monolithic nickel flexural-mode disk-array oscillator.

2. MEMS-LAST INTEGRATION PROCESS

The process flow used for MEMS-last integration is summarized in Fig. 1. As advertised, the process is done over a finished CMOS foundry circuit, in this case provided via TSMC's 0.35 μm four-metal process obtained via MOSIS. Since MOSIS provides only 2.5 mm × 2.8 mm chips of transistor circuitry, and not full wafers, 4″ carrier wafers were required to allow the use of semiconductor processing tools housed in the clean room of the Michigan Nanofabrication Facility. Each carrier wafer was prepared by first deep reactive-ion etching a single 200 μm deep trench, 2.7 mm-wide by 3.0 mm-long, into the very center of an N-type silicon

wafer; then growing 2 μm of wet oxide to passivate the surfaces. Silver paint is then dropped into the trench and the transistor IC chip carefully inserted. Once dry, the silver paint holds the die quite adequately during subsequent processing steps, all of which do not involve CMOS clean tools, so contamination by silver paint is not an issue. Note that because the die is situated at the very center of the carrier wafer, topography issues arising from the trench surrounding the die are of little consequence.

The starting CMOS wafer has the cross-section shown in Fig. 1(a), where its surface is relatively flat after CMP planarization, and where vias defined via the CMOS bond pad mask have been etched (by the foundry) through a passivation layer down to the top level metal of the CMOS. After loading CMOS chips onto carriers, the MEMS module of the process begins with the blanket sputter deposition of 10/30/10 nm of Cr/Au/Cr, which is then patterned into interconnects that overlap the vias to the top level CMOS metal to realize electrical interconnection between the CMOS and the subsequent MEMS. At this point, the cross-section is as in Fig. 1(b).

Next, a 100-nm-thick parylene-C sacrificial layer (to be removed later) is CVD'ed at room temperature. In the deposition process, a parylene-C starting material is first sublimed under vacuum in a glass tube at a temperature of around 110~130 °C and a pressure of 0.2 mbar, then converted into reactive species by a pyrolysis process at 650~800 °C and 0.2 mbar, respectively, and all of this *away from the wafer*, which then does not experience these temperatures. Subsequent polymerization onto the process wafer mounted on a rotating cooled sample holder then occurs at room temperature and 0.2 mbar pressure. During the deposition process, an argon carrier gas flows at 20 sccm to dilute the concentration of quinodimethanes in the gas phase. The carrier gas effectively reduces intermolecular interaction and prohibits side reactions [9], resulting in better film quality. After deposition, the parylene-C is then patterned to form anchor vias, yielding the cross-section of Fig. 1(c).

Next, a 10-nm-thick nickel seed layer is blanket evaporated and 3 μm of SPR220-3.0 photoresist is spun, exposed, and patterned to form an electroplating mold that defines mechanical structures. Nickel electroplating then follows at 50°C in a sulfate-based solution [10]. After removing the photoresist mold, the nickel seed layer is stripped using a custom wet etchant solution. The parylene sacrificial layer is then removed by an isotropic O_2 plasma etch to yield the final released cross-section of Fig. 1(d).

As advertised, at no point in the described MEMS-last process module are the wafers exposed to any temperature exceeding 50°C.

3. OSCILLATOR DESIGN

Like a previous rendition published by this group [3], the oscillator here comprises a vibrating micromechanical resonator array embedded in a positive feedback loop with a CMOS amplifier circuit that sustains the oscillation. In this case, however, the use of parylene as a sacrificial material differs sufficiently from previous small-lateral-gap processes (e.g., in polysilicon [11] and nickel [12]) to warrant more conservative design measures, especially for the MEMS.

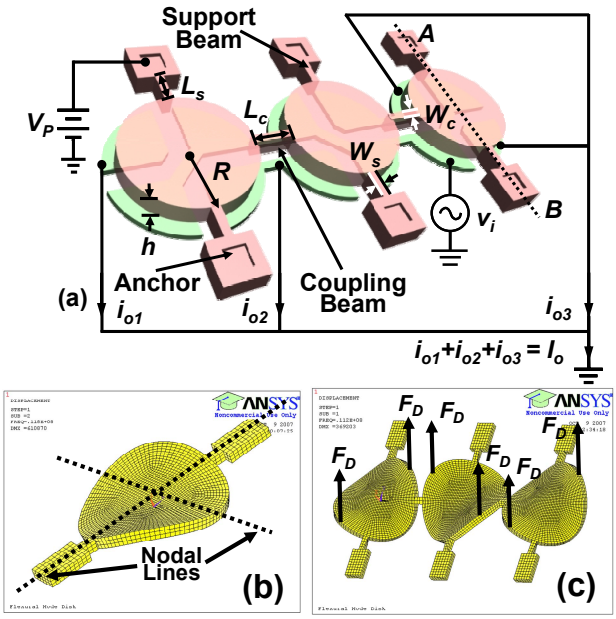

Fig. 2: (a) Perspective view schematic of a micromechanical flexural-mode disk resonator array, identifying key dimensions and showing a typical two-port bias and excitation configuration. (b) Mode shape of a constituent disk. (c) The flexural-mode shape of the disk array selected by properly phased electrostatic driving forces F_D induced by the hookup in (a). Both mode shapes were simulated via ANSYS.

A. Flexural-Mode Disk Resonator Array

Fig. 2(a) depicts the nickel flexural-mode disk resonator array used as the reference tank element in the oscillator circuit. Like the array of [3], this structure consists of several disk resonators coupled by mechanical beams. Unlike the array of [3], which used wine-glass mode resonators, the disks in the present array are designed to vibrate in the flexural mode used in [13] and shown in Fig. 2(b). For this mode shape, the resonance frequency is governed by

$$f_0 = 0.253\frac{h}{R^2}\sqrt{\frac{E}{\rho}} \qquad (1)$$

where h and R are the thickness and radius, respectively, of the disk; and ρ and E are the density and Young's modulus, respectively, of its nickel structural material. Each disk has a radius of 15 μm and thickness of 3 μm, and is equipped with electrodes spaced d = 100 nm from the undersides of each of its four quadrants that not only provide capacitive transduction, but also allow selection of the resonator mode shape via proper phasing of signals applied to each quadrant.

The use of flexural mode resonators, rather than the wine-glass versions previously proven to have excellent Q's >50,000 in [12], is a conservative measure taken to insure successful devices in the face of a new process flow that utilizes parylene, rather than nitride, as a gap material. This strategy did indeed yield working resonator devices more quickly, but at the cost of Q, which at 1,651 is lower than that of the wine-glass resonators of [12] by 33X. This then degrades (i.e., raises) the close-to-carrier phase noise of the oscillator, which is proportional to $(1/Q)^2$.

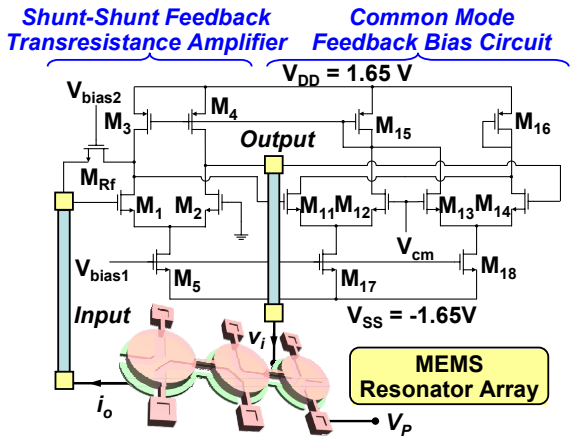

Fig. 3: Circuit schematic of the disk-array oscillator, showing the details of its single-stage transresistance sustaining amplifier comprised of a fully balanced differential stage in a one-sided shunt-shunt feedback configuration.

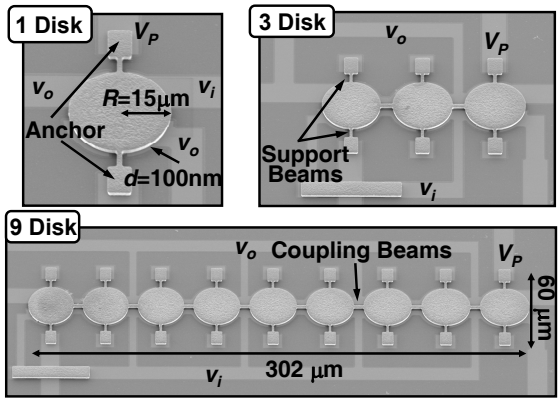

Fig. 4: SEM's of flexural-mode disk-array resonators using varying numbers of mechanically-coupled disks.

Like the structure in [3] the mechanical connection of resonators in the array actually realizes a multi-pole filter structure, from which a single mode can be selected while others suppressed by proper electrode phasing shown in Fig. 2(c). Since in the selected mode all resonators vibrate at the same frequency, their outputs can be summed, yielding a structure that practically acts as a single resonator, but with a current handling capability equal to the sum of the currents from all constituent resonators. This larger current handling greatly improves the short-term stability of the overall oscillator circuit, compensating somewhat for the lower Q issue mentioned above. It also lowers the motional resistance of the array by n times, where n is the number of resonators in the array. This then greatly simplifies the design of the oscillator, since a lower motional resistance allows oscillation with a smaller sustaining amplifier gain factor.

B. CMOS Sustaining Amplifier

The transresistance CMOS sustaining amplifier used here (shown in Fig. 3) is similar to the one in [14], in that it achieves the needed 0° phase shift for oscillation using only a single stage, which improves both its noise and bandwidth performance. As shown in Fig. 3, the circuit comprises a fully differential amplifier using shunt-shunt feedback on one side to effect a transresistance gain function, while taking the output from the other side to provide a total 0° phase shift from input to output.

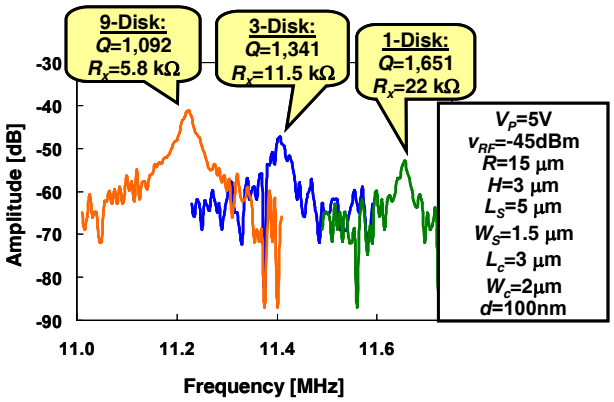

Fig. 5: Measured open-loop frequency characteristic for nickel mechanically-coupled flexural-mode disk resonator arrays.

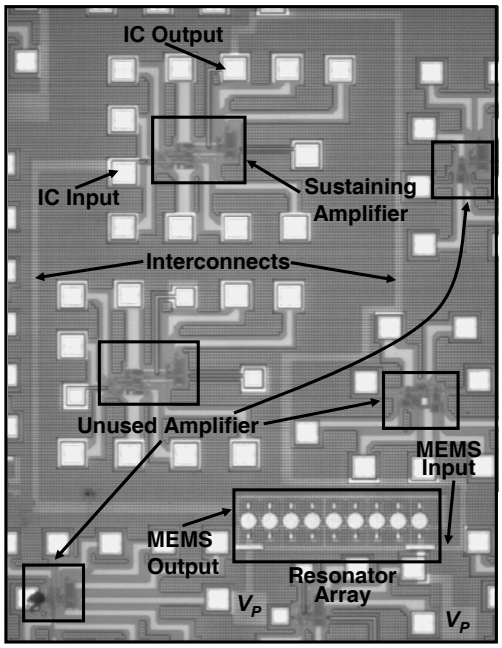

Fig. 6: Overhead photo of the 10.92-MHz fully monolithic CMOS nickel micromechanical resonator oscillator.

4. EXPERIMENTAL RESULTS

Fig. 4 presents SEM's of fabricated nickel disk arrays with varying numbers of coupled resonators, with each resonator supported by only two support beams. The measured frequency spectra for a stand-alone disk resonator together with arrays using three and nine mechanically coupled resonators are shown in Fig. 5, where a rise in output current with resonator number is clearly seen, and all Q's are greater than 1,000. For fair comparison of motional resistances, all devices shared the same 5V DC bias during measurement.

Fig. 6 presents a top-view photo of the monolithic nickel resonator-array oscillator, clearly showing the IC sustaining amplifier fully integrated alongside the MEMS resonator

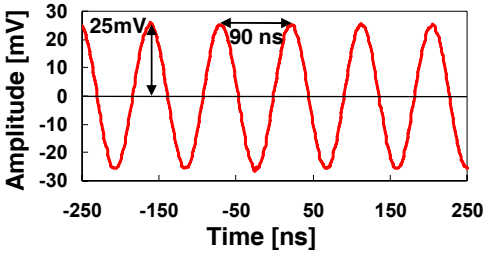

Fig. 7: Measured output oscilloscope waveform for the fully monolithic nickel micromechanical resonator oscillator.

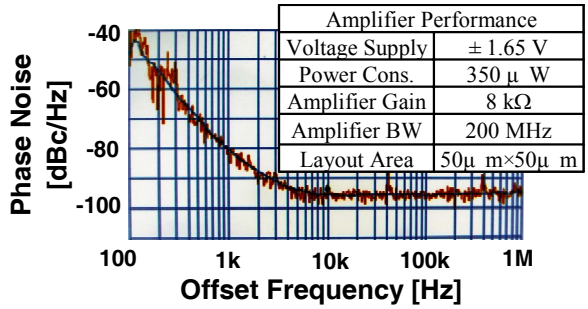

Fig. 8: Phase noise versus carrier offset frequency plots for the fully monolithic nickel micromechanical resonator oscillator.

array onto a single chip. In this rendition, the nickel resonator-array was not placed directly over the transistor IC, mainly for layout convenience and so that both can be seen without interference under a microscope. If the MEMS devices were placed directly over the transistor circuit, the footprint of this oscillator circuit would be dominated by the area of the resonator-array, which is 302μm ×60μm.

Fig. 7 presents the output waveform of the oscillator measured on an oscilloscope when operated under 1 mTorr vacuum pressure. Fig. 8 presents a plot of phase noise density versus frequency offset from the 10.92-MHz carrier, measured using an Agilent 8565EC Spectrum Analyzer equipped with a phase noise measurement module. The phase noise at 10-kHz offset from the carrier (i.e., a far-from-carrier offset) is -95 dBc/Hz, which equates to a phase jitter of about 770 ps. This is not nearly as good as achieved by the oscillator of [3], which actually met GSM phase noise specifications, but is reasonable given the use of a more conservative flexural-mode disk resonator. Work to achieve a nickel-based MEMS oscillator that meets GSM reference oscillator specifications is ongoing.

5. CONCLUSIONS

A fully monolithic 10.92-MHz nickel micromechanical reference oscillator has been demonstrated using a series resonant oscillator topology comprising a nine nickel flexural disk array atop a custom-designed transresistance sustaining amplifier IC. The 770 ps phase jitter performance of this oscillator is sufficient for low-end clock applications, such as those for digital data transfer. Further performance improvements, e.g., towards cellular phone reference oscillator phase noise specifications, should be possible via use of more aggressive resonator design, perhaps using wine-glass modes capable of achieving much higher *Q*. In this endeavor, the nickel wine-glass mode resonator of [12], with a *Q*~54,500 at 60 MHz, would be a good choice. Of course, attaining GSM phase noise specifications would be moot if the needed drift and temperature stability specs where not simultaneously met. Although methods to improve drift [15] and temperature dependence [10] in nickel micromechanical resonators have been demonstrated, much more study into the long-term stability of electroplated nickel material is needed before it can be considered for practical oscillator applications.

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