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Process technology for the modular integration of CMOS and polysilicon microstructures

James M. Bustillo, Gary K. Fedder, Clark T.-C. Nguyen, Roger T. Howe

Abstract Modular fabrication of polysilicon surface-micromachined structures after completion of a conventional CMOS electronic process is described. Key process steps include tungsten metallization with contact diffusion barriers, LPCVD oxide and nitride passivation of the CMOS, rapid thermal processing for stress-relief annealing of the structural polysilicon film, implementation of a sacrificial spin-on-glass planarization, and the final microstructure release in hydrofluoric acid. Modularity of the process enables independent modification of either the CMOS or the microstructure process sequences. This technology is used in the fabrication of various types of sensors and actuators.

1 Introduction

Polycrystalline silicon micromechanical structures have been a focus of academic research for more than a decade with increasing commercial developments over the past few years. These microstructures are fabricated by selective etching of an underlying oxide sacrificial layer, a process known as "surface micromachining." Illustrated in Fig. 1, this process relies on the sequential deposition of a sacrificial layer, in this case phosphosilicate glass, and a phosphorus-doped polycrystalline silicon structural material. The structural layer is anchored to the substrate by vias etched through the glass. Repeating this sequence can yield stacked structures consisting of more than one structural layer. The final fabrication step involves a release etch, in this case in hydrofluoric acid, to remove the underlying sacrificial glass; which results in free-standing polysilicon structures capable of vertical or lateral motion. Alternatives to this approach have been investigated in which aluminum [Hornbeck (1993)], tungsten [Chen et al. (1993)], or silicon nitride [Albrecht et al. (1990)] have been used as the mechanical material. These techniques may also employ alternative sacrificial materials, such as the polymers used in the aluminum process just mentioned. The technology described in this paper relies on low-pressure chemical vapor deposited polycrystalline silicon as the preferred mechanical material because of its compatibility with standard planar integrated circuit processing, desirable and well understood mechanical properties [Petersen (1982)], and the ability to control the resistivity throughout the structural member.

Capacitive sensing of these structures is much easier with on-chip MOS buffer amplifiers, and requires the compatible fabrication of micromechanical and electronic structures. The primary technology-design question is: in what order to build the sensor and the electronics? Surface-micromachined structures can be defined prior to circuit fabrication, afterwards as a post-circuit module or interleaved with thin film layers possibly used for both circuits and microstructures [Yun et al. (1990)]. The first alternative is undesirable because the large relief of sensor devices make subsequent circuit lithography difficult unless major planarization efforts are made. Interleaving the two technologies is feasible, was first demonstrated with NMOS in 1984 [Howe and Muller (1984)], and is being used to fabricate an integrated accelerometer for air-bag deployment [Core et al. (1993)]. Advantages of the post-circuit sensor fabrication model are that circuit areas can be fully passivated prior to initiating sensor construction and that microstructures can be fabricated on top of the interface electronics to minimize chip area. Furthermore, an IC foundry could be used for the electronics while a sensor foundry could receive the partially completed wafers and complete the fabrication sequence. We have chosen to call the modularization of CMOS and microstructures the MICS technology. Micro-electro-mechanical systems (MEMS) fabricated using this modularized MICS technology include an accelerometer [Yun et al. (1992)], a resonator oscillator [Nguyen and Howe (1993)], and an integrated test-bed with multi-mode position control [Fedder and Howe (1994)].

2 MICS technology overview

Figure 2 is a cross section of the CMOS transistors and microstructure as fabricated using the MICS technology. The 3 μm, double-polysilicon, single metal, P-well CMOS technology is fabricated as a baseline module. Precise on-chip capacitors are formed between the two CMOS polysilicon layers: gate polysilicon (CPG) and capacitor electrode polysilicon (CEL). Transistor source, drain, and gate contacts use titanium silicide

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and titanium nitride barrier metallurgy. Circuit interconnect employs a tungsten refractory metallization allowing for high temperature post-processing. Circuit passivation consists of densified phosphosilicate glass and low-stress, silicon-rich nitride depositions. Modifications to the baseline CMOS to accommodate the back-end post-CMOS structural modules were made only at the metallization and circuit passivation steps. Circuit-to-structure interconnect is made with a via cut through the passivation to the CMOS gate polysilicon (SNT mask). The phosphorus-doped ground-plane/interconnect sensor polysilicon (SP1) is then deposited and etched, forming a polysilicon-to-polysilicon contact with the circuits below. Sacrificial glass (PSG1), deposited to the thickness specified by structural designs (typically 2.0 μm), is recessed at certain locations to form stand-offs with subsequent structural polysilicon. These stand-offs, commonly called dimples or limit stops, are etched into the glass with a timed hydrofluoric acid dip (SD2 mask). Typical dimple stand-off depth is 1.0 μm. These limit surface contact area in the event of a touch-down during the post-release drying due to the compliant nature of the structural members, or can be used to reduce frictional forces during operation [Fan et al. (1988)]. Mechanical structures are anchored to the ground-plane by a via cut through the sacrificial glass (SG1 mask). The SG1 via contact serves the dual purpose of anchoring the structure to the substrate and forming an electrical contact for electrostatic detection and actuation. A thick (2.0 μm) *in situ* phosphorus-doped structural polycrystalline silicon (SP2) and 0.5 μm capping oxide are sequentially deposited, and annealed to relax the residual stresses in the structural layer. The capping oxide is used as a non-erodible masking material during the structural polysilicon etch. Holes are made at this time in the structural SP2 layer to allow the hydrofluoric acid to access the PSG1 under the larger structures. Adding another structural polysilicon layer (SP3) requires similar dimple (SD3 mask) and contact anchor (SG2 mask) processing. The high aspect ratios encountered with the SP2 structures require the use of an etch-back spin-on-glass planarization immediately before the second sacrificial glass (PSG2) is deposited. Finally the structural members are released with a hydrofluoric acid etch of the sacrificial PSG layers, leaving suspended polysilicon beams that can move both in plane and out of plane with respect to the substrate depending on the particular device design. All key layers are represented in Fig. 2, with the exception that the sacrificial glasses (PSG1 & PSG2) have already been removed. Their previous location in the structural section to the right is labelled. Table 1 lists all the sensor related lithographic steps used in the MICS process.

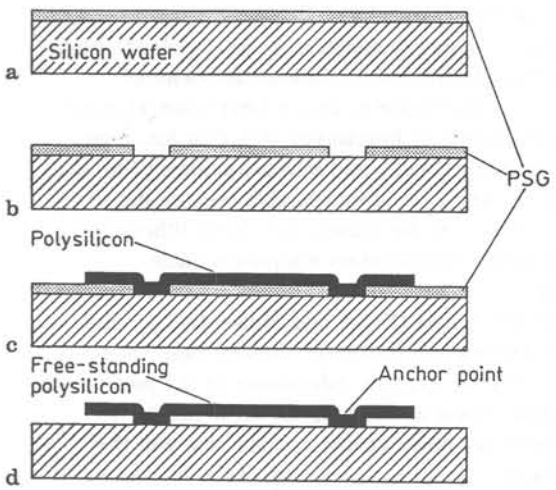

Fig. 1a–d. Surface micromachining steps. **a** deposit sacrificial phosphosilicate glass (PSG); **b** etch holes to form anchor points; **c** deposit & etch structural polysilicon; **d** HF etch of sacrificial PSG to free structures

3
Process development and fabrication issues

Polysilicon microstructure fabrication requires several temperature excursions beyond what is normally associated with typical back-end CMOS technologies. The active MEMS devices, fabricated after the electronics with post-CMOS manufacturing

Table 1. MICS sensor lithography steps

layer name	description	aligns to
SNT	passivation via cut	CPG
SP1	sensor ground-plane poly	CPG
SD2	first dimple	SP1
SG1	PSG1 anchor/via cut	SP1
SP2	first structural polysilicon	SP1
SD3	second dimple	SP2
SG2	PSG2 anchor/via cut	SP2
SP3	second structural polysilicon	SP2
SREL	protective release mask	SP2

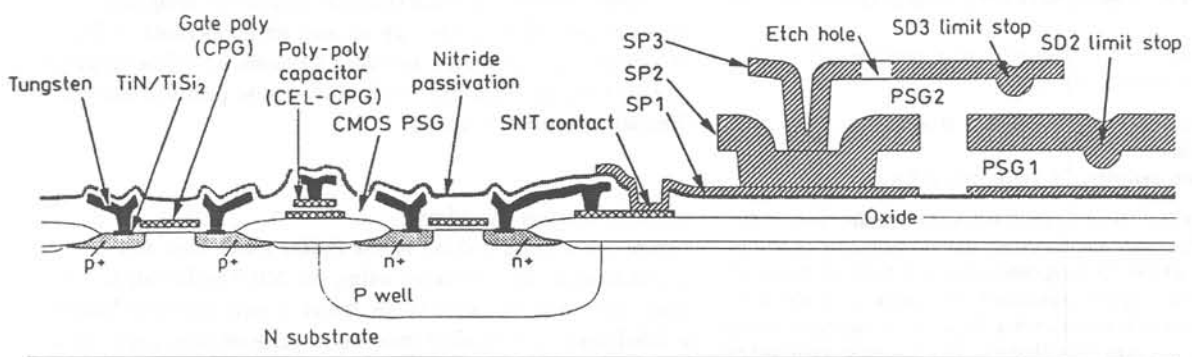

Fig. 2. Cross section of the MICS technology

modules, require that the CMOS be protected by robust passivation impervious to the environment and release etch chemistries. This passivation relies on a dual layer dielectric of LPCVD phosphosilicate glass and silicon-rich, low-stress LPCVD silicon nitride. Prerequisites for this passivating layer are that it reasonably planarize, that it have relatively low residual stress, that it be pinhole free, and unaffected by the hydrofluoric acid used in the microstructural release step.

Circuit planarization is accomplished by 4500 Å of densified PSG, which is then covered by a 1750 Å thick low-stress nitride that serves as an acid barrier. The low PSG deposition temperature of 450 °C is followed by a densifying rapid thermal anneal (RTA) at 900 °C for 30 sec. RTA is used in order to minimize electronic degradation due to temperature-induced dopant redistribution. The stress of the amorphous low-stress silicon nitride is regulated during deposition by fixing the stoichiometry to silicon-rich, rather than by post-deposition annealing. This is done by adjusting the ratio of the reactant gases, dichlorosilane and ammonia (DCS and NH_3), so that the gas chemistry is silicon-rich as compared to conventional LOCOS silicon nitride. Figure 3a shows the dramatic effect of this gas ratio on the measured average film stress. Typical passivating films use a 4:1 DCS:NH_3 gas ratio, resulting in films having 250–300 MPa tensile stress. Also shown is the change in refractive index as a function of stoichiometry-regulated film stress (Fig. 3b). This optically measured parameter is routinely used as an in-line process monitor. The nitride deposition temperature of 835 °C places constraints on the interconnect metallurgy, requiring that both the silicide and interconnect metals be able to withstand high temperatures.

MICS structural polysilicon is formed by a decomposition of silane and phosphine (thin-film phosphorus content at the point of supersaturation) at 375 mT and 610 °C. The 2 μm thick structural polysilicon films must have low average residual stress and a very low stress gradient in order to be useful for microstructure fabrication. As-deposited *in situ* phosphorus-doped films that generally nucleate in the crystalline phase at deposition temperatures of 610 °C do not satisfy these requirements and require post-deposition RTA to relieve stresses. Figure 4 is a transmission electron micrograph showing the as-deposited phase morphology for the MICS polysilicon [Johnson and Krulevitch (1993)]. The graph on the right shows the stress gradient through the polysilicon thickness, and illustrates how the intrinsic stress is directly associated with this morphology. This stress can go from compressive to tensile depending on whether the film is amorphous or crystalline respectively. Phase transformations throughout the thickness of the film are particularly troublesome for the MEMS engineer because they result in through-film stress gradients that will cause the mechanical structures to bend upwards or downwards with respect to the substrate. Unlike the amorphous silicon nitride passivation layer, the structural polycrystalline silicon material can undergo phase changes with post-deposition thermal treatments. RTA at 900 °C for 60 sec. in argon changes the average stress from approximately 500 MPa compressive to between 40 MPa compressive to 5 MPa tensile. Figure 5 illustrates how the RTA can adjust both the residual film stress and electrical resistivity of the MEMS structural layers. The average film stress was reduced from an as-deposited 550 MPa +/− 32 MPa (3σ) compressive, to values ranging from 136 MPa

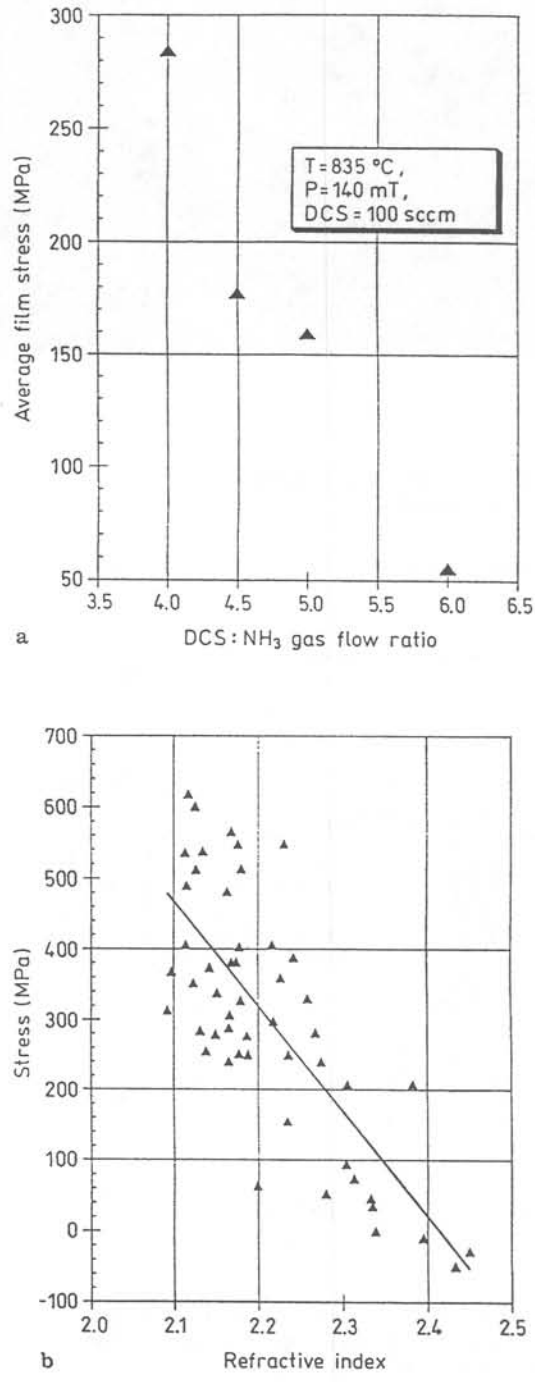

Fig. 3a, b. Stoichiometry control of low-stress nitride. a average film stress vs silicon content; b in-process stress monitoring using the refractive index. Positive values imply average tensile stress

compressive to 69 MPa tensile with 60 sec. anneals from 800 °C to 1050 °C respectively. Shorter anneal times of 30 sec. resulted in less stress relaxation at temperatures less than or equal to 900 °C, with no additional relaxation observed for longer time anneals at the higher temperatures. Residual stress was calculated by measuring the induced wafer curvature for a given film thickness after removing that film from one side of a substrate whose Young's Modulus and thickness are known. Wafers used in this characterization experiment did not have the capping oxide, and as such, were susceptible to dopant

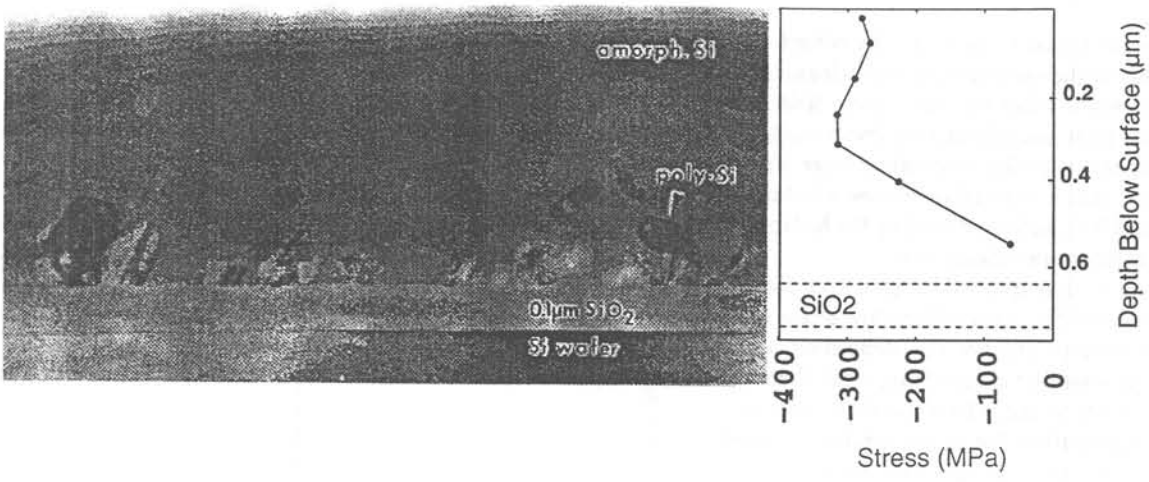

Fig. 4. TEM of structural polysilicon. Morphology vs stress before RTA. (courtesy: P. Krulevitch)

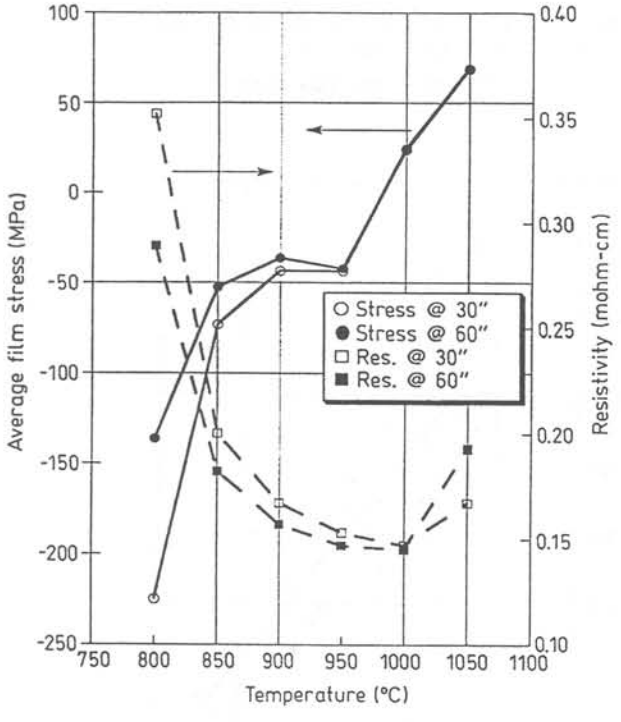

Fig. 5. Residual film stress and resistivity of phosphorus-doped polycrystalline silicon as a function of rapid thermal anneal time and temperature. Typical MICS RTA is 60 sec at 900 °C

outgassing during very high temperature annealing. We believe this to be the explanation for the resistivity increase measured for those wafers annealed at 1050 °C. Nominally, the structural *in situ* doped polysilicon resistivity was reduced from 1.211 mohm-cm +/− 0.008 mohm-cm (3σ) to values ranging from 0.15 to 0.35 mohm-cm with the 60 sec. anneals. The polysilicon recrystallization stress-relief anneal, as with all post-CMOS temperature excursions, is limited to rapid thermal annealing at 900 °C as a precaution against degrading the source/drain contact metallurgy and circuit device performance. The data shows that this temperature results in near tensile films with low bulk resistance. Optimization of the polysilicon deposition and annealing processes is on-going to achieve minimum stress gradient films. This effort is concentrating on changing the polysilicon deposition conditions in order to form films whose as-deposited stress is already tensile [Biebl and Mulhern (to be published)].

A consequence of the structural layer thickness is that conventional lithography and etching can be difficult to handle. With nominal thicknesses of 2 μm, the polycrystalline silicon requires particular attention during the plasma etch step because of the time required to clear any residual stringers. Photoresist masking typically cannot withstand the long etch times necessary, at times exceeding six minutes. Because of this, we have employed a non-erodible masking strategy for all thick structural polysilicon layers (SP2 and SP3). A 5000 Å PSG cap oxide film is deposited immediately after each mechanical polysilicon deposition. The following lithographic step is used then to pattern and etch this cap oxide in a fluorine-based plasma etch. The wafers are then directly transferred to a chlorine-based polysilicon etch having excellent selectivity to oxide. Sometime during this second etch the remaining photoresist is completely eroded, leaving the cap oxide to define the pattern transfer for the bulk of the polysilicon removal. Relatively good anisotropic polysilicon sidewalls are achieved with this etch sequence as can be seen by the cross-sectional scanning electron micrographs (Figs. 10, 11). Another advantage of this strategy is that the minimum polysilicon feature size is determined by the cap oxide lithography using 1.0 μm i-line photoresist rather than the much thicker resist that would be required if it were to have to act as the sole vehicle for pattern transfer.

The interconnect, contact metallurgies, and the passivating films must be robust to survive the relatively high MEMS fabrication temperatures. Potential problems associated with high temperature post-processing include interconnect metal hillock formation resulting in a compromised passivation integrity, S/D contact degradation, thin film blistering, and spin-on glass outgassing. Titanium silicide was chosen for contacts for its low contact resistance as well as for its stability up to 900 °C, being one of the only silicide metallurgies capable of withstanding temperatures in excess of 800 °C. Unfortunately the large barrier height of titanium silicide to p-type silicon

and the greater than 20% volumetric reduction during disilicide formation [Murarka (1983)] can cause problems both for the P+ S/D current-voltage linearity and metallization cracking within the contact regions. The latter problem can be somewhat curtailed by thinning down the as-deposited titanium to below 250 Å, which also prevents undue silicon consumption during the three-step silicidation. The silicide is formed with a 30 sec. RTA at 600 °C in nitrogen followed by an ammonium hydroxide ($NH_4OH:H_2O_2=3:1$) strip which removes all the unreacted titanium from the oxide regions. Finally, a 30 sec. RTA at 900 °C in argon is used as a contact resistance reduction anneal. Four point probe resistance measurements of the titanium silicide process show there to be a four-fold reduction in contact silicide resistance with this final thermal treatment (from 21.0 $\Omega/\square$ +/− 4.0 $\Omega/\square$ to 4.9 $\Omega/\square$ +/− 1.5 $\Omega/\square$). To protect the S/D silicon and titanium silicide from diffusion related to the tungsten interconnect deposition, a 200 Å thick layer of reactively sputtered titanium nitride is deposited. This thin barrier layer is deposited from a pure titanium target in a plasma containing argon and nitrogen. The resulting film is then furnace annealed for 20 min. at 600 °C in nitrogen to fully react the material and stuff grain boundaries to eliminate any potential diffusion paths. P+ and N+ electrical contact resistances are measured using conventional 3 μm × 3 μm Kelvin contact structures, and found to be 30–90 ohms and 10–50 ohms respectively immediately after the tungsten metallization forming gas sinter.

Tungsten was chosen for the interconnect metal because of its high melting point of 3410 °C and relatively low resistivity of 5.64 μohm-cm (as compared to aluminum at 2.66 μohm-cm and copper at 1.68 μohm-cm). Because tungsten can oxidize in air at temperatures exceeding 400 °C, care must be taken when performing pre-passivation thermal treatments such as the stress-relieving RTA or sinter steps, which are done in well purged argon and forming gas environments respectively. As with the passivation and structural layers, the metallization must have low intrinsic residual film stress to avoid delamination or hillock formation. Experiments comparing our in-house dc-sputtered tungsten with that obtained using chemical vapor deposition have indicated that CVD tungsten has significantly lower as-deposited stress than does the sputtered film. Two CVD gas chemistries were investigated: silane and hydrogen reduction of WF_6. The former, at 300 °C, is normally used as a nucleation layer because of the potential for aggressive reactions with silicon in the contacts when using the hydrogen-reduced process. Hydrogen reduction at 490 °C results in lower stress, and as such, is used for the bulk layer. Typical values for as-deposited films were +730 MPa, −65 MPa, and +850 MPa for the silane CVD, hydrogen CVD and sputtered films respectively. Post-deposition stress relief RTA at 900 °C resulted in all films being tensile at +235 MPa, +150 MPa, and +480 MPa respectively. Figure 6, an SEM cross-section through a transistor after the structural ground-plane/interconnect (SP1) etch, shows how dc-sputtered tungsten hillocks might compromise the passivation integrity by preventing adequate coverage by the silicon nitride. Because of this, we have been forced to use a precautionary photoresist mask to protect the circuitry during the release etch process (SREL mask). This is not necessary with the flatter CVD tungsten films. Figure 7 compares the stress-induced hillock formation in the as-deposited

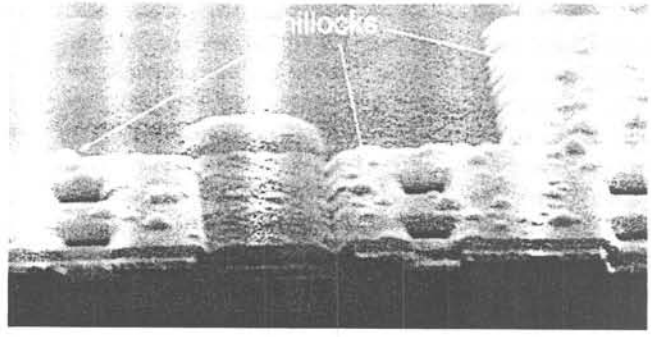

Fig. 6. SEM showing transistor cross-section with dc-sputtered tungsten hillocks protruding from underneath the passivation layers

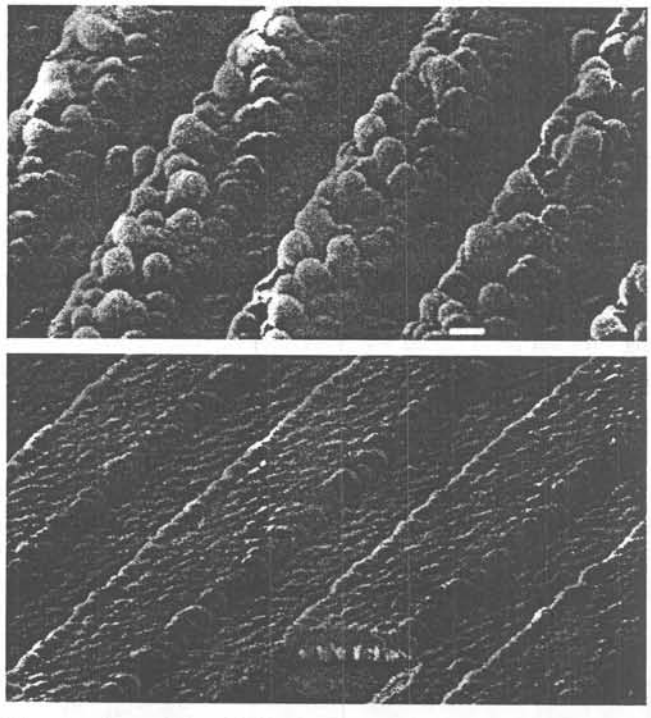

Fig. 7a, b. Stress-induced hillocks in as-deposited tungsten thin-films. a dc magnetron sputtered tungsten; b chemical vapor deposition using hydrogen-reduced WF_6

sputtered film with that deposited using CVD. The SEM micrographs were taken after the 450 °C PSG and 835 °C nitride passivation depositions, and show patterned 3.0 μm lines of 5000 Å thick tungsten. The size of the hillocks in the sputtered film are comparable to the original film thickness, a testament to the amount of stress-relaxation. A reduction in hillock density and size is clearly observed with the CVD deposition process. These results would indicate that substituting sputtered tungsten for a combined silane and hydrogen reduced CVD process would greatly minimize potential film stress problems, which must be controlled for all thin-films used in order to prevent subsequent blistering as thicker structural layers are deposited. Further technology development will be in this direction.

Although many integrated MEMS devices using the MICS process rely on only two sensor polysilicon layers; the ground

plane/interconnect (SP1) and one 2.0 μm structural polysilicon layer (SP2), more complex mechanical devices use a second 1.0 μm structural polysilicon layer (SP3). The addition of this third polysilicon complicates the MEMS fabrication sequence somewhat because of planarization issues in dealing with the very high aspect ratios involved. At this stage in the production flow, typical aspect ratios of the mechanical device can approach 2:1 with 4 μm features separated by 2 μm spaces. Figures 8 and 9 illustrate keyhole formation between SP2 interdigitated fingers during the nonconformal sacrificial PSG deposition and the resulting SP3 stringers remaining after the SP3 removal. Planarization of the inter-polysilicon sacrificial dielectric layer is needed in order to avoid this stringer formation. We have found that a siloxane-type spin on glass (SOG), along with an intermediate dielectric layer and an isotropic etch-back, provides adequate filling of 2 μm-deep trenches in the patterned first structural polysilicon layer (SP2). Subsequent sacrificial PSG layers of 2–3 μm can then be deposited without initiating keyhole formation. Unlike conventional applications for SOG, we require only that the film act as a temporary trench filling agent, to be capped by other sacrificial glass material and later removed from under the structural polysilicon during the release etch step. Thick crack-free SOG requires that careful attention be paid to the application and cure steps. The high viscosity SOG used in this step had a 14% organic content and spun to thicknesses of 5000 Å. Typical quoted volumetric shrinkage after a 425 °C cure was 4% (manufacturer supplied product literature). Multiple coating with hot plate curing was necessary to achieve an adequate thickness to planarize the MEMS structures. The four step process as implemented consisted of a thin LPCVD PSG interdielectric layer in order to cover the exposed polysilicon (SP2), two coats of hot plate cured SOG (one minute each at 90 °C, 150 °C, and 250 °C), a 60 min. furnace cure at 425 °C in nitrogen, and an isotropic SF_6 plasma etchback. The last step was done to both smooth the surface topography and reduce the amount of SOG that required etching during the SP3 to SP2 anchor contact cut. Figure 10 shows the SP2 trenches formed by the interdigitated fingers of the comb-drive structure after the SOG etch-back step (10a) and after the planarization process (10b), where the SOG has been etched back from the cleave edge with HF in order to enhance the SEM contrast. Figure 11 is an SEM of a released triple polysilicon MEMS structure with SP1 circuit-to-structure runners, SP2 interdigitated comb drives, suspension springs, fuses, mechanical plate, SP3 upper electrode, and dimpled limit stops. Note that there are no SP3 stringers present at the comb drive. Etch holes, allowing hydrofluoric acid access to the sacrificial PSG underlying both structural layers, are visible. SP3-to-SP2 and SP2-to-SP1 anchors (SG2 and SG1 masks respectively) are also depicted.

Unfortunately, the cure temperatures of 400–450 °C may not be sufficient to fix the SOG for the final PSG and polysilicon processing, since these steps require temperatures up to 900 °C. As a result, the SOG encapsulated by the final sacrificial PSG can undergo further volumetric reductions and outgas more of its organic consitutent. We have seen "whisker-like" stringers left behind after the sacrificial HF release etch step at the periphery of enclosed SP2 features. We attribute these to residual organic material and managed to remove them with extended sulfuric peroxide acid treatments after release. Further investigation is underway to study this residual organic contaminant, the SOG adhesion to underlying dielectric, proper curing of the multiple SOG layers to prevent cracking, and the SOG dissolution rate in hydrofluoric acid. Our process requires that the sacrificial layer etch rapidly in hydrofluoric acid. As a result, the SOG is applied directly onto a heavily phosphorus-doped interdielectric PSG layer rather than an undoped LTO layer. Adhesion problems of the siloxane-based SOG to the heavily doped dielectric glass [Gupta (1989)] were not observed. Slight adjustments could however be made to the doping level of the thin interdielectric layer if adhesion became an issue.

The final steps in the structural fabrication sequence involve releasing the polysilicon structures by dissolving the sacrificial phosphosilicate glass in aqueous hydrofluoric acid. After release, the structures must be carefully dried to prevent "stiction",

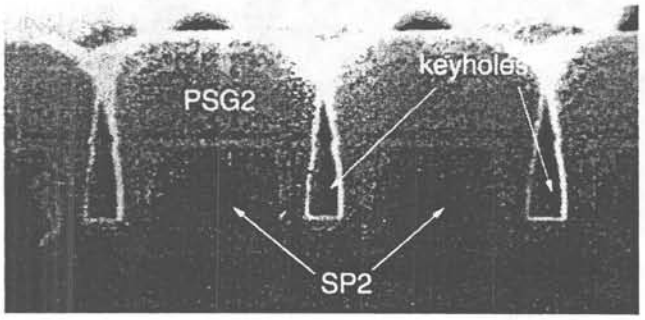

Fig. 8. SEM of high aspect ratio structural polysilicon (SP2) after the sacrificial PSG2 deposition, showing keyholes resulting from the nonconformal CVD process

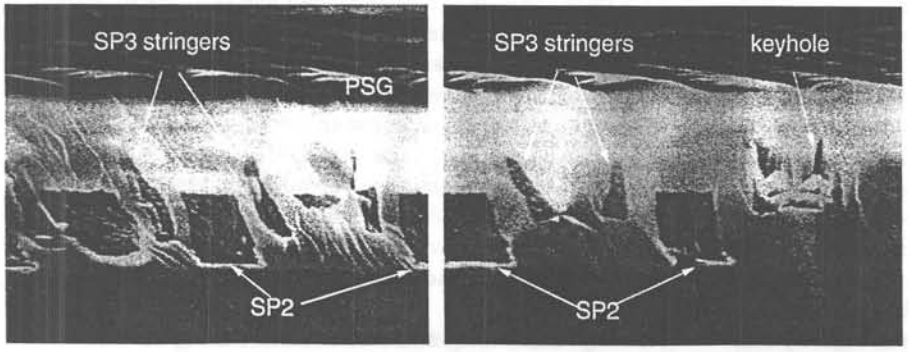

Fig. 9. SEM examples of adjacent SP3 stringers

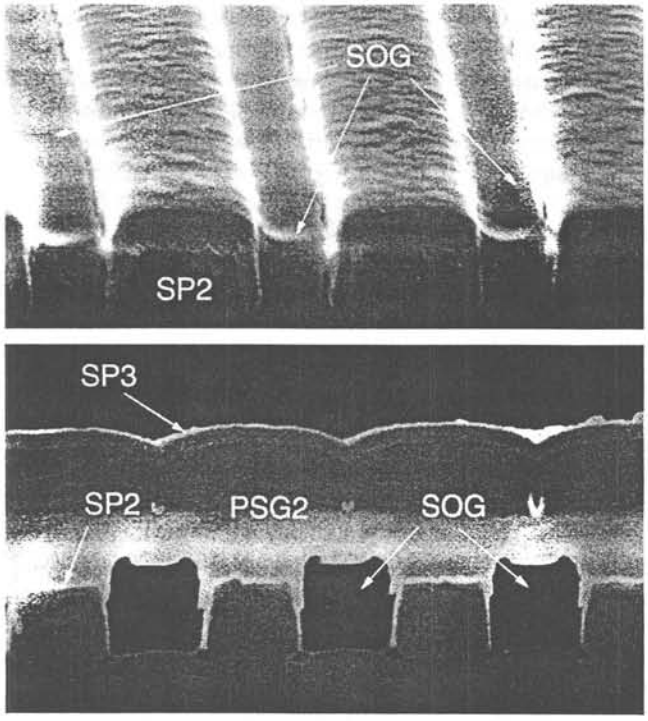

Fig. 10. a SOG-filled trenches after the etch-back planarization; b completed planarization with SP3

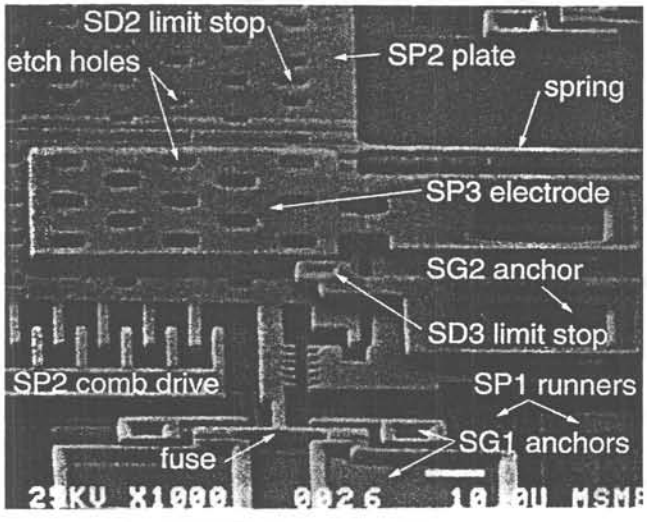

Fig. 11. SEM of planarized three-polysilicon structure

which is caused by the attractive surface tension forces of interfaces with the rinse liquid. This phenomena results in the mechanical structures being permanently adhered to the underlying substrate. At this time there are four methods commonly used to execute the drying step of the microstructure release: simple air or infrared heat-lamp drying, vacuum sublimation drying such as was attempted with t-butyl alcohol or methanol-water mixtures [Inoue and Osatake (1988), Guckel et al. (1989)], temporary polymeric supporting members which are later plasma removed as was reported by Mastrangelo and Saloka (1993) when they used parylene as an intermediate support structure during the HF sacrificial etch, or supercritical drying of hydrophilic passivated structures as was pioneered for MEMS devices by Mulhern [Mulhern et al. (1993)]. Yields with the first method are very low unless some form of fusible link anchor structure is designed to hold the MEMS device in place during release and packaging [Fedder et al. (1992)]. The second method has proved impractical for wafer-level processing, primarily because of the long sublimation times required for wafer-sized samples. Temporary polymeric supporting structures is a viable method, and may be implemented in future MICS work.

At this time the MICS technology uses the supercritical drying technique with CO_2 as the supercritical fluid because of its relatively low supercritical pressure (1073 psi) and temperature (31.1 °C). Four steps are involved in the release/drying process. The release is accomplished by immersion in 5 : 1 buffered HF for enough time to completely undercut 10 μm of phosphosilicate glass from beneath the structural members. Substrate and structures are then passivated by immersion in a sulfuric peroxide solution, resulting in hydrophilic silicon surfaces. Both acid treatments are followed by thorough deionized water rinses. The last rinse is a methanol soak used to displace the water prior to entering the supercritical drying chamber. Finally, the wafer is loaded into a pressure vessel where the methanol is completely displaced by liquid CO_2 at 1200 psi. Drying takes place by passing from the liquid phase to the gas phase through the supercritical region. Refer to Fig. 12 for the phase diagram of supercritical CO_2. First the vessel is heated until the liquid CO_2 makes the transition to the supercritical phase. Venting the vessel to rapidly reduce the pressure isothermally above the CO_2 supercritical temperature results in dried "stiction-free" surfaces. Because the liquid-to-vapor transition occurs in the supercritical region, there are no attractive capillary forces to cause "stiction".

In contrast to the interleaved MEMS processes using aluminum metallization, which requires protection of the aluminum from the HF etchant, the passivated tungsten-metallized CMOS does not require a protective photoresist mask over the circuit area during the final release etch. Similarly, the supercritical CO_2 drying process avoids the polymeric application necessary for the parylene pedestal stiction prevention

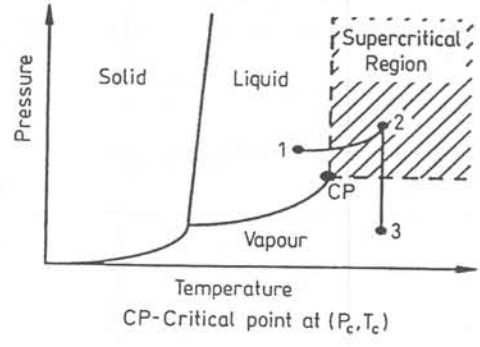

Fig. 12. Phase diagram of a supercritical fluid. Exchange methanol with liquid CO_2 at 20 °C and 1200 psi; 1–2 close off vessel and heat liquid CO_2 to a supercritical fluid. There is no interface formed during this transition; 2–3 Vent vessel at a constant temperature above T_c. The CO_2 exits in gaseous form (courtesy: G. Mulhern)

technique. As a result, the polysilicon surfaces are not subject to organic contamination and can be passivated using oxidizing solutions such as sulfuric-peroxide.

Having a standardized front-end CMOS technology with repeatable parametric control is routinely accomplished by using a 3 µm p-well baseline CMOS technology for the electronics. As previously mentioned, the CMOS is fabricated as a pre-structural module. Only at metallization does the MICS technology deviate from that of conventional single-metal CMOS. Because of the high temperature back-end microstructural processing, it is necessary to monitor basic transistor parametrics in-line immediately after the post-metallization forming gas sinter and again during the structural fabrication. Comparing these parametric measurements gives us insight on how to modify those CMOS fabrication steps that determine device performance in order to compensate for parametric shifts that might occur because of dopant redistribution. Figure 13 shows how the post-CMOS thermal cycling results in reduced saturated drain current for the CMOS devices – in this case for the 25/3 N-channel (13 a) and P-channel (13 b) devices as measured on

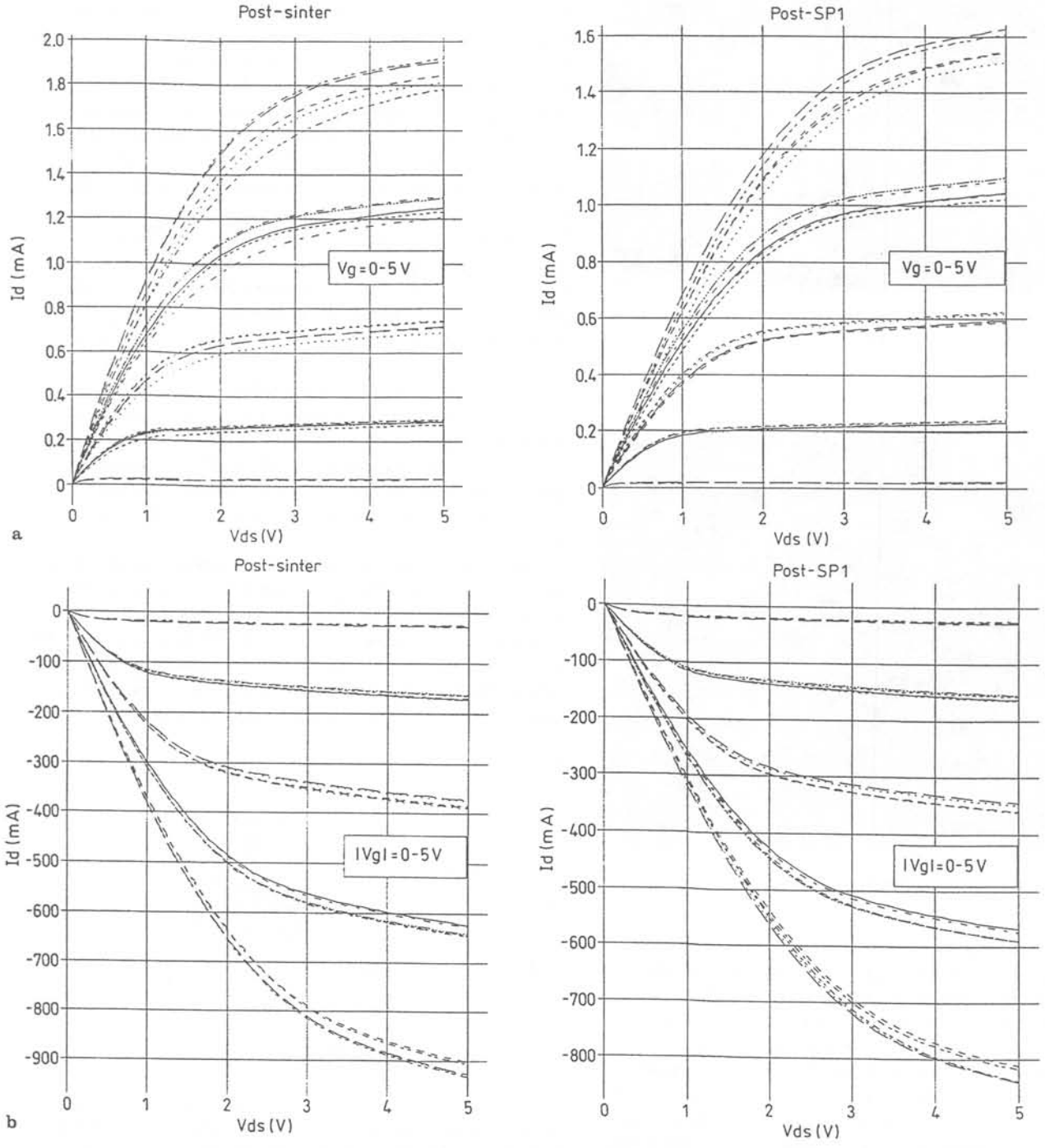

Fig. 13. a N-ch parametric drift; b P-ch parametric drift

five sites (T, C, B, L, R) across one fabricated wafer. Typical post-sinter values for these devices are 1.85 mA (N-ch) and 0.93 mA (P-ch). After processing through the first structural polysilicon, these values reduce to 1.55 mA and 0.84 mA respectively. Although not a major problem for the performance of the final electro-mechanical system, this drift might be minimized by a reduction in the back-end thermal cycling and/or better front-end optimization of CMOS channel doping. Other parametrics, such as contact resistance, were not measured during the structural fabrication because electrical test structure limitations did not allow access post-CMOS. Future mask designs will allow for complete parametric testing, both at the CMOS sinter step, and in-process during the back-end structure fabrication steps – namely after the SP1 and SP2 etches.

By using a common baseline fabrication process, a variety of integrated MEMS can be fabricated using the MICS technology on a single multiproject chip. Figure 14 is a die-photo of a completed MICS die with several MEMS devices being fabricated simultaneously. Some, such as the gyroscopes and electrostatic voltmeter require three levels of structural polysilicon (through SP3), while devices such as the accelerometer and resonant tuning fork oscillators require only two (up to SP2). Since the three-polysilicon micromechanical process simply extends the two-polysilicon process by a few extra modules, they can be fabricated together with relative ease. Proceeding on to complete the SP3 modules does not jeopardize the SP2 MEMS structures. Also worthy of mention is the extensive set of device characterization test structures that accompany each run. By employing the modularized concept and separating the electronics fabrication from the mechanical fabrication, two foundries, each with specialized process control, might participate in the overall fabrication of the final MEMS product.

The post-CMOS microstructure process has been characterized by a set of geometrical design rules (GDR) and process

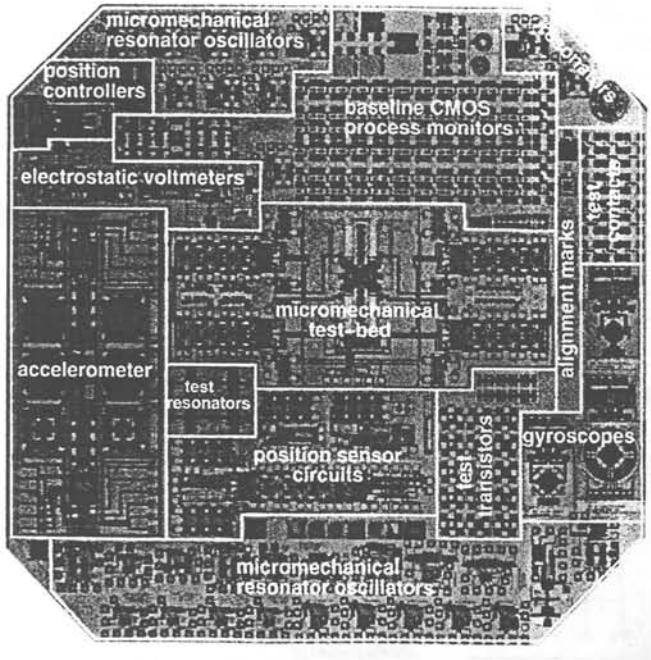

Fig. 14. Optical photograph of multi-project integrated MEMS chip

SP2/SP1 Contact (SG1)

a) Minimum contact size	5.0
b) Minimum contact to contact space	2.0
c) SP2 overlap of contact	2.0
d) SP1 overlap of contact	2.0
e) Minimum SP2/SP1 to SP1/CPG contact space	4.0
f) Stacked SP2/SP1 and SP1/CPG contacts permitted	

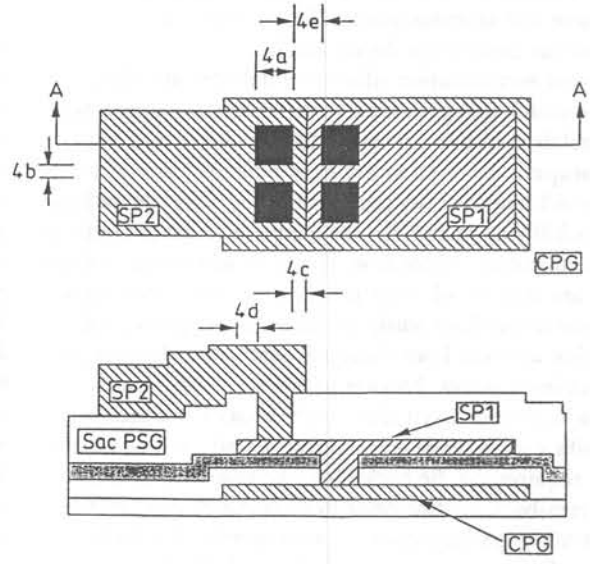

Fig. 15. Geometrical design rules for baseline MICS

parameters in order to maximize yields and improve robustness. All MEMS included in the multiproject chip must conform to certain geometrical layout constraints pertaining to the mechanical design. These constraints have been developed to avoid problems associated with the high aspect ratio, plasma etching, and layer-to-layer overlap of the relatively thick structural films. These GDRs have been defined for every step in the back-end MICS process, an example of which is illustrated in Fig. 15, where the SP2 to SP1 anchor contact is shown in its relation to the SP1 to CPG structure-to-circuit interface contact.

4
Packaging issues

Effective and reliable packaging remains an area requiring attention. Vacuum encapsulation is desirable for high mechanical quality factor and thermal noise minimization. Integrated micro-vacuum shells may be feasible in the MICS process. This process was first demonstrated for bulk micromachined microlamp devices by Mastrangelo [Mastrangelo and Muller (1993)] where polysilicon filaments were encased by an optically transparent low-stress silicon nitride film. Holes were cut in the nitride film to allow the removal of the bulk silicon using an anisotropic potassium hydroxide etchant. Finally, the evacuated shells were placed once again in the low-stress nitride deposition furnace to seal the etch holes. During the pumpdown step of the LPCVD operation the shells were evacuated to a pressure of 300 mT prior to deposition and encapsulation. Later attempts by Lin and McNair [Lin et al. (1993)] expanded this technique to surface micromachined

devices covered with thick PSG platforms. Opening etch holes in the nitride, removing the sacrificial glass, and resealing the holes with nitride, produced a fully encapsulated MICS resonator, which operated at the reduced pressure. Improvements to the silicon-rich nitride LPCVD deposition equipment and process allowed these shells to achieve inside pressures of 140 mT. One clear disadvantage to this approach is the limitation placed on minimum achievable inner shell pressure, determined by the LPCVD process. Also, while sealing the shell, reactant gasses (i.e. dichlorosilane and ammonia) enter the shell and can compromise the mechanical device inside.

Our current encapsulation efforts use industry standard eutectic die-attach and gold/tin lid sealing under vacuum with conventional dual in-line packages. To this end, a dedicated vacuum encapsulation station has been built that provides a minimum achievable cavity pressure of 6 E-7 Torr and package heating capability up to 400 °C – the temperature range required for die attach and lid solder flow. The basic advantages behind this effort are that the ultimate pressure inside the evacuated cavity is now determined solely by the vacuum system, and encapsulation ambient limitations are eliminated allowing for sealing with inert gasses. Because packaging temperatures exceed 300 °C, conventional silver paste epoxy die attach is replaced with a more stable gold eutectic die-attach. The eutectic die-attach requires the die backside to be silicon. A backside strip and etch-back module prior to release etch can provide bulk substrate-to-package contact. Alternatively, the thick structural polycrystalline can simply be left behind.

The three step vacuum packaging module immediately follows the supercritical CO_2 drying step, which ensures that the backside silicon is clean and oxide free. The die is placed in a ceramic dual inline package with an intermediate gold/silicon foil (98% Au/2% Si), and heated to 375 °C allowing the die, foil, and package to form a strong eutectic bond. At this time, the die is wire-bonded to the package leadframe with an ultrasonic aluminum wire bonder. Afterwards, an EPROM-like quartz windowed lid with a gold/tin (80% Au/20% Sb) preform is placed over the die cavity and held in place with a spring-loaded clip. The capped package is then placed in a quartz ampoule and evacuated to the desired base pressure, allowing sufficient time for the pressure inside the cavity to equilibrate with that of the vacuum system. A final anneal at 375 °C sweats the Au/Sb perform and seals the lid to the package.

An alternative wafer-level post-release packaging scheme might be to use silicon-to-glass anodic bonding with etched Pyrex™ capping wafers having recessed cavities and access to metalized bondpads on the device wafer [Fung et al. (1985)]. This technique would provide the flexibility of vacuum and ambient control as well as the convenience of wafer-level encapsulation ("packaging") that could then be transferred to any type of chip carrier.

5
Selected applications

Although post-CMOS fabrication of integrated microstructures does not allow for the simultaneous optimization of circuit and structural processes, the MICS process is capable of successful fabrication of functional CMOS interface electronics and polysilicon microstructures – the building blocks for a large class of MEMS. Projects currently being fabricated with the MICS process include the micromechanical resonator oscillator, and the integrated MEMS test-bed. Initial motivation for these devices was derived by the integration of suspended polysilicon plates and CMOS electronics for a digital force-balanced accelerometer [Yun et al. (1992)]. Figure 16 shows this device with its movable sense capacitors and fixed reference capacitor. The detection circuitry in the center consists of low-input capacitance buffers, a variable gain amplifier, demodulator, cosine filter, bias circuits, and a 1-bit quantizer. The level of integration for this early device exceeded 500 transistors on-chip with the micromechanics. The overall die size was 12.5 mm^2.

Figure 17 shows an optical micrograph of a high-Q oscillator fabricated via the MICS process, utilizing a capacitively driven polysilicon micromechanical resonator and transresistance-based sustaining CMOS electronics [Nguyen and Howe (1993)]. This oscillator takes advantage of the high Q of the polysilicon resonator, with frequency ranges from 100 Hertz to tens of megahertz, and measured Q's of 50000 for 100 kHz (unbalanced) while operated under vacuum. The oscillator shown has a 16.5 kHz center frequency and an oscillation amplitude determined by nonlinearities in the resonator. Higher frequency versions would require that the resonator design be significantly scaled down. These oscillators can be used for a myriad of applications such as: accelerometers, vapor or pressure sensors,

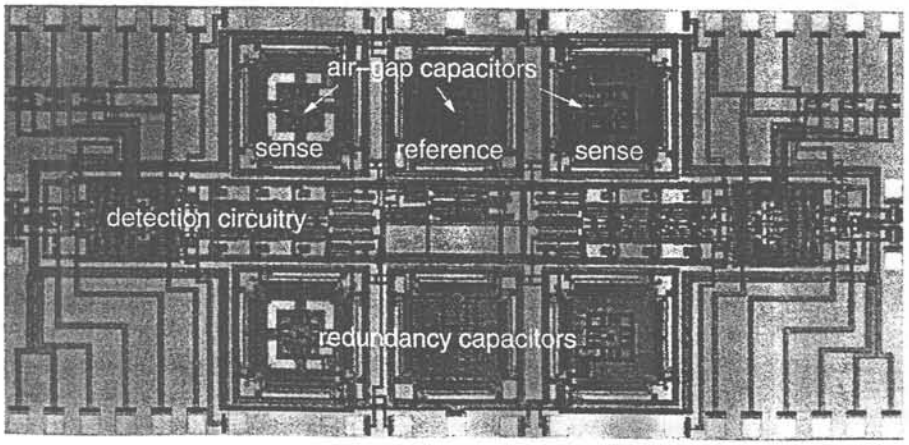

Fig. 16. Digitally forced-balanced accelerometer

instrumentation, or perhaps replacing off-chip quartz crystal oscillators in communications systems.

Figure 18 is an optical micrograph of an integrated test-bed for research in multi-mode digital control of MEMS: a suspended polysilicon plate having four capacitive-bridge vertical position sensors, each with an integrated CMOS buffer amplifier, and four differential electrostatic feedback actuators on the plate's corners [Fedder and Howe (1994)]. The integrated test-bed enables the experimental verification of models and simulations of general control strategies for a suspended plate with three degrees of freedom. Digital force-balance feedback is used to control each corner of the plate. In air, vertical displacement and tilt of the plate in two axes are controlled within $+/-25$ nm and $+/-0.03^{\circ}$, respectively. Eight buffer amplifiers, four variable gain differential amplifiers, and bias circuitry are included in the system. The upper feedback actuators are made from the second structural layer, and shown in Figure 11.

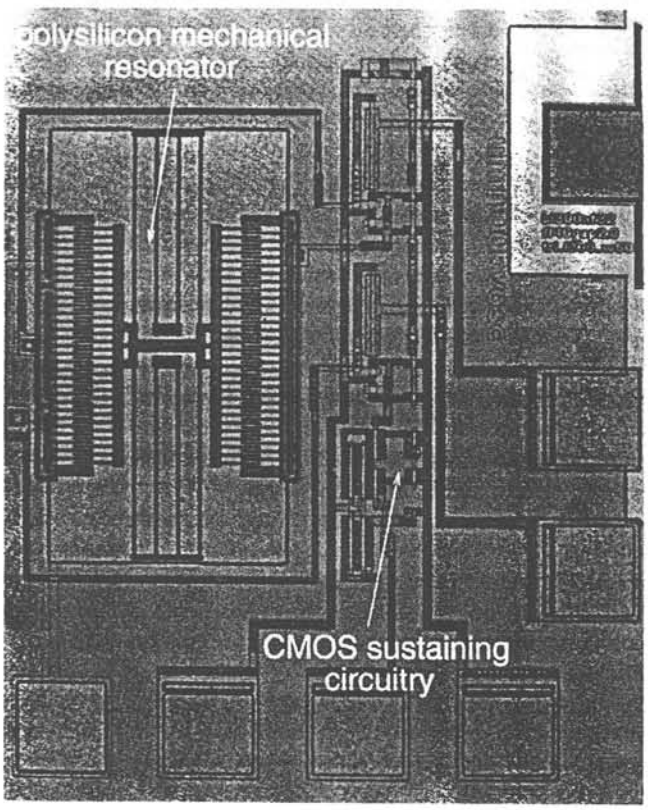

Fig. 17. High-Q micromechanical resonant oscillator

6 Conclusions

Combining IC designs and mechanical devices on the same chip using standard silicon-based technologies is a rapidly growing technology thrust that will provide low-cost manufacturing of MEMS. We have developed a surface micromachining technology fabricated in a post-CMOS modularized process that provides a technology platform for manufacture of a variety of surface-micromachined microelectromechanical systems. Our plan is to convert to an n-well CMOS technology in order to push transistor geometries and circuit performance and to switch to CVD tungsten to minimize the stress of our interconnect metallurgy. Further development resulting in additional scaling, improved signal to noise characteristics, and fabrication robustness will improve manufacturability and expand potential market applications of this technology.

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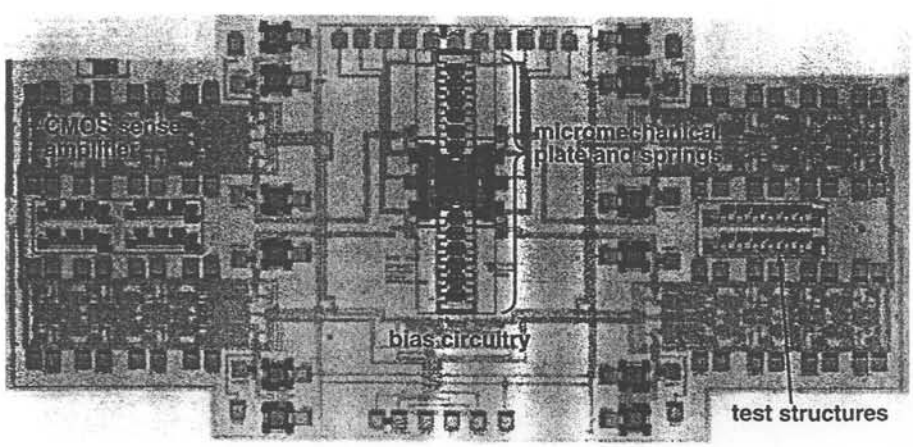

Fig. 18. Integrated testbed for multi-mode digital control

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