Analog Design Using \( g_m/l_d \) and \( f_t \) Metrics

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Overview

• Traditional analog design methodologies typically require iteration
  – "Square Law" design equations are inaccurate for submicron devices
  – Depend on poorly defined parameters: $\mu C_{ox}$, $V_{th}$, $V_{dsat}$, …
  – Difficult to achieve an “optimum” (e.g. minimum power)

• $g_m/I_d$-based design
  – Links design variables ($g_m$, $f_t$, $I_d$, …) to specification (bandwidth, power)
  – Employs design charts to accurately size transistors
Motivation: A design example

Specifications:

- Small signal gain: \( a_v = \frac{v_o}{v_i} = 5 \)
- Bandwidth: \( B \geq 10 \text{MHz} \)
- Source resistance: \( R_s = 1 \text{M} \Omega \)
- Load capacitance: \( C_L = 5 \text{pF} \)
- Minimum power dissipation
Design Approaches

Design equations (Square-Law model)

\[ I_d = \frac{1}{2} \mu C_{ox} \frac{w}{L} (V_{GS} - V_{TH})^2 \]
\[ g_m = \mu C_{ox} \frac{w}{L} (V_{GS} - V_{TH}) \]
\[ C_{GS} = C_{ox} WL \]

etc. ... 

Difficulties

- Sub-micron transistors are not well described by these equations
- Non-obvious relation of model parameters to design specification
- Leads to many iterations
- What is the minimum power, anyway?
Natural Variables for Analog Design

- Transconductance: \( g_m \)
- Current: \( I_d \)
- Efficiency: \( g_m/I_d \)
- Capacitance: \( C_{gs}, \ldots \)
- Transit frequency: \( f_t = g_m/2\pi C_{gs} \)
Example

Design constraints

- Low frequency gain: \( a_v = g_m R_L \)
- Pole at input: \[ |p_{in}| = \frac{1}{R_s C_{gs}} \geq \frac{1}{2\pi B} \]
- Pole at output: \[ |p_{out}| = \frac{1}{R_L C_L} \geq \frac{1}{2\pi B} \]

Specifications:

- Small signal gain: \( a_v = v_o/v_i = 5 \)
- Bandwidth: \( B \geq 10\text{MHz} \)
- Source resistance: \( R_s = 1\text{M\Omega} \)
- Load capacitance: \( C_L = 5\text{pF} \)
- Minimum power dissipation

\[ g_m \geq 2\pi B C_L \]
\[ C_{GS} \leq \frac{1}{2\pi B R_s} \]
minimize \( I_d \)
Design Constraints and Objectives

Design constraints

\[ g_m \geq 2\pi B C_L = 1.57 \text{ mS} \]

\[ C_{GS} \leq \frac{1}{2\pi B R_s} = 16 \text{ fF} \]

minimize \( I_d \)

Design objectives

1. High current efficiency to minimize power

\[ \frac{g_m}{I_d} \]

2. Small \( C_{gs} \) \( \rightarrow \) high \( f_T \) to meet bandwidth constraint

\[ f_T = \frac{g_m}{2\pi C_{gs}} \]
Transit Frequency $f_T$

**Compromise**
- high $g_m/I_d$ for low power
- high $f_t$ for low $C_{gs}$

**Design choice**
- Maximum $C_{gs}$ to meet specification at minimum power:
  - minimum $f_t$
  - minimum $L$
  - maximum $g_m/I_d$

\[
f_{t,\text{min}} = \frac{g_{m,\text{min}}}{2\pi C_{gs,\text{max}}} = 15.7 \text{ GHz}
\]
Transistor Current Efficiency $g_m/I_d$

- **Strong Inversion**
  - Poor current efficiency
  - Low output voltage range
- **Weak Inversion**
  - Good current efficiency (low $V_{d\text{sat}}$)
  - High output voltage range
- **High $f_t$**
- **Small transistor**
- **Low $f_t$**
- **Large transistors**
Completing the Design: Transistor Sizing

\[ \frac{g_m}{I_d} = 14 \, \text{V}^{-1} \text{ and } f_T = 16 \, \text{GHz} \]

\[ I_d = \frac{g_m}{g_m/I_d} = 112 \, \mu\text{A} \]

\[ \frac{I_d}{W} = 12.4 \, \frac{\text{A}}{\text{m}} \text{ (from chart)} \]

\[ W = \frac{I_d}{I_d/W} = 9 \, \mu\text{m} \]
Verification: (1) Bias

Analog design using $g_{m}/I_{d}$ and $f_{t}$ metrics
Verification: (2) Specification

- Bias is as designed
- Gain and bandwidth slightly below spec
- Design ignored transistor $r_o$ and self-loading
- Adjust by choosing a slightly higher $f_t$
## Summary

<table>
<thead>
<tr>
<th>Silicon</th>
<th>SPICE Model</th>
<th>“Square Law” based design</th>
<th>$g_m/l_d$ based design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complicated Physics</td>
<td>Complicated Equations (BSIM, PSP, …)</td>
<td>Simple “Square Law” Equations</td>
<td>$g_m/l_d$ &amp; $f_t$ Charts (process specific)</td>
</tr>
</tbody>
</table>

- **Silicon**
  - Accurate
  - Good for verification
  - Unsuitable for design

- **SPICE Model**
  - Complicated Physics

- **“Square Law” based design**
  - Simple
  - “Square Law” Equations

- **$g_m/l_d$ based design**
  - Good accuracy
  - Simple equations
  - Transistor data from charts

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Analog design using $g_m/l_d$ and $f_t$ metrics
NMOS Transit Frequency $f_T$

Analog design using $g_m/I_d$ and $f_T$ metrics

$12V^{-1}$, 19.5GHz

$L_n=180\text{nm}$
$L_n=250\text{nm}$
$L_n=350\text{nm}$
$L_n=500\text{nm}$

$g_m/I_d$ [1/V]

$[2\pi f_T]$
PMOS Transit Frequency $f_T$

![Graph showing PMOS Transit Frequency $f_T$ vs. $-g_m/I_d$ for different $L_p$ values with annotations for $8V^2$, 3.80GHz]
Extrinsic Capacitances $C_{gd}$ and $C_{dd}$

**NMOS**

$$\frac{C_{gd}}{C_{gg}} \text{ and } \frac{C_{dd}}{C_{gg}}$$

**PMOS**

$$\frac{C_{gd}}{C_{gg}} \text{ and } \frac{C_{dd}}{C_{gg}}$$

Legend:
- $L_n = 180\,\text{nm}$
- $L_n = 250\,\text{nm}$
- $L_n = 350\,\text{nm}$
- $L_n = 500\,\text{nm}$
NMOS Current Density

![Graph showing NMOS Current Density](image)

- $I_d/W$ [A/m] vs. $g_m/I_d$ [1/V]
- Lines represent different values of $L_n$: $L_n=180nm$, $L_n=250nm$, $L_n=350nm$, $L_n=500nm$
- Annotation: $12V^{-1}$: 19.4A/m
PMOS Current Density

Analog design using $g_m/I_d$ and $f_t$ metrics
NMOS Intrinsic Gain $g_m r_o$

Analog design using $g_m/I_d$ and $f_t$ metrics
PMOS Intrinsic Gain $g_m r_o$

Analog design using $g_m/I_d$ and $f_t$ metrics
Intrinsic Gain $g_m r_o$

**NMOS**

- $g_m r_o$ vs. $v_{ds}$ for different $L$ values:
  - $L=180\text{nm}$
  - $L=250\text{nm}$
  - $L=350\text{nm}$
  - $L=500\text{nm}$

- Key points:
  - $L=180\text{nm}$: $v_{ds} = 100\text{mV}$, $g_m r_o = 41.5$
  - $L=350\text{nm}$: $v_{ds} = 300\text{mV}$, $g_m r_o = 16.0$

**PMOS**

- $g_m r_o$ vs. $v_{ds}$ for different $L$ values:
  - $L=180\text{nm}$
  - $L=250\text{nm}$
  - $L=350\text{nm}$
  - $L=500\text{nm}$

- Key points:
  - $L=180\text{nm}$: $v_{ds} = 100\text{mV}$, $g_m r_o = 51.9$
  - $L=350\text{nm}$: $v_{ds} = 200\text{mV}$, $g_m r_o = 17.2$
OTA Design Example

Specifications

- Voltage gain \( A_v = 2 \)
- Dynamic range \( DR \geq 72\text{dB} \)
- Settling accuracy \( \epsilon_d \leq 100\text{ppm} \)
- Settling time \( t_s \leq 10\text{ns} \)

- Switched capacitor gain stage (switches not shown)

- Applications: A/D converters, filters, …
Circuit Topology

- Fully differential OTA
- Common mode and cascodes (for gain) not shown
- Differential mode half circuit
- Large & small signal models

Analog design using $g_{m}/I_d$ and $f_t$ metrics
Design Flow

1. Determine feedback factor
2. Determine $C_L$ to meet dynamic range requirement
3. Determine $g_m$ to meet settling requirement
4. Pick transistor characteristics based on analysis
   – Channel length $L$
   – Current efficiency $g_m/I_D$ (or $f_t$)
5. Determine bias currents and transistor sizes
   – $I_D$ (from $g_m$ and $g_m/I_D$)
   – $W$ (from $I_D/W$, current density chart)
(1) Feedback Factor

- Open feedback loop
  \[ \beta = \frac{V_x}{V_o} = \frac{C_f}{C_f + C_s + C_x} = \frac{1}{1 + A_v + \frac{C_x}{C_f}} \]

- \( C_x \) is amplifier input capacitance (\( C_{gs} + \ldots \))
  - Small \( C_x \) \( \rightarrow \) large feedback factor \( \beta \)
  - Large \( C_x \) \( \rightarrow \) low transistor \( f_t \) requirement \( \rightarrow \) higher \( g_m/l_d \) \( \rightarrow \) reduced current
  - Typically \( C_x = (\frac{1}{3} \ldots 1) \times (C_s + C_f) \) (shallow optimum)
(2) Dynamic Range

Output resistance: \( R \approx \frac{1}{\beta g_{mn}} \)

Noise density:
\[
\frac{V^2_{o,n}}{\Delta f} = 4kT \gamma g_{mn} \left( 1 + \frac{g_{mp}/I_d}{g_{mn}/I_d} \right) \cdot \frac{R}{1 + j\omega RC_{Ltot}}^2
\]

choose \( \frac{g_{mp}}{I_d} < \frac{g_{mn}}{I_d} \) for low noise

Sampled noise:
\[
\overline{v^2_{o,n}} = \frac{1}{\beta} \frac{kT}{C_{Ltot}} \gamma \left( 1 + \frac{g_{mp}}{g_{mn}} \right)
\]

with \( C_{Ltot} = C_L + (1 - \beta)C_f \)

Dynamic range:
\[
DR = \frac{\frac{1}{2} V^2_{o,max}}{V^2_{o,n}}
\]

Minimum load capacitance:
\[
C_{Ltot} \geq 2kT \frac{\gamma}{\beta} \left( 1 + \frac{g_{mp}}{g_{mn}} \right) \frac{DR}{V^2_{o,max}}
\]
(3) Settling

Step response: $v_{out}(t) = V_{step} \frac{C_S}{C_f} \cdot \frac{T_0}{1 + T_0} \cdot (1 - e^{-t/\tau})$

with $\tau = \frac{C_{Ltot}}{\beta g_{mn}}$

Solve for transconductance: $g_{mn} \geq -\frac{C_{Ltot} \ln \varepsilon_d}{\beta t_s}$
(4) Transistor Channel Length, $g_m/I_d$ and $f_t$

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$L$</td>
<td>180 nm</td>
<td>250 nm</td>
<td>$L_{n,\text{min}}$ reduces power</td>
</tr>
<tr>
<td>$g_m/I_d$</td>
<td>12 V$^{-1}$</td>
<td>8 V$^{-1}$</td>
<td>$g_{mp}/I_d &lt; g_{mn}/I_d$ (noise)</td>
</tr>
<tr>
<td>$f_t$</td>
<td>19.7 GHz</td>
<td>3.78 GHz</td>
<td>$C_{gsn} &lt; C_s + C_f$</td>
</tr>
<tr>
<td>$I_d/W$</td>
<td>18.7 A/m</td>
<td>7.06 A/m</td>
<td></td>
</tr>
</tbody>
</table>

- Reduce $g_m/I_d$ of NMOS if $C_{gsn} < C_s + C_f$
- $f_t$ and $I_d/W$ obtained from charts
### (5) Bias Currents and Transistor Sizes

#### Specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic range</td>
<td>DR = 6.12 dB</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>( f_s := 50, \text{MHz} ) ( t_s := \frac{1}{2 \cdot f_s} ) ( t_s = 10, \text{ns} )</td>
</tr>
<tr>
<td>Closed-loop gain</td>
<td>( A_{vo} = 2 )</td>
</tr>
<tr>
<td>Settling accuracy</td>
<td>( e := 2^{-13} \quad e = 122.07 , \text{ppm} \quad e_d := 100, \text{ppm} )</td>
</tr>
<tr>
<td>Supply voltage (min)</td>
<td>( V_{dd} = 1.8, \text{V} )</td>
</tr>
<tr>
<td>Sampling cap</td>
<td>( C_s := 200, \text{fF} \quad \text{e.g., matching} \quad C_f := \frac{C_s}{A_{vo}} )</td>
</tr>
</tbody>
</table>

#### Design

- Feedback factor:
  
  \[
  \beta := \frac{1}{1 + A_{vo} + \frac{C_x}{C_f}} \quad \beta = 0.222
  \]

- Dynamic range:
  
  \[
  V_{\text{omax}} := 0.6\, \text{V} \]

  \[
  C_{L_{\text{tot}}} := 2 \cdot k_B \cdot T_r \cdot \frac{1}{\beta} \left( 1 + \frac{\text{gm}_{idp}}{\text{gm}_{idn}} \right) \cdot \frac{10.1 \cdot \text{DR}}{V_{\text{omax}}^2}
  \]

  \[
  C_{L_{\text{tot}}} = 2.644\, \text{pF}
  \]

  \[
  \sigma_{mn} := \sqrt{\frac{2 \cdot k_B \cdot T_r \cdot \frac{1}{\beta} \left( 1 + \frac{\text{gm}_{idp}}{\text{gm}_{idn}} \right)}{C_{L_{\text{tot}}}}} = 106.57\, \mu\text{V}
  \]

#### Transistor \( L_{gm/Id} \) (Guess)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length</td>
<td>( L_n := 180, \text{nm} ) ( L_p := 250, \text{nm} )</td>
</tr>
<tr>
<td>( gm/Id )</td>
<td>( \text{gm}<em>{idn} := 12 \cdot V^{-1} ) ( \text{gm}</em>{idp} := 8 \cdot V^{-1} )</td>
</tr>
<tr>
<td>( \frac{2}{\text{gm}<em>{idn}} = 166.667, \text{mV} ) ( \frac{2}{\text{gm}</em>{idp}} = 250, \text{mV} )</td>
<td></td>
</tr>
<tr>
<td>Current density (chart)</td>
<td>( id_{wn} := 18.7 \cdot A/m ) ( id_{wp} := 7.06 \cdot A/m )</td>
</tr>
<tr>
<td>Cutoff frequency (chart)</td>
<td>( f_{tn} := 19.7, \text{GHz} ) ( f_{tp} := 3.78, \text{GHz} )</td>
</tr>
</tbody>
</table>

#### Transistor sizing...

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_n := \frac{I_d}{id_{wn}} )</td>
<td>( W_n = 47.774, \mu\text{m} )</td>
</tr>
<tr>
<td>( W_p := \frac{I_d}{id_{wp}} )</td>
<td>( W_p = 126.541, \mu\text{m} )</td>
</tr>
</tbody>
</table>
Verification: (1) Test Bed

OTA

OTA in Feedback Loop
Verification: (2) Bias

So far, so good ...
Verification: (3) Dynamic Range

![Graph showing dynamic range with a perfect result at 106μV (target: 106μV) and 7.15nV/√Hz.]
Verification: (4) Settling Time

- Dynamic settling error target met
- Large static error ~10%
Openloop Gain

- Openloop gain only $A_{vo} \sim 50$
- $T_o = \beta A_{vo} = 11$
- Add cascodes to increase low frequency gain
Generic $g_m/I_d$-based Design Flow

1. Determine $g_m$ from design objectives (dynamic range, bandwidth, …)
2. Pick $L$
   - Short channel $\rightarrow$ high $f_t$ (high speed)
   - Long channel $\rightarrow$ high intrinsic gain, good matching, …
3. Pick $g_m/I_D$ or $f_t$
   - Large $g_m/I_D$ $\rightarrow$ low power, large signal swing
   - Small $g_m/I_D$ $\rightarrow$ high $f_t$ (high speed)
4. Determine $I_D$ (from $g_m$ and $g_m/I_D$)
5. Determine $W$ (from $I_D/W$, current density chart)

• Adapt to design specifics
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