Advanced Analog Integrated Circuits

Matching

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Issue

- In SPICE, two transistors with equal dimensions and terminal voltages (and temperature) carry the same current

- In Si, the current are (slightly) mismatched
  - Why?
  - How much mismatch?
  - Fix?
  - Verification?
Origins of Mismatch
### Wafer to Wafer Variations

**Wafer 1**
- all NMOS fast
- all PMOS nominal
- all C nominal
- all R fast

**Wafer 2**
- all NMOS slow
- all PMOS slow
- all C fast
- all R nominal

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Slow</th>
<th>Nominal</th>
<th>Fast</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TH}$</td>
<td>0.5V</td>
<td>0.4V</td>
<td>0.3V</td>
</tr>
<tr>
<td>$\mu C_{ox}$ (NMOS)</td>
<td>200 $\mu$A/V$^2$</td>
<td>250 $\mu$A/V$^2$</td>
<td>300 $\mu$A/V$^2$</td>
</tr>
<tr>
<td>$\mu C_{ox}$ (PMOS)</td>
<td>100 $\mu$A/V$^2$</td>
<td>130 $\mu$A/V$^2$</td>
<td>160 $\mu$A/V$^2$</td>
</tr>
<tr>
<td>$C_{MIM}$</td>
<td>1.2 fF/µm$^2$</td>
<td>1 fF/µm$^2$</td>
<td>0.8 fF/µm$^2$</td>
</tr>
<tr>
<td>$R_{poly}$</td>
<td>80 $\Omega$/□</td>
<td>70 $\Omega$/□</td>
<td>60 $\Omega$/□</td>
</tr>
<tr>
<td>$R_{nwell}$</td>
<td>1.3 k$\Omega$/□</td>
<td>1 k$\Omega$/□</td>
<td>0.7 k$\Omega$/□</td>
</tr>
</tbody>
</table>

- Verify performance for all combination (with simulator)
- Also low/high supply and temperature
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Random Variations

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Random Variations

Parameters for typical 180nm CMOS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{\text{vt}}$ (MOS)</td>
<td>5 mV-$\mu$m</td>
</tr>
<tr>
<td>$A_{\beta}$ (MOS)</td>
<td>1 %--$\mu$m</td>
</tr>
<tr>
<td>$A_{\Delta I_s/I_s}$ (BJT)</td>
<td>2 %--$\mu$m</td>
</tr>
<tr>
<td>$A_{\Delta \beta/\beta}$ (BJT)</td>
<td>4 %--$\mu$m</td>
</tr>
<tr>
<td>$A_{\Delta C/C}$ (MIM capacitor)</td>
<td>1 %--$\mu$m</td>
</tr>
<tr>
<td>$A_{\Delta R/R}$ (Poly resistor)</td>
<td>3 %--$\mu$m</td>
</tr>
</tbody>
</table>
A$_{\text{vt}}$ for 180nm CMOS

- Good match between heuristic model and experimental data, except
  - minimum channel length (actual length is smaller than drawn)
  - very long channel device

$A_{VT}$ versus Gate Oxide Thickness

- $A_{VT}$ increases $\sim 1 \text{ mV} \times \mu\text{m}$ for every nm of gate insulator thickness
  - for well-engineered process
- But: circuits get smaller …
- $A_{VT}$ scaling design: e.g.
  - Outlier for 0.6 $\mu\text{m}$ PMOS is result of compensating implant, leading to high variability
  - beyond 0.6 $\mu\text{m}$ node dedicated well implant is used

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Yield

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Random Mismatch - Example

What is the mismatch between two MIM capacitors with \( W = L = 20\mu m \)?

\[
\sigma_{\Delta C/C} = \frac{A_{\Delta C/C}}{\sqrt{20\mu m \times 20\mu m}} = \frac{1\% \times \mu m}{20\mu m} = 0.05\%
\]

\( \rightarrow \) 68.2\% of all devices fabricated match to ±0.05\%.

Yield

- Fraction of devices that meet specification

<table>
<thead>
<tr>
<th>Interval</th>
<th>Yield</th>
<th>Fraction Bad</th>
</tr>
</thead>
<tbody>
<tr>
<td>1σ</td>
<td>68.3%</td>
<td>1/3</td>
</tr>
<tr>
<td>2σ</td>
<td>95.4%</td>
<td>1/22</td>
</tr>
<tr>
<td>3σ</td>
<td>99.7%</td>
<td>1/370</td>
</tr>
<tr>
<td>4σ</td>
<td>99.99%</td>
<td>1/16,000</td>
</tr>
<tr>
<td>5σ</td>
<td>99.999%</td>
<td>1/1,700,000</td>
</tr>
<tr>
<td>6σ</td>
<td>99.999 999 8%</td>
<td>1/507,000,000</td>
</tr>
</tbody>
</table>

- Large customers tolerate less than 1ppm failures
  - 6σ design
  - Testing, binning
  - Capacitor example: 1σ → ±0.05%, 6σ → ±0.3%,
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Mismatch in Mirrors and Differential Pairs

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Mismatch in Current Mirror

\[ V_1 \]
\[ I_1 \]
\[ M_1 \]
\[ \beta \]

\[ \Delta V_{TH} \]

\[ V_2 = V_1 \]
\[ I_2 \]
\[ M_2 \]
\[ \beta + \Delta \beta \]
Differential Pair

\[ V_1 \]
\[ I_1 \]
\[ V_{i1} \]
\[ M_1 \]
\[ \beta \]

\[ V_2 = V_1 \]
\[ I_2 \]
\[ V_{i2} \]
\[ M_2 \]
\[ \beta + \Delta \beta \]

\[ I_{ss} \]
Verification

1. PVT
   - Process, voltage, temperature
   - Perform verification for all combinations on design and extracted netlist

2. Random variations
   - Monte-Carlo analysis
Technology Trend

- slow/fast spread decreases
  - better process control
- random variations increase
  - smaller devices

$V_{TH}$ spread for 90nm NMOS and PMOS:

- random variations comparable to slow/fast spread