Advanced Analog Integrated Circuits

Operational Transconductance Amplifier II
Multi-Stage Designs

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

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Voltage Gain

Low gain, high swing

High gain, low swing
<table>
<thead>
<tr>
<th>Voltage gain stage</th>
<th>Single</th>
<th>Multiple</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Bias current</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Output swing</td>
<td>limited by cascode</td>
<td>higher</td>
</tr>
<tr>
<td></td>
<td>single path to ground</td>
<td>multiple bias currents</td>
</tr>
</tbody>
</table>
Frequency Compensation

• Cascaded amplifiers
  – Each stage contributes a pole
  – Stability: only one “dominant pole” \( f_p < f_u \) of \( T(s) \)
  – Ensuring this is called “compensation”

• Main compensation techniques
  – Narrowbanding
  – Feedback zero
  – Miller
  – Feedforward
Narrowbanding

\[ |T(s)| \]

\[ \log \omega \]

\[ \omega \]

\[ \omega_p \]

\[ \omega_p_1 \]

\[ \omega_p_2 \]

\[ \omega_u = \frac{\omega_p_2}{3} \]
Feedback Zero

• LHP zero adds “lead”
• Closed-loop response modified above zero
• Compensation only marginally reduces bandwidth

Miller Compensation
Intuitive Appreciation of Pole Splitting

- Capacitive feedback splits the poles
Compensated $a(s)$

\[
p_1 \approx -\frac{1}{R_1 R_2 C_c} \quad \text{Miller gain}
\]

\[
p_2 \approx -\frac{g_{m2}}{C_2 \left(1 + \frac{C_1}{C_c}\right) + C_1} \approx -\frac{g_{m2}}{C_2}
\]

\[
z = +\frac{g_{m2}}{C_c}
\]

\[
\text{GBW} = \omega_u \approx |\omega_{p1}| T_o = \beta \frac{g_{m1}}{C_c}
\]
Bandwidth Comparison

Single voltage gain stage

\[ \omega_u \approx \beta \frac{g_{m1}}{C_L} \]

\[ \omega_{nd} \approx \frac{\omega_T}{3} \]

Two voltage gain stages

\[ \omega_u \approx \beta \frac{g_{m1}}{C_c} \]

\[ \omega_{nd} = \omega_{p2} \approx \frac{g_{m2}}{C_L} = \frac{g_{m2}}{C_L} \left( \frac{C_1}{C_L} \right) \left( \frac{\omega_{T2}}{\omega_{T2}} \right) \text{ <1?} \]

\[ C_L \uparrow \quad \text{PM} \uparrow \]

\[ \text{PM} \downarrow \]
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Miller Zero

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

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Root Locus

Ignoring zero

With zero
Bode Plot

Bode Diagram

-20
-40
-60
-80
0
20
40
60
80
0
180
Phase (deg) +180

Frequency (rad/s)

<table>
<thead>
<tr>
<th>Frequency (rad/s)</th>
<th>Magnitude (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10^{-2}</td>
<td>-20</td>
</tr>
<tr>
<td>10^{-1}</td>
<td>-40</td>
</tr>
<tr>
<td>10^0</td>
<td>-60</td>
</tr>
<tr>
<td>10^1</td>
<td>-80</td>
</tr>
<tr>
<td>10^2</td>
<td>0</td>
</tr>
<tr>
<td>10^3</td>
<td>90</td>
</tr>
<tr>
<td>10^4</td>
<td>-30</td>
</tr>
<tr>
<td>10^5</td>
<td>-50</td>
</tr>
<tr>
<td>10^6</td>
<td>-70</td>
</tr>
</tbody>
</table>

Poles:
- $p_1$
- $p_2$
- $z$
Intuitive Appreciation of Zero

![Circuit Diagram]

- $C_c$
- $g_{m2}$
- $v_1$
- $i_c$
- $i_g$
Mitigating Impact of Zero

Key: unilateral feedback

Options:
- SE
- H-bridge comp
- Muling resistor
Nulling Resistor

\[ T(s) = T_0 \frac{1 - sC_c \left( \frac{1}{g_{m2}} - R_z \right)}{(1 - \frac{s}{p_1})(1 - \frac{s}{p_2})(1 - \frac{s}{p_3})} \]

- \( R_z \) can be used to “tune” the zero
- Poles \( p_1 \) and \( p_2 \) unchanged
- Additional pole \( p_3 \approx -\frac{1}{R_zC_1} \)
Choices for $R_z$

\( a) \quad R_z = \frac{1}{g_m 2} \)

\( b) \quad R_z = \frac{1 + \frac{C_2}{C_c}}{g_m 2} \)

\( \omega_p 3 \approx \frac{\omega_n^2}{1 + \frac{C_2}{C_c}} \)

\[ \text{cancel } p_2 \]
Ahuja Compensation

- No zero (ideal cascode)
- $p_2$ at higher frequency
- Translates into smaller $C_c$ for given $C_2$
- Problems:
  - Current $I_2$ (extra power)
  - Mismatch (in $I_2$ sources) causes offset
  - $I_2$ limits slew rate

\[ p_1 \approx -\frac{1}{(1 + g_{m2}R_2)R_1C_c} \approx -\frac{g_{m1}}{a_{v0}C_c} \]

\[ p_2 \approx -\frac{g_{m2}C_c}{C_c + C_2 \frac{C_1}{C_2}} \]

\[ = p_2^* \frac{C_2}{C_c + C_2 \frac{C_1}{C_2}} \]

\[ \text{usually } > 1 \]

[Ahuja, IEEE JSSC, 12/1983]
B. E. Boser

Ribner Variant

- Uses 1st stage cascode to make feedback unilateral
- No extra power or slewing limitation
- 3rd order response
  - very challenging design problem

[ Ribner, IEEE JSSC, 12/1984 ]
Noise Analysis

For full treatment, see

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Design Example

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

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Design Example
Specification

Closed-loop gain (magnitude):
\[ A_{vo} := 2 \]

Settling time:
\[ t_s := 2\text{ns} \]
\[ f_{s_{\text{max}}} := \frac{1}{2 \cdot t_s} = 250 \cdot \text{MHz} \]

Dynamic settling accuracy:
\[ \varepsilon_d := 0.02\% \]

Dynamic range at output:
\[ \text{DR} := 10^{6.5} \]
\[ 10 \cdot \log(\text{DR}) = 65 \text{ dB} \]

Sampling capacitance:
\[ C_s := 2\text{pF} \]
\[ C_L := \frac{C_s}{A_{vo}} = 1\text{pF} \]

Load capacitance:
\[ V_{dd} := 1.8\text{V} \]

Supply voltage:
\[ R_z = \frac{1}{\text{minimum}} \]

Zero mitigation:

Power:
Unknowns

• Topology

• Device parameters:
  – \( M_1: g_{m1}, V_1^*, f_{T1} \Rightarrow I_{D1}, L_1, W_1 \)
  – \( M_2: g_{m2}, V_2^*, f_{T2} \Rightarrow I_{D2}, L_2, W_2 \)

• Compensation capacitance, \( C_c \)

• Noise excess factors, \( \alpha_1, \alpha_2 \)

• Output voltage range
Structural Parameters

• Guess (and iterate):

  M1 channel length:
  \[ L_1 := 250\text{nm} \]

  M2 channel length:
  \[ L_2 := 250\text{nm} \]

  Available output voltage range:
  \[ V_{\text{opp}} := V_{\text{dd}} - 300\text{mV} = 1.5\text{V} \]

  OTA noise factor (topology & bias):
  \[ \alpha_1 := 2 \quad \alpha_2 := 2 \]

  \( C_{g_{g1}} \) as a fraction of \( C_{s+Cf} \):
  \[ r_{g_{g1}} := 1 \]

  \( C_{g_{g2}} \) as a fraction of \( C_{\text{Ltot}} \):
  \[ r_{g_{g2}} := 1 \]

• Now calculate remaining design parameters …
Gain and Feedback Factor

Feedback capacitance:

\[ C_f := \frac{C_s}{A_{vo}} \]
\[ C_f = 1 \cdot \text{pF} \]

M1 gate capacitance (guess):

\[ C_{gg1} := r_{gg1} \cdot (C_s + C_f) \]
\[ C_{gg1} = 3 \cdot \text{pF} \]

Feedback factor:

\[ \beta := \frac{C_f}{C_f + C_s + C_{gg1}} \]
\[ \beta = 0.167 \]

Total load capacitance:

\[ C_{L_{tot}} := C_L + (1 - \beta) \cdot C_f \]
Dynamic Range

Total noise at output:

\[ N_{ot} := \frac{1}{2} \cdot \left( \frac{V_{opp}}{2} \right)^2 \]

\[ \sqrt{N_{ot}} = 298.227 \cdot \mu V \]

Compensation capacitance:

guess (for MathCad):

\[ C_c := 1 \text{pF} \]

actual value: given

\[ N_{ot} = \frac{\alpha_1}{\beta} \cdot \frac{k_B \cdot T_r}{C_c} \cdot \left( 1 + \beta \cdot \frac{\alpha_2}{\alpha_1} \cdot \frac{C_c}{C_{Ltot}} \right) \]

find \( C_c = 0.568 \text{pF} \)
Settling time (single pole, no slewing):

\[ t_s = -0.7 \cdot \tau \cdot \ln(\varepsilon_d) \]

Settling time constant:

\[ \tau := \frac{-t_s}{0.7 \cdot \ln(\varepsilon_d)} = 335.456 \cdot \text{ps} \]

Settling time constant:

\[ \tau = \frac{C_c}{\beta \cdot g_{m1}} \quad \omega_u := \frac{1}{\tau} = 474.444 \cdot \text{MHz} \cdot 2\pi \]

Transconductance of M1:

\[ g_{m1} := \frac{C_c}{\beta \cdot \tau} = 17.886 \cdot \text{mS} \]

Nondominant pole (\(\sim 73\ \text{deg PM})\):

\[ \omega_{p2} := 3.3 \cdot \omega_u = 1.566 \text{GHz} \cdot 2\pi \]

Gate capacitance of M2 (guess):

\[ C_{gg2} := r_{gg2} \cdot C_{Ltot} = 1.833 \text{ pF} \]

Transconductance of M2:

\[ g_{m2} := \omega_{p2} \cdot \left[ C_{Ltot} \cdot \left( 1 + \frac{C_{gg2}}{C_c} \right) + C_{gg2} \right] = 69.135 \text{ mS} \]
Power Dissipation

Cutoff frequency of M1:
\[ \omega_T^1 := \frac{g_{m1}}{C_{gg1}} = 0.949 \text{GHz} \cdot 2\pi \]

Cutoff frequency of M2:
\[ \omega_T^2 := \frac{g_{m2}}{C_{gg2}} = 6.002 \text{GHz} \cdot 2\pi \]

M1 power efficiency (lookup):
\[ V_{1\text{star}} := 85 \text{mV} \]

M2 power efficiency (lookup):
\[ V_{2\text{star}} := 120 \text{mV} \]

M1 drain current:
\[ I_{d1} := 0.5 \times V_{1\text{star}} \times g_{m1} = 760.159 \mu\text{A} \]

M2 drain current:
\[ I_{d2} := 0.5 \times V_{2\text{star}} \times g_{m2} = 4.148 \text{mA} \]

Power dissipation:
\[ P_t := V_{dd} \times (I_{d1} + I_{d2}) = 8.835 \text{mW} \]

Close to weak inversion:
- increase \( L_1 \) (higher gain)
- reduce \( r_{gg1} \) (lower power?)
Iteration: $r_{gg1} = 0.1$

Cutoff frequency of M1:

$$\omega_{T1} := \frac{g_{m1}}{C_{gg1}} = 5.219 \text{GHz} \cdot 2\pi$$

Cutoff frequency of M2:

$$\omega_{T2} := \frac{g_{m2}}{C_{gg2}} = 5.788 \text{GHz} \cdot 2\pi$$

M1 power efficiency (lookup):

$$V_{1\text{star}} := 120 \text{mV}$$

M2 power efficiency (lookup):

$$V_{2\text{star}} := 120 \text{mV}$$

M1 drain current:

$$I_{d1} := 0.5 \cdot V_{1\text{star}} \cdot g_{m1} = 590.241 \mu\text{A}$$

M2 drain current:

$$I_{d2} := 0.5 \cdot V_{2\text{star}} \cdot g_{m2} = 3.703 \text{mA}$$

Power dissipation:

$$P_t := V_{dd} \cdot (I_{d1} + I_{d2}) = 7.728 \text{mW}$$

was 8.8 mW
Sanity Check: Single Gain Stage

- About half the power of 2-stage
  - Provided gain & dynamic range can be met
  - Practical “lower bound”

\[
\tau_1 := \frac{-0.7 \cdot t_s}{\ln(\varepsilon_d)} = 164.373 \text{ ps}
\]

\[
g_m := \frac{C_{L_{\text{tot}}}}{\beta \cdot \tau_1} = 34.069 \text{ mS}
\]

\[
C_{gg} := 0.5 \cdot (C_s + C_f) = 1.5 \text{ pF}
\]

\[
\omega_T := \frac{g_m}{C_{gg}} = 3.615 \text{ GHz} \cdot 2\pi
\]

\[
V_{\text{star}} := 100 \text{ mV}
\]

\[
I_d := 0.5 \cdot g_m \cdot V_{\text{star}} = 1.703 \text{ mA}
\]

\[
P_1 := V_{dd} \cdot I_d = 3.066 \text{ mW}
\]
Finalize Design

- Iterate over all parameters (use Matlab “lookup”)
- Estimate and add extrinsic capacitances
- Other design elements
  - Static settling error
  - Slewing
  - Biasing
  - Device geometry
  - Corners
  - Layout …
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Special OTA Topologies

Bernhard E. Boser
University of California, Berkeley
bosер@eecs.berkeley.edu

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Nested Miller Compensation

Settling Behavior

• Very challenging design problem
• Accurate and fast settling (nearly?) impossible
• Good choice for broad-band, high gain & other situations that do not require fast settling

Feedforward OTA