Advanced Analog Integrated Circuits

Operational Transconductance Amplifier I & Step Response

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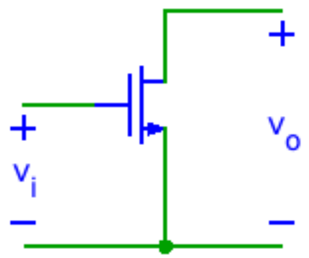
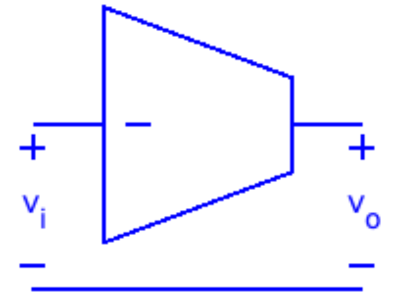
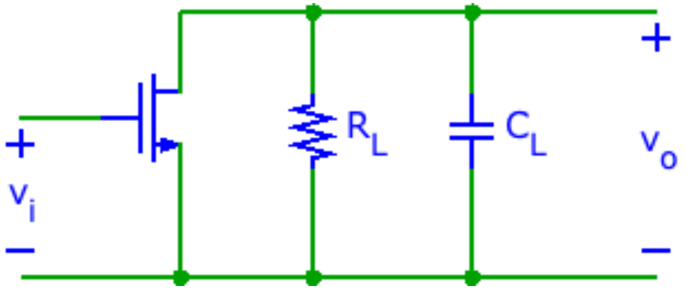
High-Level View



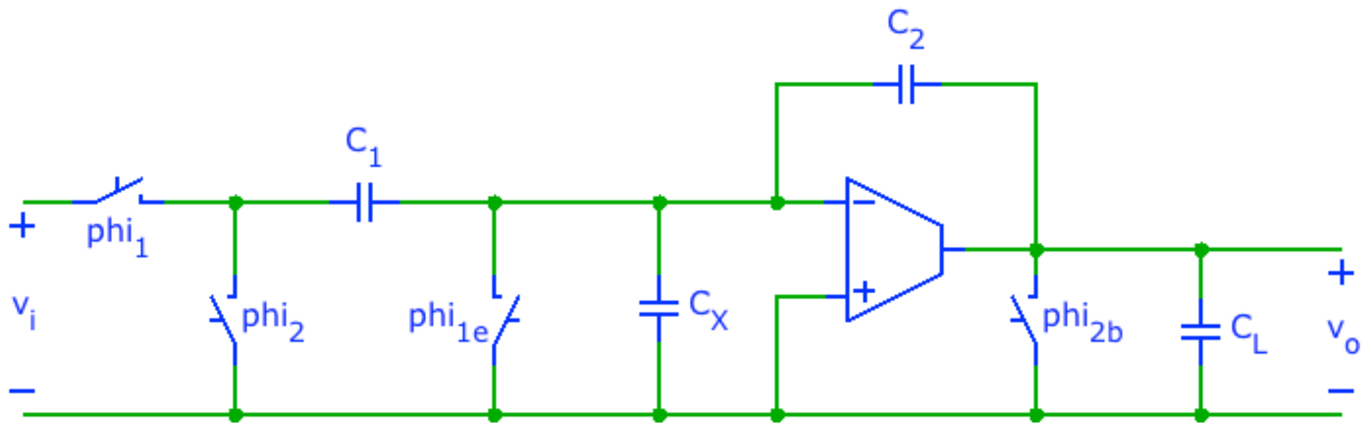


- Transistors are transconductors
- Some OTA designs consist of >40 transistors
  - Only few (typically 1 … 2) provide the transconductance in the signal path
  - The rest is support, e.g.
    - increasing low frequency gain
    - output voltage range
    - biasing
- Hierarchical design strategies are imperative
  - Unless you like nodal equations for 40 transistors …

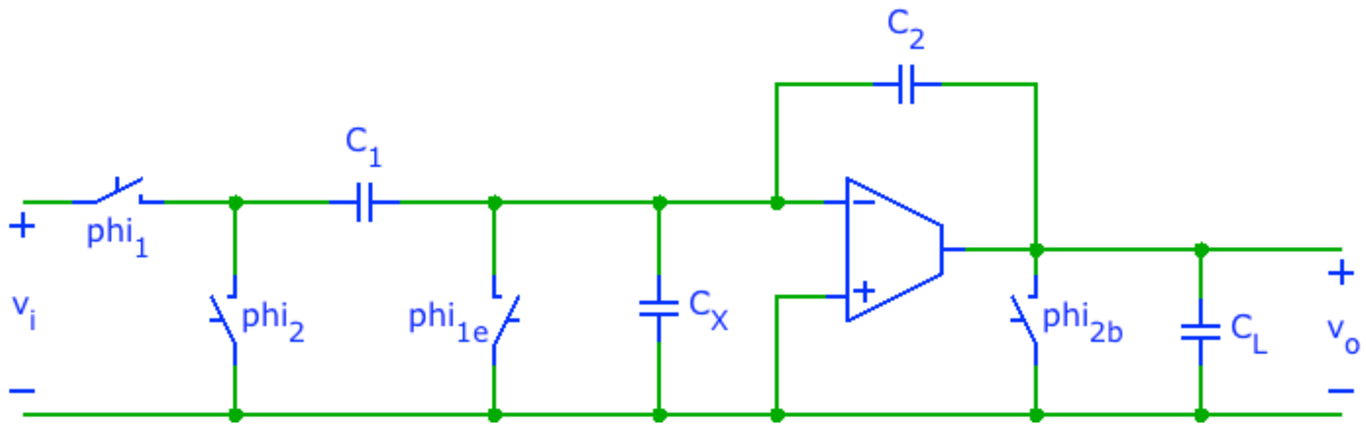
Divide and Conquer



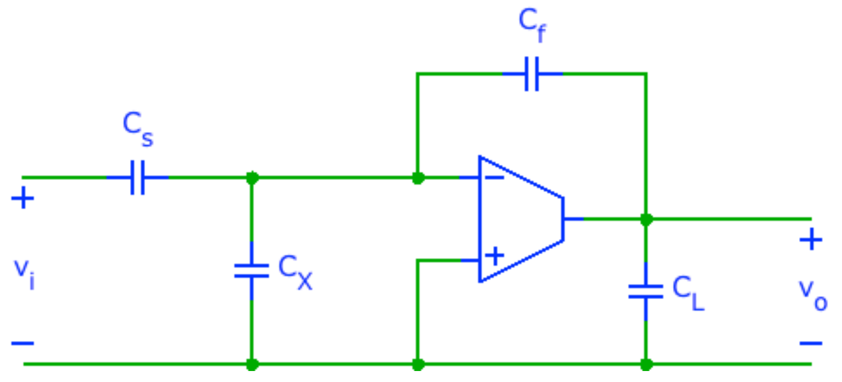
In SC Circuit



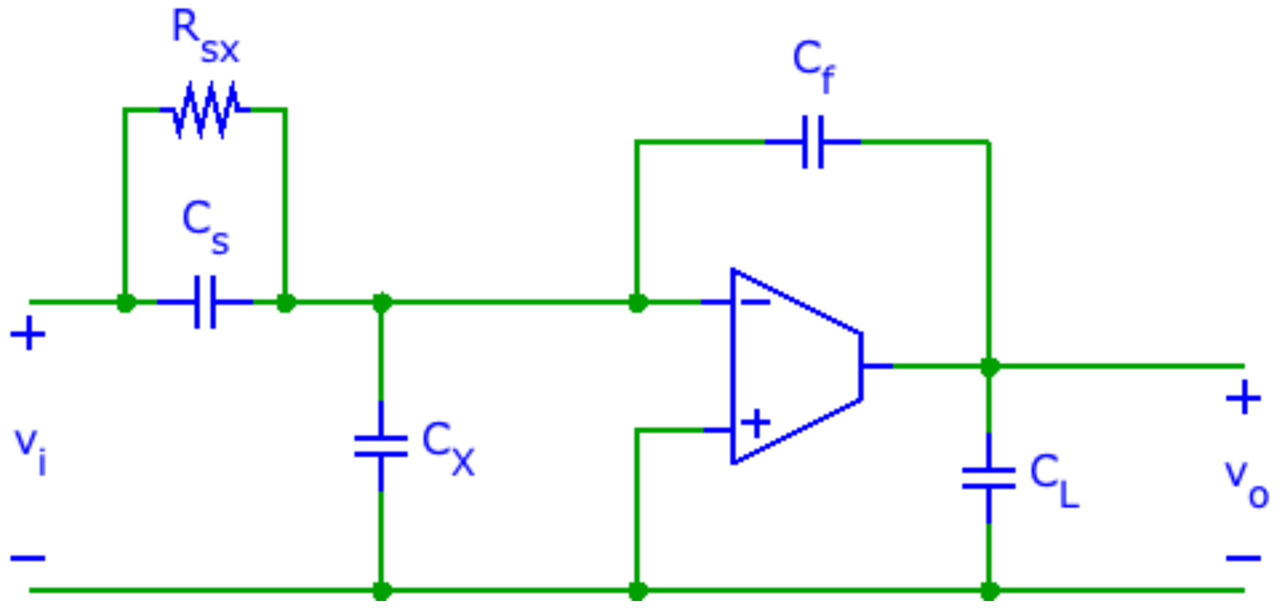
In SC Circuit



Amplifier is active only in ϕ_2:

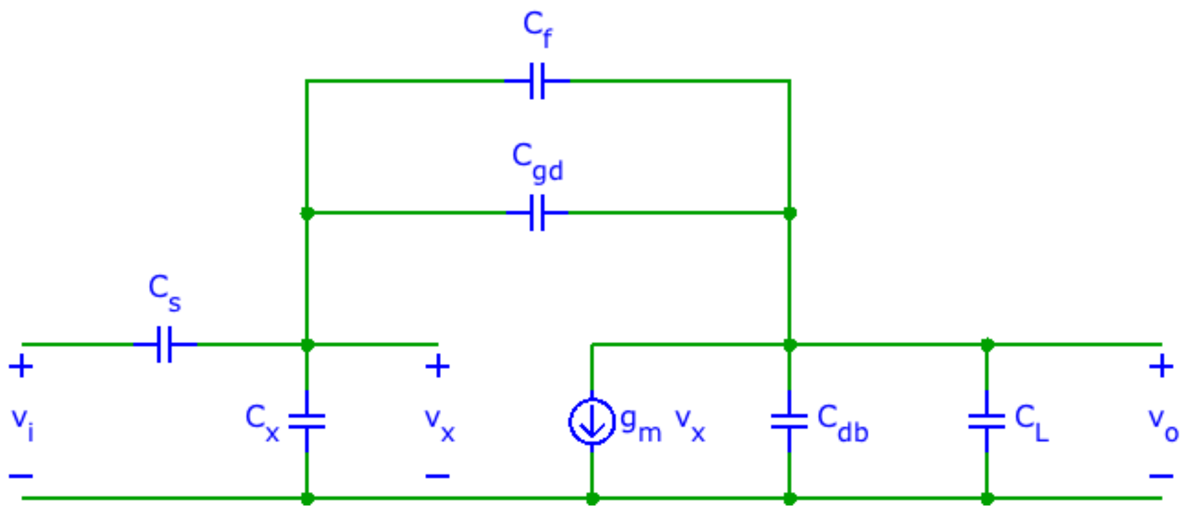


Capacitive Feedback … Simulation



$$R_{sx} \cong 20\ \mathrm{G\Omega}$$

Small-Signal Model



Absorb C_{gd}, C_{db}, etc. in C_f, C_L, …

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Loop-Gain & Stability

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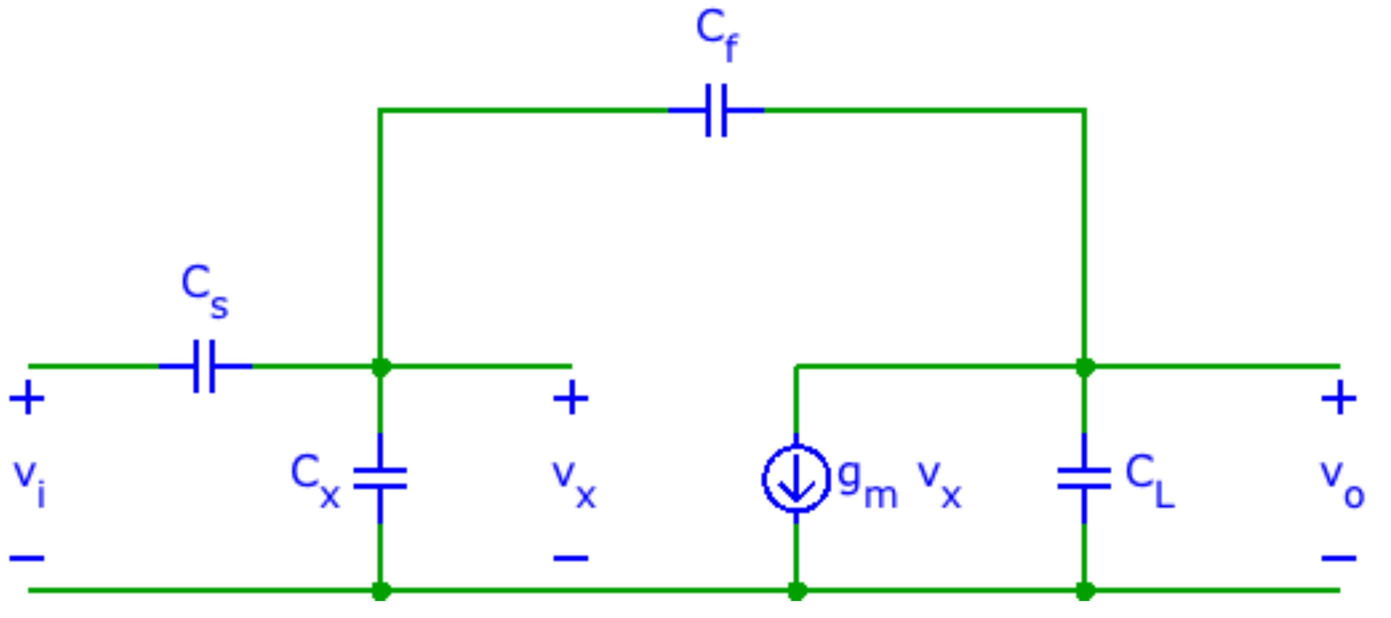
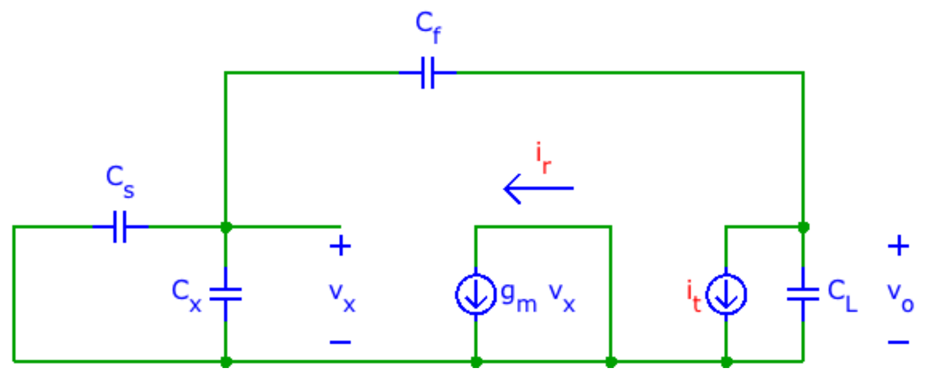
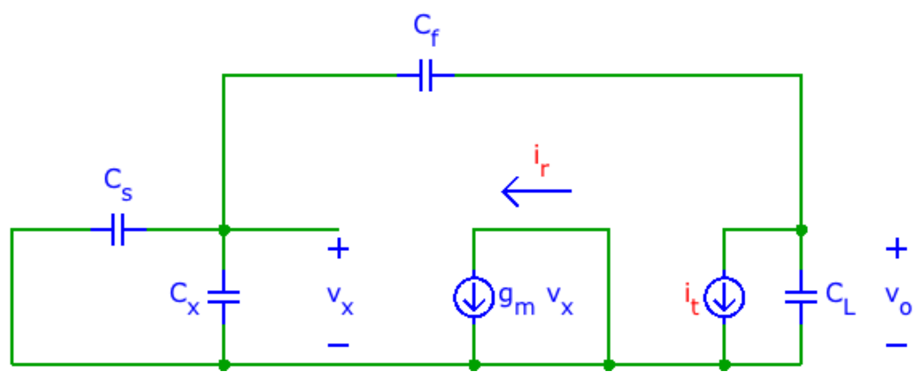
Model



Loop-Gain Analysis



Loop-Gain T(s)



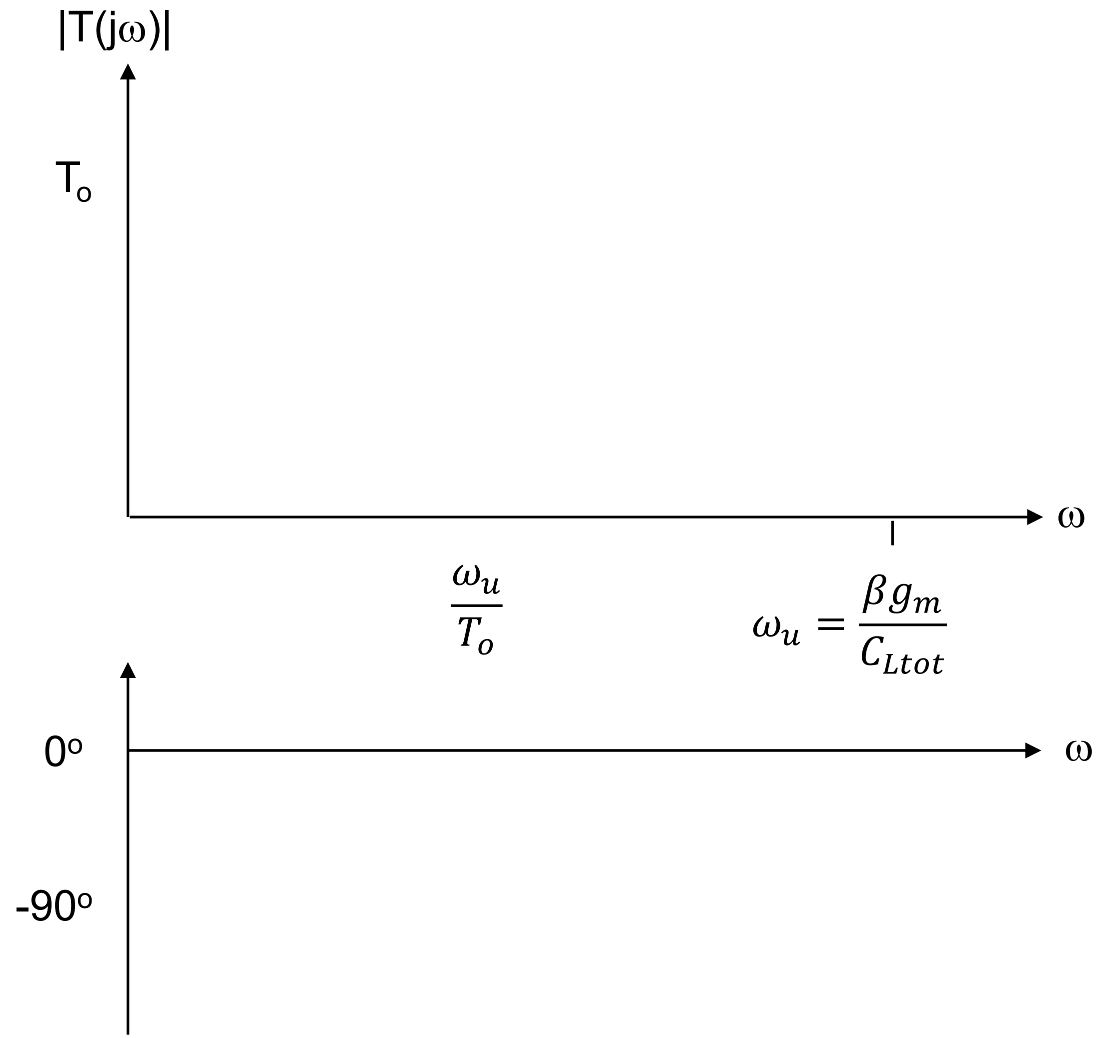
$$T(s) = \beta \frac{g_m}{s \cdot C_{Ltot}}$$

Feedback factor $\beta = \frac{v_x}{v_o} = \frac{C_f}{C_f + C_s + C_x} \neq \frac{1}{a_{vo}}$

Effective Load Capacitance $C_{Ltot} = C_L + (1 - \beta)C_f$

Frequency Response of T(s)

$$T(s) = \frac{\beta g_m}{s \cdot C_{Ltot}}$$



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Closed-Loop Response

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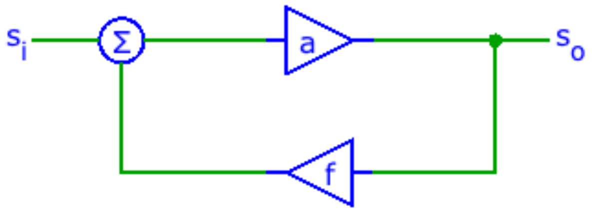
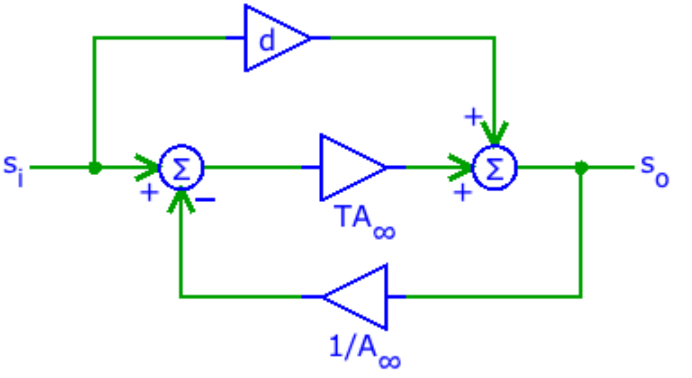
Closed-Loop Analysis

Feedback-Only Model

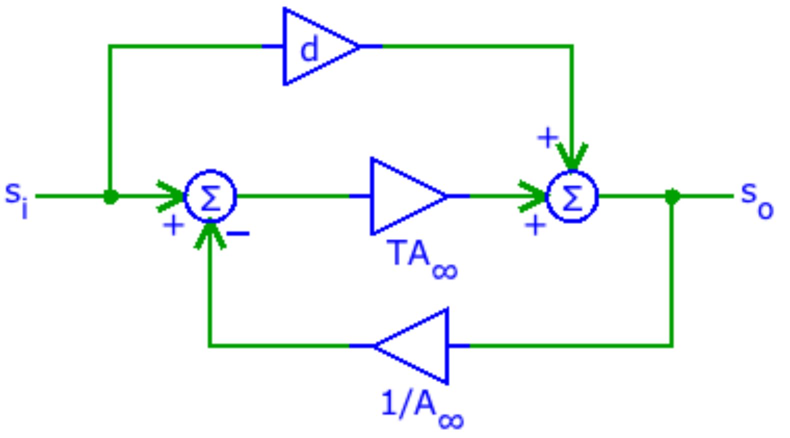


Generalized Model

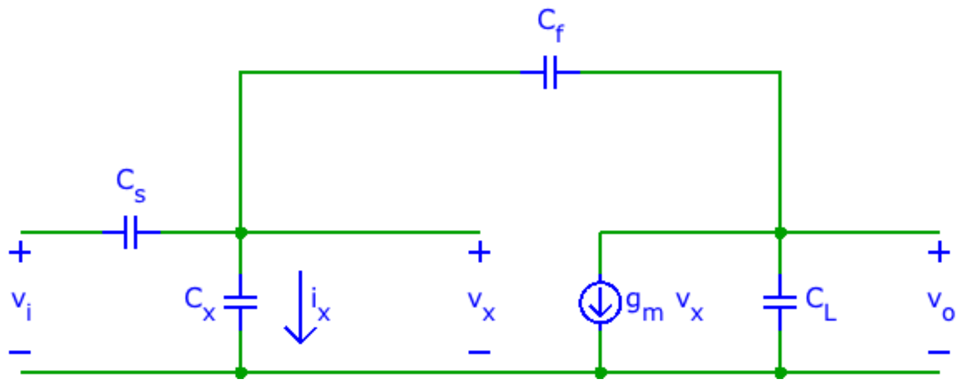


Ref: P. Hurst, "A comparison of two approaches to feedback circuit analysis," IEEE Trans. edu., Aug. 1992, pp. 253-261.

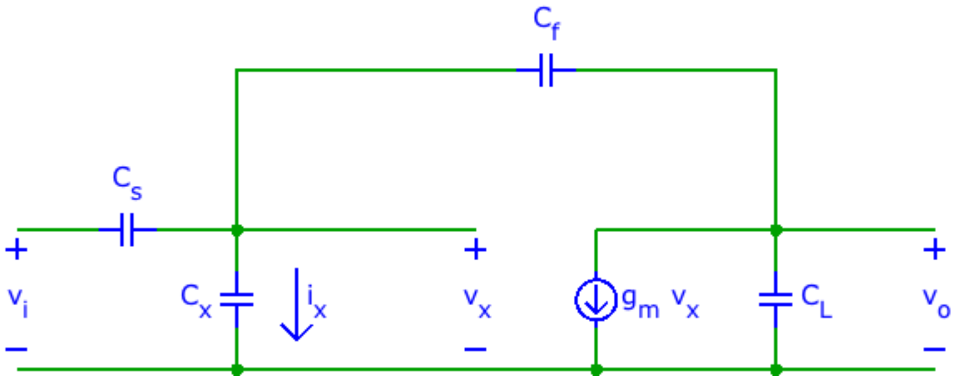
Closed-Loop Transfer Function



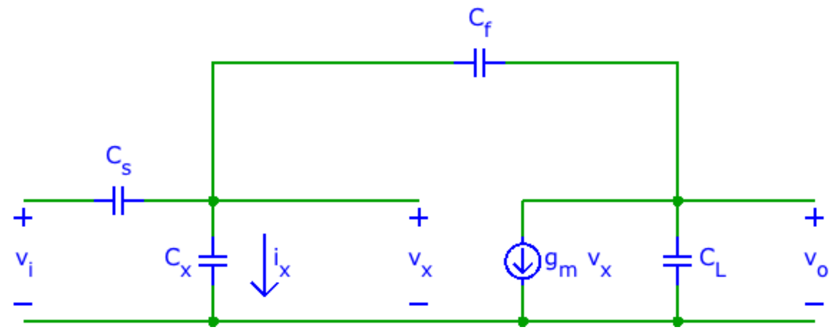
A_∞



d



Closed-Loop Gain



$$A(s) = A_\infty \frac{T(s)}{1+T(s)} + \frac{d}{1+T(s)} = -\frac{C_s}{C_f} \frac{\frac{\beta g_m}{s \cdot C_{Ltot}}}{1+\frac{\beta g_m}{s \cdot C_{Ltot}}} + \frac{\beta \frac{C_s}{C_{Ltot}}}{1+\frac{\beta g_m}{s \cdot C_{Ltot}}}$$

$$= -\frac{C_s}{C_f} \frac{1 - s\frac{C_f}{g_m}}{1 + s\frac{C_{Ltot}}{\beta g_m}} = -\frac{C_s}{C_f} \frac{1-\frac{s}{z}}{1-\frac{s}{p}}$$

$$p = -\frac{\beta g_m}{C_{Ltot}} \qquad z = +\frac{g_m}{C_f}$$

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Stability and T(s) with Simulator

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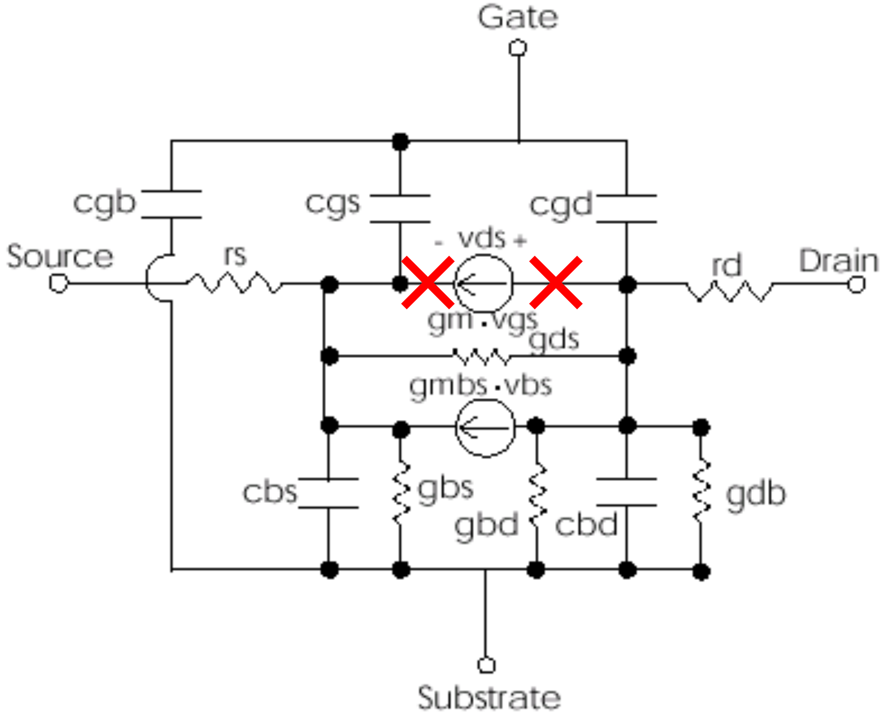
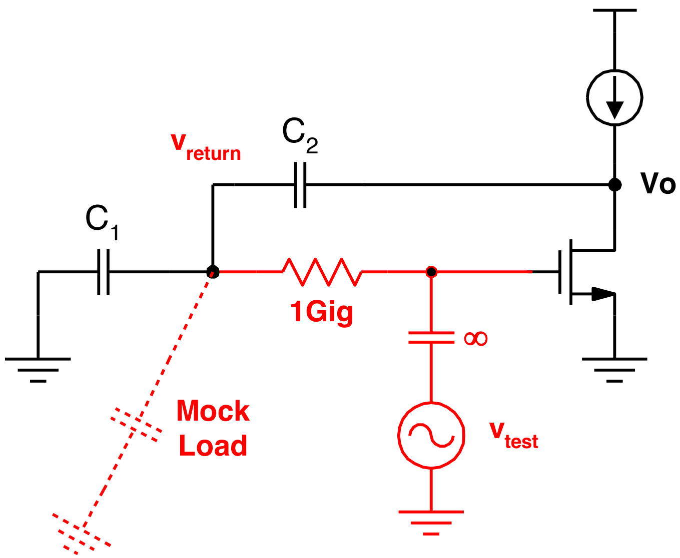
T(s) Verification with Simulator

- Infinite impedance point to break loop usually not accessible
  - E.g. inside transistor



[Hspice manual]

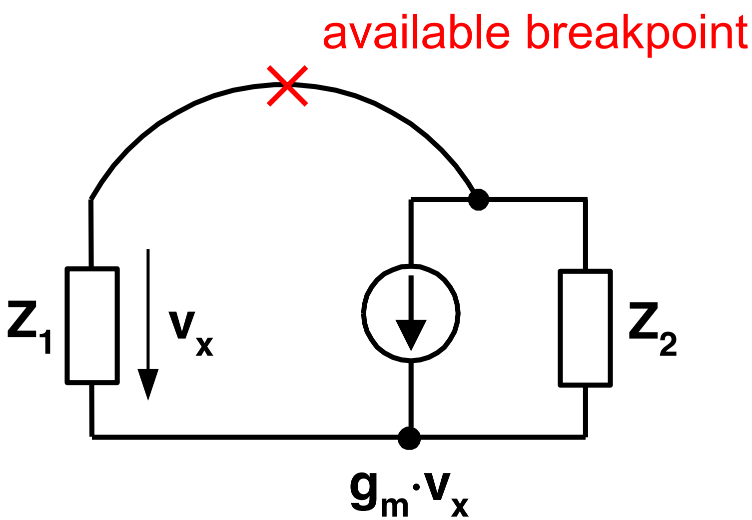
Workaround (Don't do this!)



[Drawing by B. Murmann]

General Problem

Any “single loop“ feedback circuit can be represented as:

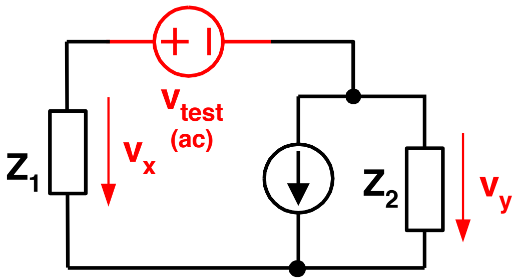


[Drawing by B. Murmann]

$$T(s) = g_m \frac{Z_1 \cdot Z_2}{Z_1 + Z_2}$$

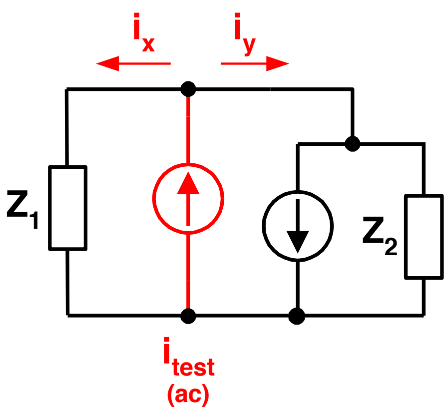
Breakpoint at ideal source is not available.
But there is a breakpoint “between finite impedances“

Middlebrook Double Injection Method



$$\frac{v_y}{v_x} \equiv T_v = g_m \cdot Z_2 + \frac{Z_2}{Z_1}$$

True Loop Gain: $$T = g_m \cdot \frac{Z_1 Z_2}{Z_1 + Z_2}$$



$$\frac{i_y}{i_x} \equiv T_i = g_m \cdot Z_1 + \frac{Z_1}{Z_2}$$

Solving yields:

$$\boxed{T = \frac{T_v T_i - 1}{T_v + T_i + 2}}$$

[Drawing by B. Murmann]

[Middlebrook 75]

- No "DC" break in the loop, all loading effects covered.
- Measure T_v and T_i, then calculate actual T
- Variant implemented in many simulators, e.g. stb-analysis in Spectre

SPICE

Multiple Feedback Loops

- Break all loops at a single point
- If such a point does not exist: [Bode 45]

"If a circuit is stable when all its tubes have their nominal gains, the total number of clockwise and counterclockwise encirclements of the critical point must be equal to each other in the series of Nyquist diagrams for the individual tubes obtained by beginning with all tubes dead and restoring the tubes successively in any order to their nominal gains"

– Suggestion: take a controls class if your circuit depends on this!

Nonlinearities

- Real circuits are nonlinear – frequency response depends on signal amplitude. Bode:

> "... thus the circuit may sing when the tubes begin to lose their gain because of age, and it may also sing, instead of behaving as it should, when the gain increases from zero as power is supplied to the circuit ..."

- Always run a "large signal" transient analysis for a complete stability check!
  - With realistic (large) signal amplitudes including overload
  - Power supply ramping. Is a special order required?

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Settling

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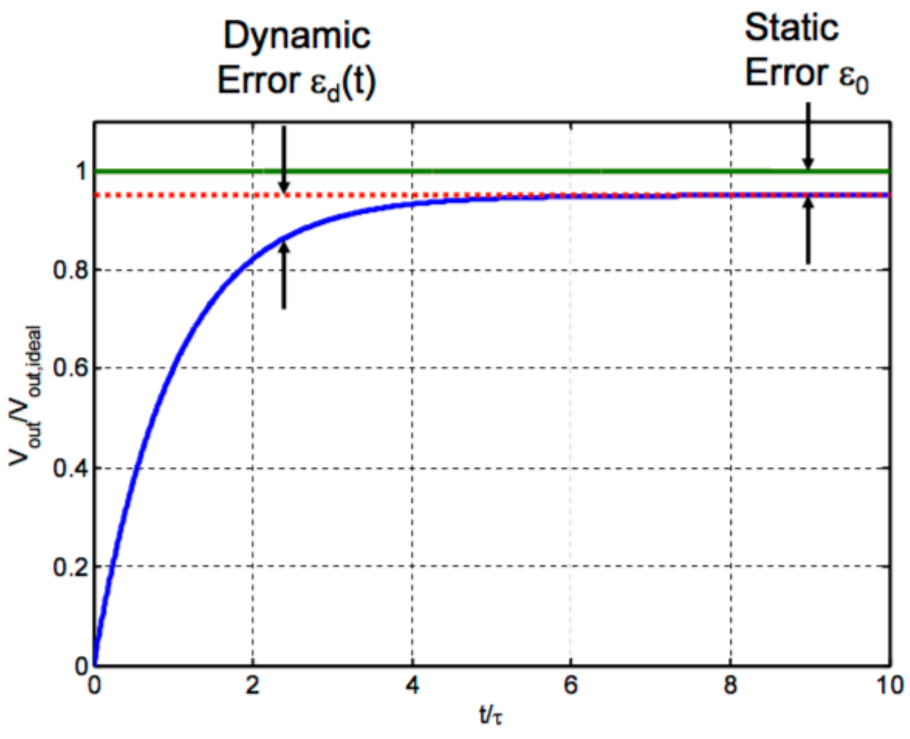
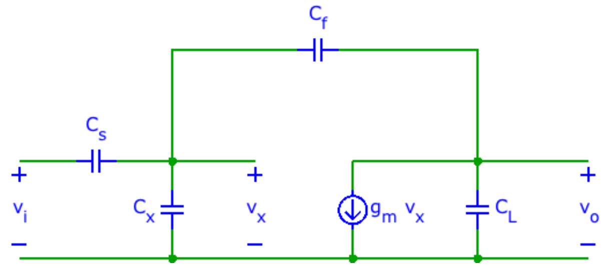
Step Response



Closed-Loop Gain



- Use favorite analysis method, e.g. return-ratio analysis*, nodal analysis, …

$$A(s) = \frac{V_o(s)}{V_i(s)} = -\frac{C_s}{C_f}\frac{1 - s\frac{C_f}{g_m}}{1 + s\frac{C_{Ltot}}{\beta g_m}} = -\frac{C_s}{C_f}\frac{1-\frac{s}{z}}{1-\frac{s}{p}}$$

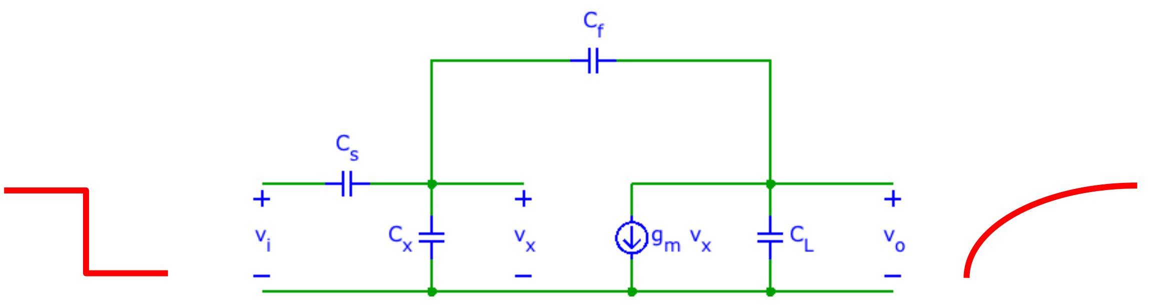
$$\omega_p = \frac{\beta g_m}{C_{Ltot}} \cong \omega_{-3dB} \text{ of } A(s) = \omega_u \text{ of } T(s)$$

$$\omega_z = \frac{g_m}{C_f}$$

$$\frac{\omega_z}{\omega_p} = \frac{C_{Ltot}}{\beta C_f} \qquad \text{usually} \quad \gg 1$$

*Note: 2-port analysis ignores the feedforward path and therefore does not get the zero

Dynamic Error (no zero)



Assume switch on-resistance contribution to settling is negligible

Dynamic Settling Error

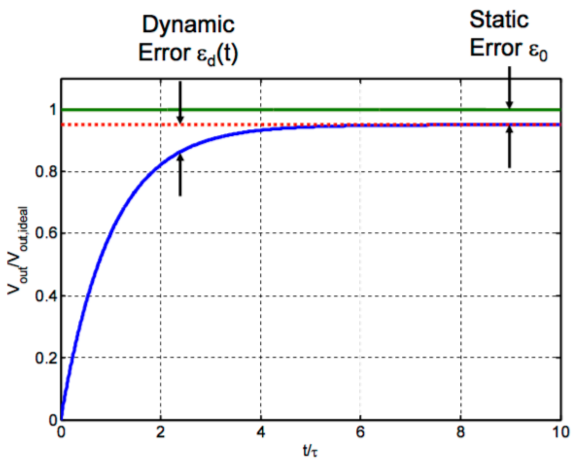
Dynamic Settling Error (single pole)

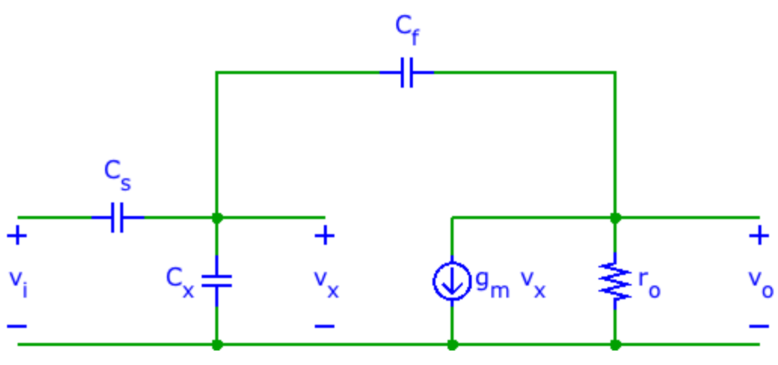
ε_d	t_s/τ
1%	4.6
0.1%	6.9
0.01%	9.2
10^{-6}	13.8

Amplifier Bandwidth versus f_s

ε_d	f_{-3dB}/f_s
1%	1.5
0.1%	2.2
0.01%	2.9
10^{-6}	4.4

Static Settling Error

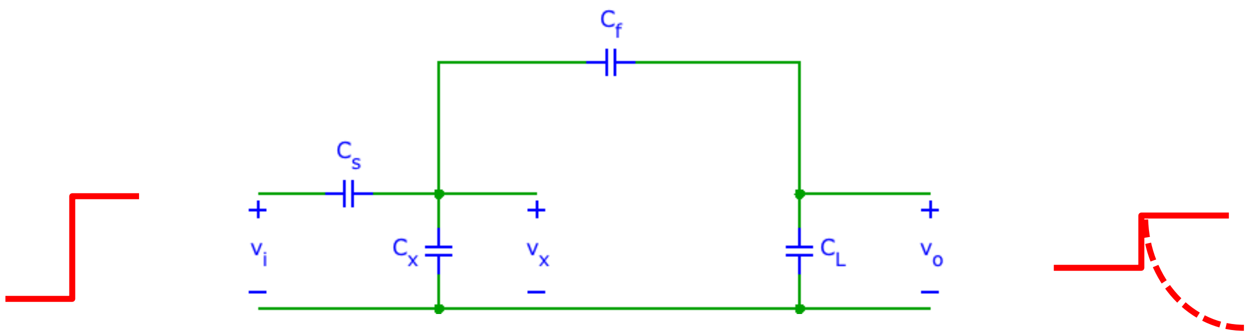




Example

$C_s = 4\text{pF}$ $\quad C_f = 1\text{pF}$ $\quad C_x = 1\text{pF}$ $\quad g_m r_o = 6000$

Dynamic Error (with zero)



- Instant response to step determined by capacitive feed-forward

$$A(s) = \frac{V_o(s)}{V_i(s)} = -\frac{C_s}{C_f} \frac{1 - s\frac{C_f}{g_m}}{1 + s\frac{C_{Ltot}}{\beta g_m}}$$

$$z = +\frac{g_m}{C_f} \qquad p = -\frac{\beta g_m}{C_{Ltot}}$$

Step Response with Zero

$$v_{o,step}(t) = -V_{step} \cdot G_i \left\{1 - \left(1 - \frac{p}{z}\right) e^{-t/\tau}\right\}$$

$$1 - \frac{p}{z} = \frac{1}{1 - \beta \frac{C_f}{C_f + C_L}}$$

$$t_s = -\tau \cdot \ln\left\{\varepsilon_d \left(1 - \beta \frac{C_f}{C_f + C_L}\right)\right\}$$

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Phase Margin

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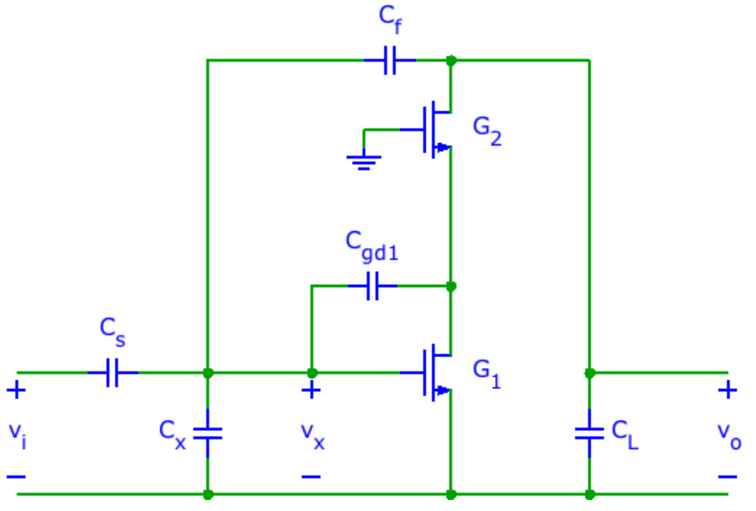
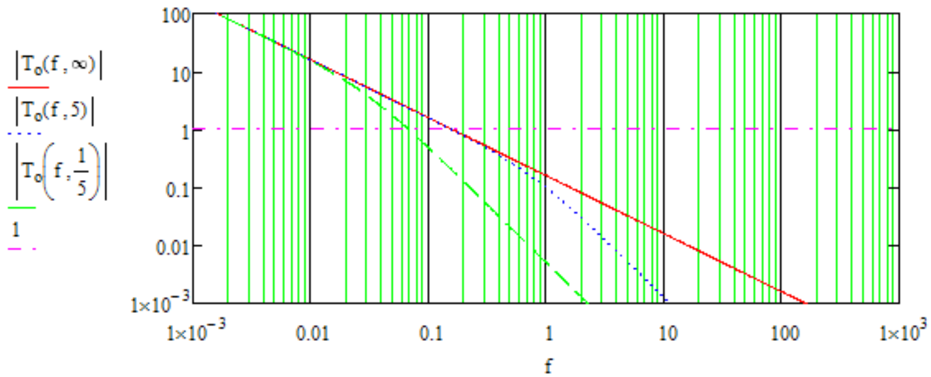
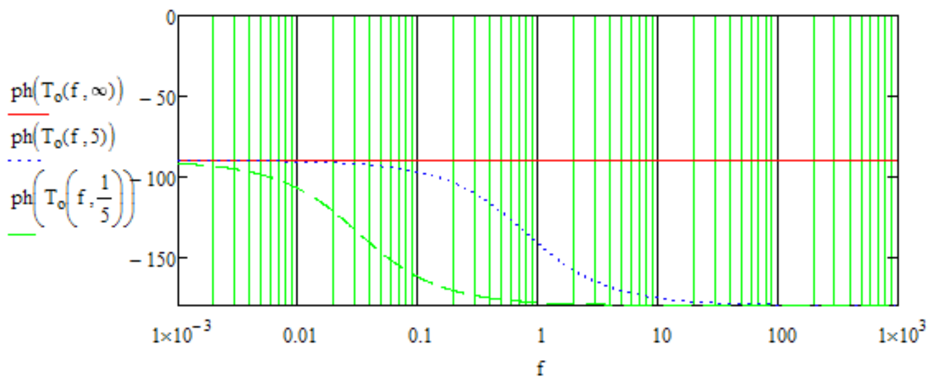
Cascode



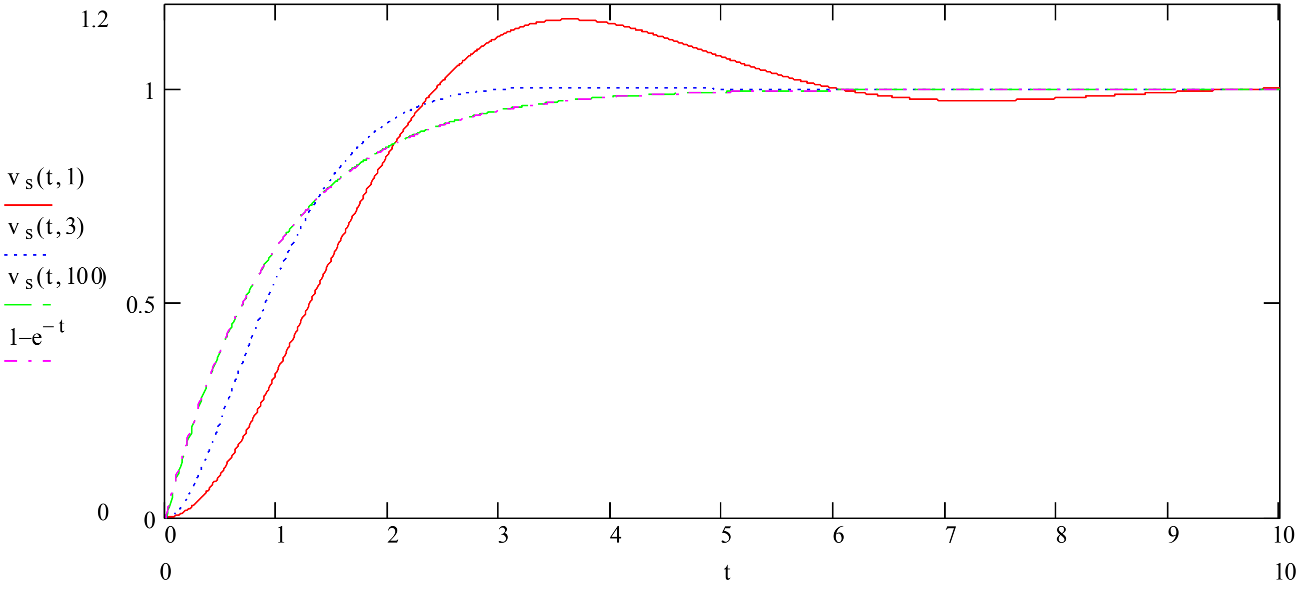
Phase Margin



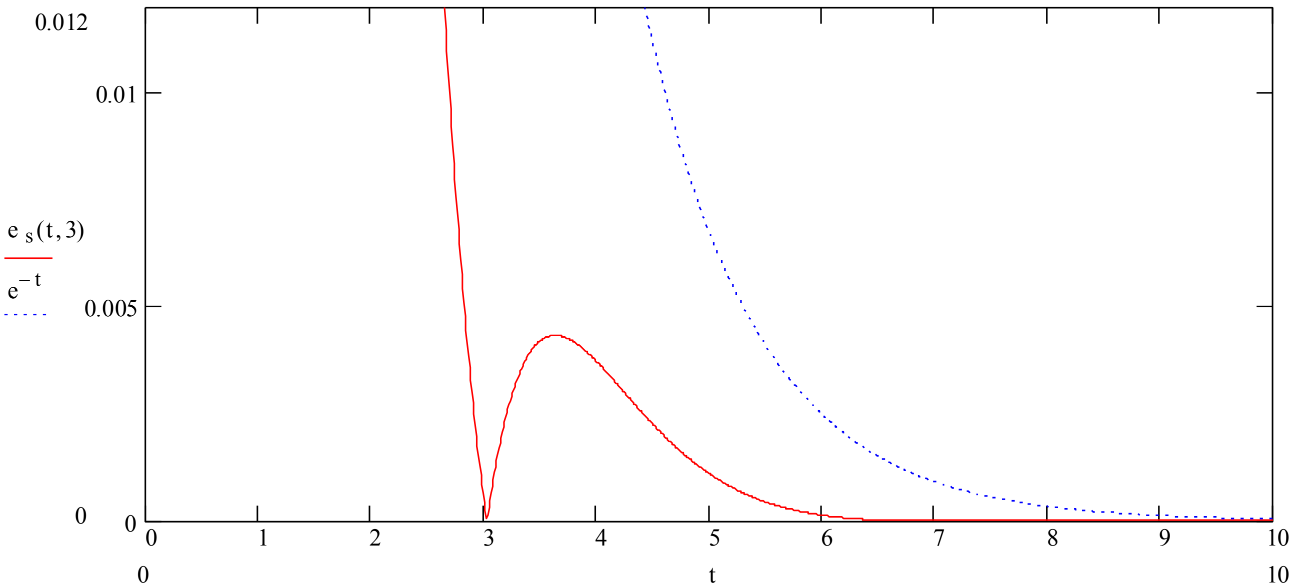


f_{p2}/f_u	Phase Margin
∞	90°
5	~80°
1/5	~28°

Step Response

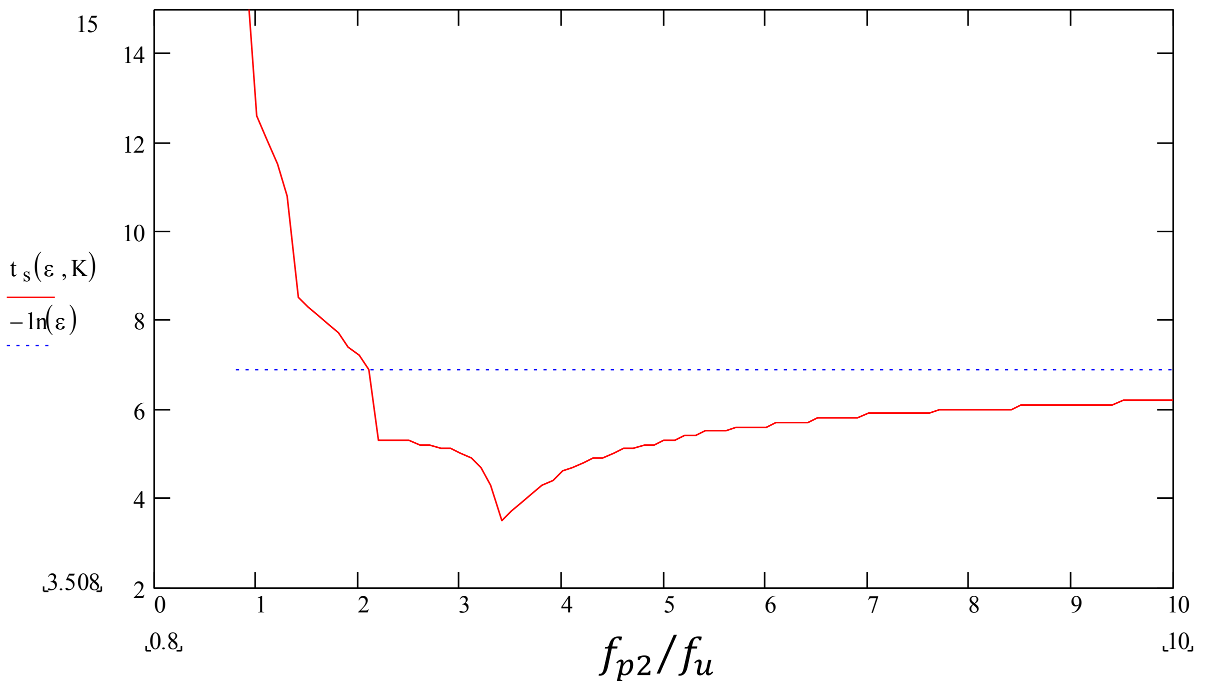


Relative Settling Error for $f_{p2}/f_u = 3$

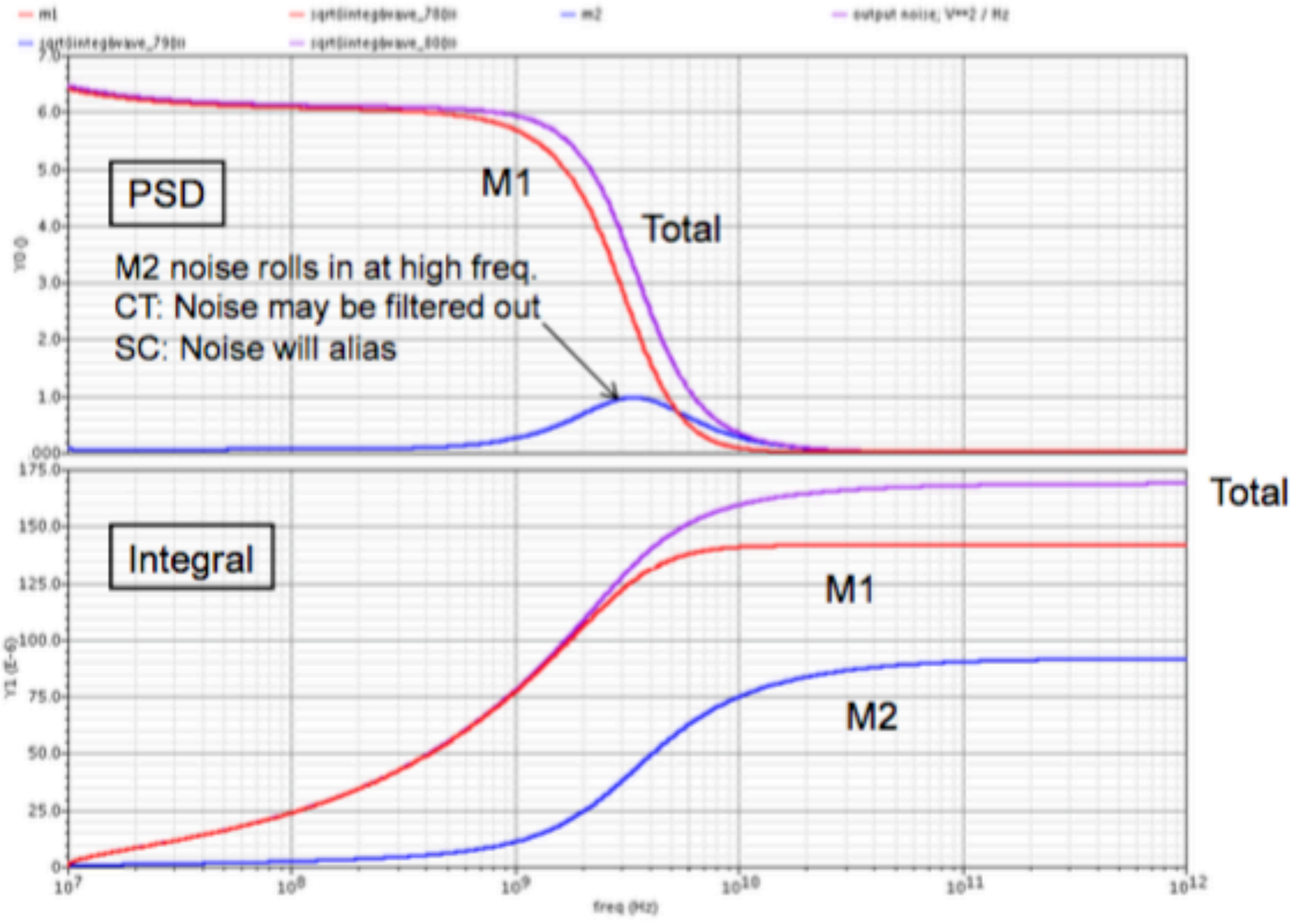


Settling Time versus f_{p2}/f_u

$\varepsilon_d = 0.1\%$



Noise



[B. Murmann]

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Design Example

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Design Example: Specification

Closed-loop gain (magnitude):	$A_{vo} := 2$	
Settling time:	$t_s := 5ns$	$f_{s\_max} := \frac{1}{2 \cdot t_s} = 100\,MHz$
Dynamic settling accuracy:	$\varepsilon_d := 0.02\%$	
Static settling accuracy:	not specified (later)	
Dynamic range at output:	$DR := 10^7$	$10 \cdot \log(DR) = 70$ dB
Supply voltage:	$V_{dd} := 1.8V$	
Power:	minimum	

Design: Gain & Feedback Factor

Sampling capacitance: $C_s := 4pF$ set by previous stage / iterate ...

Feedback capacitance: $C_f := \frac{C_s}{A_{vo}}$ $C_f = 2 \cdot pF$

"Maximum" input capacitance: $C_{x\_max} := 0.7 \cdot (C_s + C_f)$ $C_{x\_max} = 4.2 \cdot pF$

Actual input capacitance (iterate): $C_x := 0.7pF$

Feedback factor: $\beta := \frac{C_f}{C_f + C_s + C_x}$ $\beta = 0.299$

Design: Dynamic Range

Available output voltage range: $V_{opp} := V_{dd} - 400mV$

Total noise at output: $N_{ot} := \dfrac{\frac{1}{2}\cdot\left(\frac{V_{opp}}{2}\right)^2}{DR}$ $\sqrt{N_{ot}} = 156.525\cdot\mu V$

Total noise at output: $N_{ot} = \dfrac{k\cdot T}{\beta}\cdot\left(\dfrac{1}{C_f} + \dfrac{\alpha}{C_{Ltot}}\right)$

OTA noise factor (topology & bias): $\alpha := 4$

Sampling noise (phase 1): $\sqrt{\dfrac{k_B\cdot T_r}{\beta}\cdot\dfrac{1}{C_f}} = 81.89\cdot\mu V$ <? $\sqrt{N_{ot}} = 156.525\cdot\mu V$

Total load capacitance: $C_{Ltot} := \dfrac{\alpha}{N_{ot}\cdot\dfrac{\beta}{k_B\cdot T_r} - \dfrac{1}{C_f}}$ $C_{Ltot} = 3.015\cdot pF$

Total load capacitance: $C_{Ltot} = C_L + (1-\beta)\cdot C_f$

Load capacitance: $C_L := C_{Ltot} - (1-\beta)\cdot C_f$ $C_L = 1.612\cdot pF$

Design: Settling

Settling time (single pole, no slewing): $t_s = -\tau \cdot \ln\left[\varepsilon_d \cdot \left(1 - \beta \cdot \frac{C_f}{C_f + C_L}\right)\right]$

Settling time constant: $\tau := \frac{-t_s}{\ln\left[\varepsilon_d \cdot \left(1 - \beta \cdot \frac{C_f}{C_f + C_L}\right)\right]} = 574.854 \cdot \text{ps}$

Settling time constant: $\tau = \frac{C_{Ltot}}{\beta \cdot g_m}$ $\quad f_u := \frac{1}{2 \cdot \pi \cdot \tau} = 276.862\,\text{MHz}$

Transconductance: $g_m := \frac{C_{Ltot}}{\beta \cdot \tau} = 17.57 \cdot \text{mS}$

Design: Power Dissipation

Minimum cutoff frequency:	$f_T := \frac{1}{2 \cdot \pi} \cdot \frac{g_m}{C_x} = 3.995 \cdot \text{GHz}$
Channel length:	$L_1 := 250\text{nm}$
Current density:	$V_{star} := 120\text{mV}$
Actual fT:	$f_{T\_actual} := 6\text{GHz}$ >? $f_T = 3.995\,\text{GHz}$
Actual Cx (update):	$C_{x\_actual} := \frac{g_m}{2 \cdot \pi \cdot f_{T\_actual}} = 0.466\,\text{pF}$ <? $C_x = 0.7\,\text{pF}$
Bias current:	$I_d := \frac{g_m \cdot V_{star}}{2} = 1.054 \cdot \text{mA}$

Could we go Faster?

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Gain Boosting

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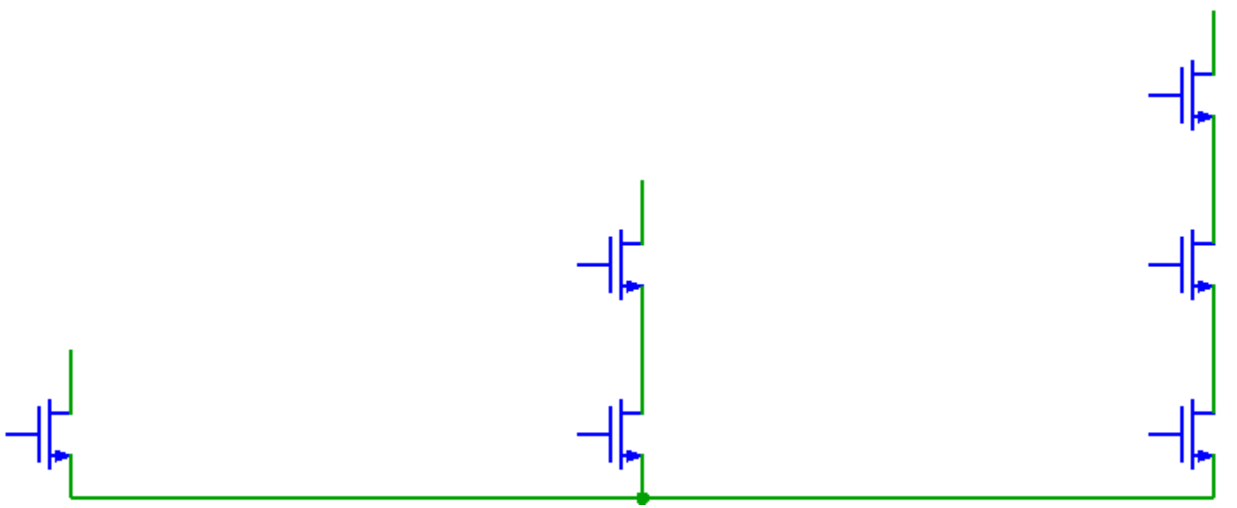
Openloop Gain

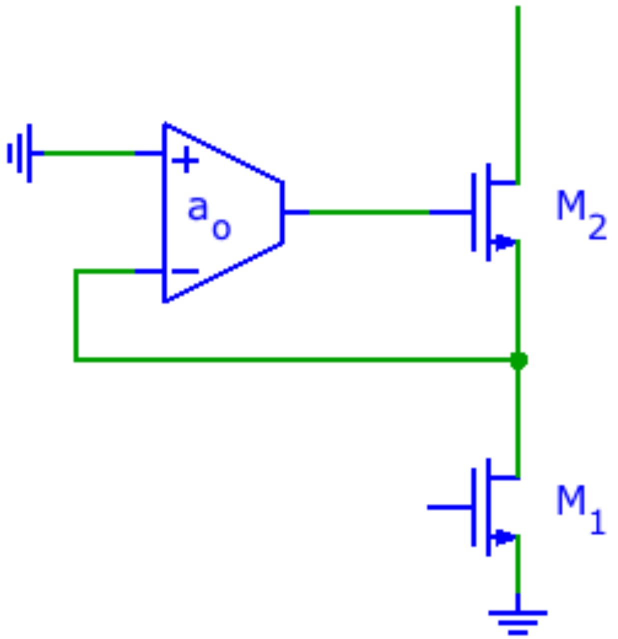
$$a_{vo} = g_m R_o$$

Openloop Gain

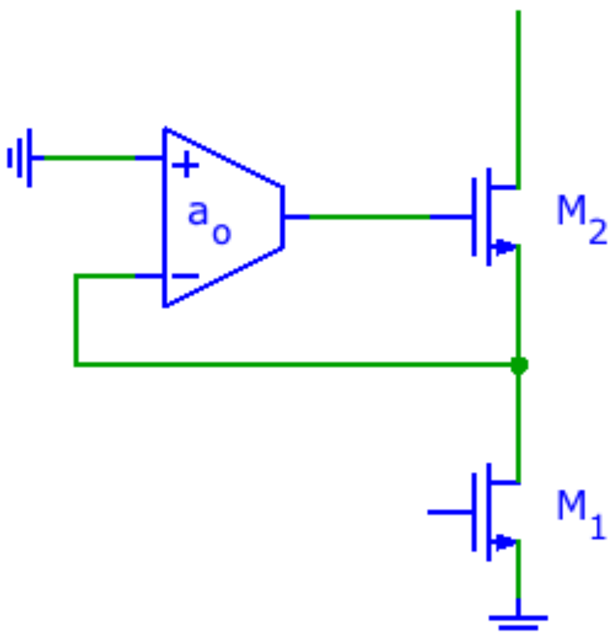
$$a_{vo} = g_m R_o$$



Gain Boosting

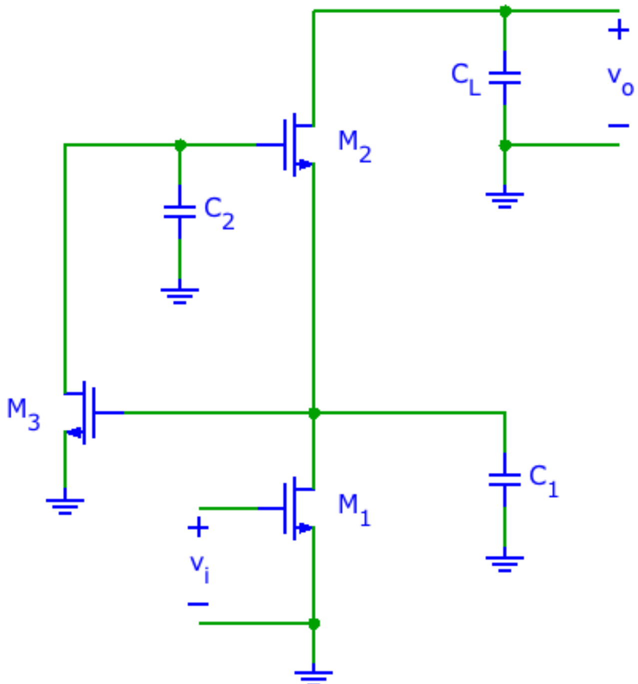


Gain Boosting

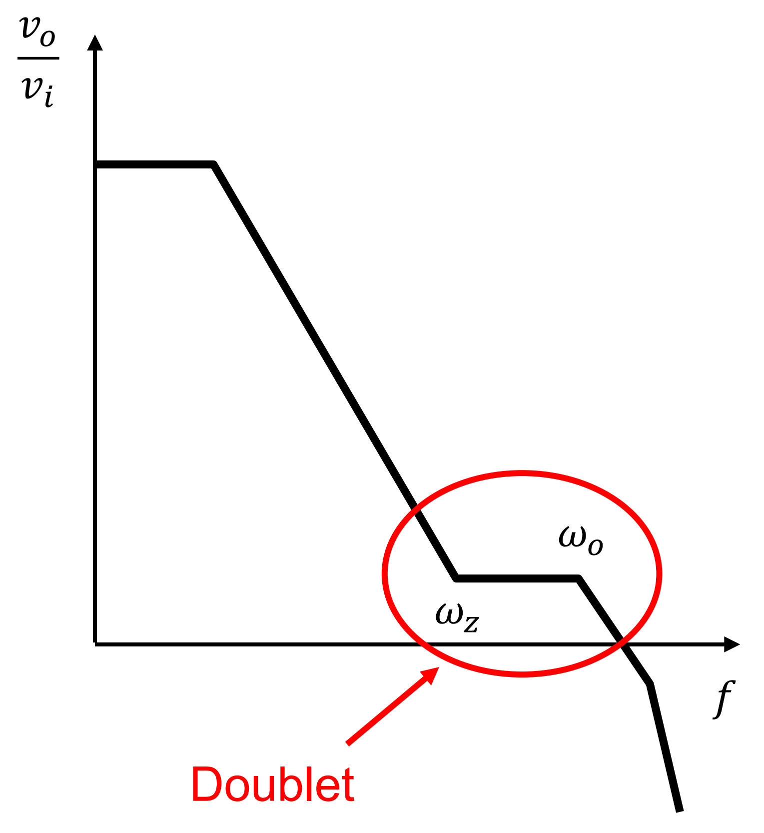


- Use feedback to boost low-frequency output resistance
- References
  - B. J. Hosticka, “Improvement of the gain of MOS amplifiers,” JSSC, Dec. 1979 , pp. 1111-4.
  - E. Sackinger and W. Guggenbuhl, “A high-swing high-impedance MOS cascode circuit”, JSSC, Feb. 1990, pp. 289-298.
  - K. Bult, G. Geelen, “A fast-settling CMOS op-amp for SC circuits with 90-dB DC gain,” JSSC, Dec. 1990 , pp. 1379-84.

High Frequency Analysis



Overall Amplifier Response



Ref: M. Das, "Improved design criteria of gain boosted CMOS OTA with high-speed optimizations," IEEE CAS II, March 2002, pp. 204-7.

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Pole-Zero Doublets

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Pole-Zero Doublets

Ref: Y. Kamath, R. G. Meyer, and P. R. Gray, “Relationship between frequency response and settling time of operational amplifiers,” *IEEE J. Solid-State Circuits*, pp. 347–352, Dec. 1974.

Doublet Settling

- Amplifier model: replace G_{mo} with

$$G_m(s) = G_{mo} \frac{1 + \dfrac{s}{\omega_z}}{1 + \dfrac{s}{\omega_p}}$$

<u>Notation from</u> Y. Kamath, R. G. Meyer, and P. R. Gray, “Relationship between frequency response and settling time of operational amplifiers,” *IEEE J. Solid-State Circuits*, pp. 347–352, Dec. 1974.

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with

$$\omega_p = \beta \omega_{-3dB}, \qquad \omega_{-3dB} \text{ is bandwidth of } T(s)$$

$$\omega_z = \frac{\omega_p}{\alpha}$$

$$\alpha = 1 + \varepsilon \qquad \text{with} \qquad |\varepsilon| << 1$$

- Closed-loop response

$$\frac{V_o}{V_{in}} = -c \frac{1}{1 + s \frac{C_{Leff}}{FG_m(s)}} \cong -\frac{c}{1 + \frac{s}{\omega_{-3dB}}} \left(\frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_{pp}}} \right)$$

with

$$\omega_{-3dB} = \frac{FG_{mo}}{C_{Leff}}$$

$$\omega_{pp} \cong \omega_p$$

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Doublet Step Response

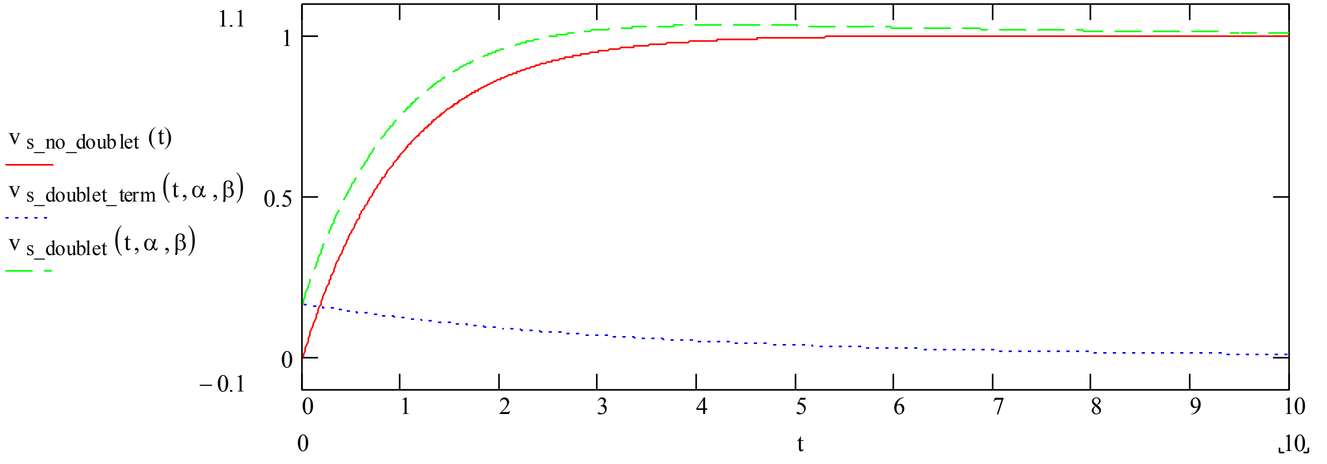
$$v_{o,step}(t) = -cV_{step}\left(1 + Ae^{-t\omega_{-3dB}} + Be^{-t\omega_{pp}}\right)$$

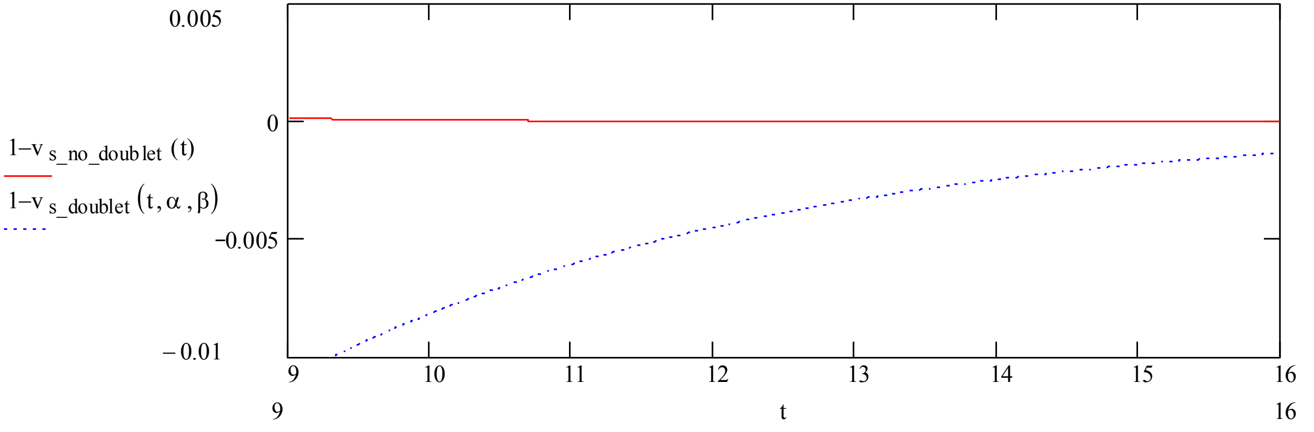
with

$$A \cong -1$$

$$B \cong \varepsilon \frac{\beta}{1-\beta^2}$$

Doublet Example





$\alpha = 1.5$

$\beta = 0.3$

Gain Boosting – Doublets