Due in the “EE 105 box” near 125 Cory Hall by 5pm on Friday 11/9/2012.

Read Sections 11.3–6 in B. Razavi: Fundamentals of Microelectronics

Use the following parameters in all problems, unless otherwise specified (problems from B. Razavi: Fundamentals of Microelectronics use the parameters specified in B. Razavi: Fundamentals of Microelectronics):

<table>
<thead>
<tr>
<th>Device</th>
<th>Parameter values</th>
</tr>
</thead>
<tbody>
<tr>
<td>BJT</td>
<td>$I_s = 1 \text{fA}$, $\beta = 100$, and $V_A = 100 \text{V}$</td>
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<tr>
<td>N/PMOS</td>
<td>$</td>
</tr>
<tr>
<td>NMOS</td>
<td>$\mu_n = 300 \text{cm}^2/\text{Vs}$</td>
</tr>
<tr>
<td>PMOS</td>
<td>$\mu_p = 150 \text{cm}^2/\text{Vs}$</td>
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</table>

Unless otherwise specified, assume room temperature and $V_t = 25 \text{mV}$.


3. Do the Exercise after Example 11.18 in B. Razavi: Fundamentals of Microelectronics. Use a plotting program (e.g. Excel, Matlab, …) for the plot.


13. Design a PMOS common source amplifier with the following specifications:

- Small-signal DC gain $a_{vo} = -5$
- Load resistance $R_L = 5 \, \text{k}\Omega$
- Source resistance $R_s = 5 \, \text{M}\Omega$ (output resistance of the small signal source driving the CS amplifier)
- 3-dB bandwidth $BW = 2 \, \text{MHz}$
- Minimum power dissipation (minimum $I_D$)
- $V_{dd} = 5 \, \text{V}$

Proceed as follows:

a) Draw large and small-signal models of the amplifier.
b) Determine the minimum transconductance $g_m$ required.
c) In the first pass, assume $C_{ol} = 0$. Determine the maximum value of $C_{GS}$ that still meets the specification.
d) Determine the channel length $L$ that meets the specification (this is easy).
e) Determine the minimum value of $V_{GS} - V_{TH}$ that meets the specification.
f) Determine the minimum drain current $I_D$ that meets the specification.
g) Determine the the value of $W$.
h) Verify your design with SPICE. Turn in a printout of the schematic (or netlist) and a bode-plot. Mark the points values where you read off $a_{vo}$ and $BW$. Explain discrepancies between specifications and simulation results.
i) Redo steps (c) to (h) for $C_{ol} \neq 0$. Suggestion: use the Miller approximation.
j) By what percentage did you have to increase $I_D$ due to finite $C_{ol}$?

Look at the notes for lecture L17 on the course web for an example. An ac-analysis example has been added to the LTSpice notes.

Note: Finding a good sequence of steps that minimizes iteration is one of the challenges of design. In this problem you are given a lot of help, increasingly you will have to find an appropriate approach yourself. Unlike most design problems, this one does not require iteration—provided you use the right approach.