Due in the “EE 105 box” near 125 Cory Hall by 5pm on Friday 11/2/2012.

Read Section 11.2 in B. Razavi: Fundamentals of Microelectronics

Use the following parameters in all problems, unless otherwise specified (problems from B. Razavi: Fundamentals of Microelectronics use the parameters specified in B. Razavi: Fundamentals of Microelectronics):

<table>
<thead>
<tr>
<th>Device</th>
<th>Parameter values</th>
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<tbody>
<tr>
<td>BJT</td>
<td>( I_s = 1 \text{ fA}, \beta = 100, \text{ and } V_A = 100 \text{ V} )</td>
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<tr>
<td>NMOS</td>
<td>(</td>
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<td>PMOS</td>
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Unless otherwise specified, assume room temperature and \( V_t = 25 \text{ mV} \).

1. The MOS channel resistance depends on the region of operation of the device. In Midterm 2, several of you were confused about this (indicated by “blindly ?” applying the \( \lambda I_D \) equation). The objective of this problem is to shed light on this.
   a) Plot (using an appropriate program) \( I_D \) versus \( V_{DS} = 0 \ldots 5 \text{ V} \) for an NMOS transistor with \( V_{GS} = 3 \text{ V} \). For which value of \( V_{DS} \) does the transistor enter saturation? In what region of operation is it for smaller values of \( V_{DS} \)?
   b) Add the I/V characteristics of 1 k\( \Omega \) and 100 k\( \Omega \) resistors to the plot from part (a).
   c) Derive analytical expressions for the small-signal transistor output resistance \( r_o \) for \( V_{DS} = 0, 2, \) and \( 4 \text{ V} \).
   d) Calculate the small-signal transistor output resistance \( r_o \) for \( V_{DS} = 0, 2, \) and \( 5 \text{ V} \) and add them to the plot from part (a). Verify that the slopes of the I/V characteristics of the different \( r_o \)’s are tangential to the transistor I/V characteristics at their respective values of \( V_{DS} \).

2. Analyze the amplifier shown below for \( V_{dd} = 3.3 \text{ V}, V_O = V_{dd}/2, W_1 = 5 \mu \text{m} \) and \( W_2 = 8 \mu \text{m} \) and \( L_1 = L_2 = 500 \text{ nm} \). \( M_2 \) is biased in saturation.
   a) What is the region of operation of \( M_1 \)?
   b) Draw the small-signal model and calculate the values of all small-signal parameters. Beware: \( |V_{DS1}| \ll 2(V_{GS1} - V_{TH}) \).
   c) Derive an algebraic expression for the small-signal voltage gain \( a_v = v_o/v_i \). You may use the shorthand \( r_x \parallel r_y \).
   d) Calculate the value of \( a_v \).
3. Design a circuit such that \( v_o = r_x i_s \) with \( r_x = 10 \, \text{k}\Omega \pm 2\% \) using a single NPN transistor \((V_A = 0 \, \text{V})\) and as many resistors and (ideal) bias sources (current or voltage) as you like (fewer is better and helps avoid mistakes). The value of \( R_s \) varies in the range \( 1 \ldots 10 \, \text{M}\Omega \). The source \( i_s \) is a reverse biased diode and requires \( V_s \) in the range \( 2 \, \text{V} \leq V_s \leq 3 \, \text{V} \) to work properly. Stay close to the minimum power dissipation (not more than 2x).

Use the following sequence (you may need to iterate):

a) To familiarize ourselves with the problem, let’s set \( R_s \to \infty \) and not worry about the value of \( V_s \) or sign of \( v_o \) (this part only!). Design a circuit such that \( v_o = r_x i_s \). Note: you won’t need a transistor!

b) Now let’s add the finite \( R_s \). Does our first-cut design still meet the specification? Why not?

c) Now comes the “crux” in design: we need an idea! I’ll make a suggestion: could we solve our problem with an amplifier? How insightful! What would be the “ideal” input resistance \( R_i \) (zero or infinity) of the amplifier?

d) Which amplifier topologies (CE, CB, CC) ideally (i.e. \( g_m \to \infty, r_i \to \infty, \) and \( r_o \to \infty \)) meet the requirement from part (a)?

e) Consider each configuration (CE, CB, CC), still assuming ideal characteristics (\( g_m \to \infty, r_i \to \infty, \) and \( r_o \to \infty \)). For each explain briefly why it’s a candidate or not. Note: review your notes and get help in office hours if you feel that even with idealizing assumptions no amplifier configuration addresses the problem of finite \( R_s \).

f) Draw a prototype large signal model including all biasing elements. You may need to iterate, e.g. modify or add biasing elements during the design process.

g) Draw the small-signal diagram and determine the small-signal parameters required to meet the specifications.

h) Calculate the large signal parameters including the values of all bias sources.

i) Verify with SPICE that your circuit meets the specifications. Turn in a printout of schematic or netlist (from SPICE) and a graph showing \( V_o \) versus \( I_s \) for \( R_s = 1 \, \text{M}\Omega, R_s = 10 \, \text{M}\Omega \) and \( V_s = 2 \, \text{V}, V_s = 3 \, \text{V} \) (a total of 4 traces!). Add the \( I/V \) characteristic of a \( 10 \, \text{k}\Omega \) resistor to your SPICE output (why?). For each trace in your SPICE output, mark the region of \( I_s \) for which meets the specification.

4. Do Problem 7.57 in B. Razavi: Fundamentals of Microelectronics. Remove \( R_G \) from the circuit and replace \( C_1 \) with a bias voltage source. Replace \( C_2 \) with a short circuit. Remember: use parameters specified in B. Razavi: Fundamentals of Microelectronics, not the ones listed at the head of the assignment!


