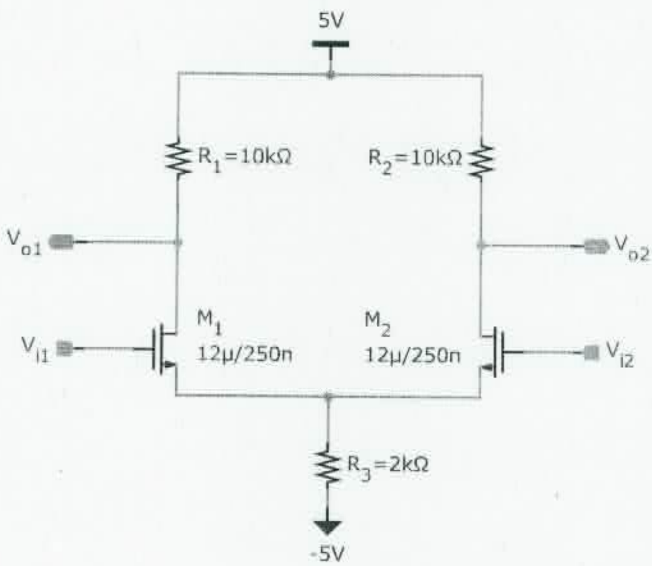
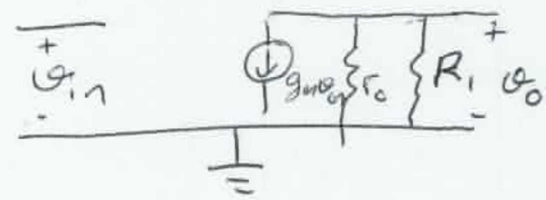
1. In the circuit below, V_{ic} is adjusted such that $V_{oc} = 0\,\text{V}$.
   a) Draw the low-frequency small-signal differential-mode half-circuit model. Calculate the values of all low-frequency small-signal parameters (r_o's, etc.).
   b) Calculate the value of the low-frequency small-signal differential-mode gain, A_{dm}, of the circuit.
   c) Draw the low-frequency small-signal common-mode half-circuit model. Specify the values of all low-frequency small-signal parameters.
   d) Calculate the value of the low-frequency small-signal common-mode gain, A_{cm}, of the circuit.
   e) Because of manufacturing imperfections, the values of resistors R_1 and R_2 are slightly different: $R_1 = R_o + \Delta R/2$ and $R_1 = R_o + \Delta R/2$ with $R_o = 10\,\text{k}\Omega$ and $\Delta R = 0.05 R_o$. Calculate the low-frequency small-signal common-mode to differential gain, A_{cdm}, and the common-mode rejection ratio, CMRR.
   f) Describe a circuit modification resulting in at least a two-orders-of-magnitude improvement of the CMRR. You do not need to design the modification.



a)



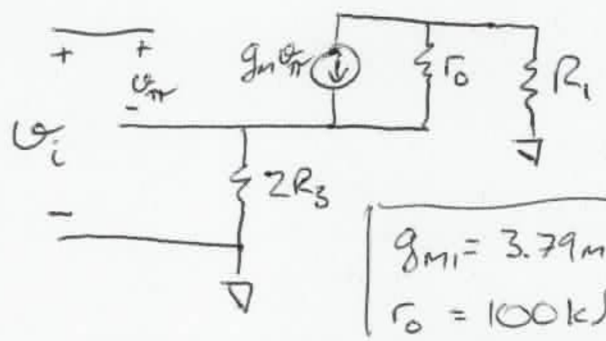
$$I_D = \frac{5\,\text{V}}{10\,\text{k}\Omega} = 0.5\,\text{mA}$$

$$g_{m1} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = 3.79\,\text{m}$$

$$r_o = \frac{1}{\lambda I_D} = 100\,\text{k}\Omega$$

b) $A_{DM} = -g_{m1}(R_1 \| r_o) = 34.5$

c)



$g_{m1} = 3.79\,\text{mS}$

$r_o = 100\,\text{k}\Omega$

d) $$A_{CM} = \frac{g_{m1} R_1}{1 + 2 g_{m1} R_3} = 2.345$$

e) $$A_{CDM} = \frac{\Delta R}{2R_3 + \frac{1}{g_{m1}}} = 0.117$$

$$\text{CMRR} = \frac{A_{DM}}{A_{CDM}} = 323.6$$

f) Replace R_3 with a current source, source resistance at least $100\times R_3$.

(2) First try: current mirror $R_{OUT} = r_o = \frac{1}{\lambda I_D} = 1.275\ M\Omega$ X

$\lambda = 0.02V^{-1}$, $I_D = 39\mu A$

doesn't meet spec ⇒ try cascode

Second try: cascode $R_{OUT} = g_m r_o^2$ — (1)

$$g_m = \frac{2I_D}{V_{GS}-V_{TH}} = \frac{2I_D}{\sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}}} = \sqrt{2I_D \mu_n C_{ox}\frac{W}{L}} \quad \text{— (2)}$$

$$r_o = \frac{1}{\lambda I_D} \quad \text{— (3)}$$

Combine equations (1), (2), (3):

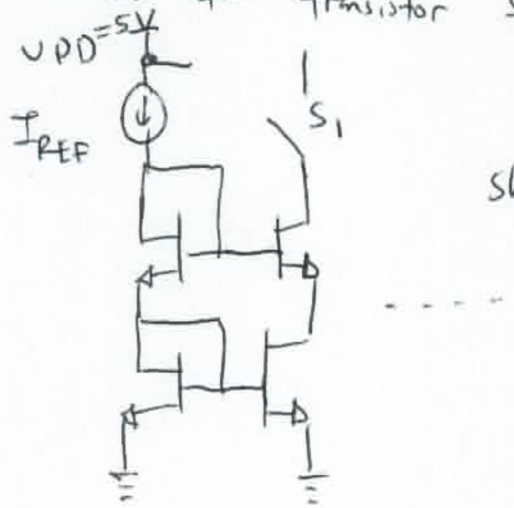
$\lambda = 0.02V^{-1}$, $I_D = 39\mu A$, $\mu_n = 300 cm^2/Vs$

$C_{ox} = 10 \frac{fF}{\mu m^2}$, $L = L_{min} = 180nm$, $W = 1\mu m$

$R_{OUT} = 587\ M\Omega$ ✓

meets spec

We could lower R_{OUT} to $10M\Omega$ and size W accordingly to minimize the transistor sizes.



Showing cascode biasing is important in schematic

Q3)

$$\omega_{3dB} = \frac{1}{C_s R_{in}}$$

$$R_{in} = \frac{1}{g_m}$$

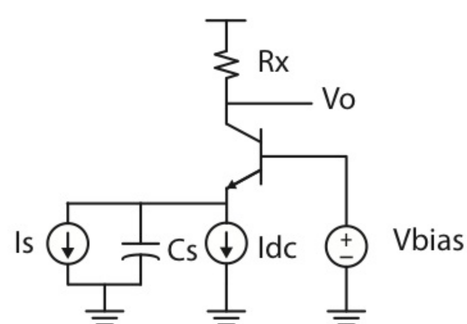
$$2\pi * 500MHz = \frac{1}{10pF * R_{in}}$$

$$R_{in} = 31.8\Omega$$

$$R_{in} = \frac{1}{g_m} \Rightarrow g_m = 31.4mS$$

$$g_m = \frac{I_C}{V_T} \Rightarrow I_C = I_{dc} = 785\mu A$$

$$V_{0,Low\ Frequency} = i_s * R_X \Rightarrow R_X = 1k\Omega$$



Q4)

We know from previous that the resistance looking down from the output node is:

$$R_{0,Down} \approx g_m {r_o}^2$$

This resistance is probably much larger than 2k so we can assume the low frequency gain is:

$$a_v = -g_m R_L \Rightarrow g_m = \frac{10}{2k} = 5mS$$

The dominant pole is in input since the resistance is larger than output (R_L) and the cascade node ($1/g_m$). Also the capacitor is larger since there is miller effect and the gate-source capacitor.

$$\omega_{3dB} = \frac{1}{R_s(C_{gs,1} + 2C_{ov,1})}$$

$$2\pi * 800MHz = \frac{1}{R_s\left(\frac{2}{3}WLC_{ox} + WC_{OV} + 2WC_{OV}\right)}$$

$$2\pi * 800MHz = \frac{1}{10K\left(\frac{2}{3}W0.18 * 10e - 15 + 3W * 0.2e - 15\right)}$$

$$W \approx 11.05\mu m$$

$$g_m = \sqrt{2\frac{W}{L}\mu_n C_{ox} I_D}$$

$$I_D = 678\mu A$$

$$V_{dsat} = \frac{g_m}{\frac{W}{L}\mu_n C_{ox}} = 270mV$$

$$V_{GS} = V_{dsat} + V_{Th} = 670mV$$

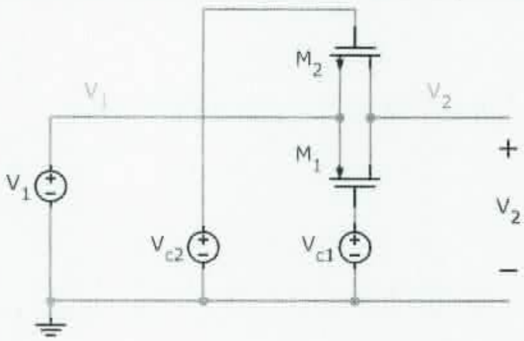
$$V_{Bias,min} = V_{dsat} + V_{GS} = 940mV$$

$$r_0 = \frac{1}{\lambda I_D} = \frac{1}{0.02 * 678e - 6} = 73.7k\Omega \Rightarrow g_m r_o^2 = 27.2M\Omega!$$

5. In the circuit below, M_1 and M_2 are used as switches to control current flow between nodes V_1 and V_2. The control voltages V_{c1} and V_{c2} are set to 0 V and 3 V to turn the switch on, and 3 V and 0 V to turn the switch off.

   Determine the minimum width of M_1 and M_2 required such that the maximum resistance R_{on} between nodes V_1 and V_2 is $10\,\Omega$ when the switch is on and V_1 varies between 0 V and 3 V for $V_2 \approx V_1$. Choose $L_1 = L_2 = 180\,\text{nm}$. For which value of V_1 does R_{on} reach its maximum?

   Relevance: thousands of switches like this one tick along in the analog-to-digital and digital-to-analog converters used in audio and video cards, cameras, or radios.



$$R_{on} = R_{on1} \| R_{on2}$$

M_1, M_2 in triode:

$$R_{on,1} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_1 - V_{c1} - |V_{TH}|)} \qquad V_1 - V_{c1} > |V_{TH}|$$

$$R_{on,2} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{c2} - V_1 - V_{TH})} \qquad V_{c2} - V_1 > V_{TH}$$

$$R_{on} = \frac{1}{\frac{1}{R_{on1}} + \frac{1}{R_{on2}}} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_1 - 0.4V) + \mu_n C_{ox}\left(\frac{W}{L}\right)_2 (2.6 - V}$$

Set $W_1 = 2W_2$

$$R_{on,max} = \frac{1}{2\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (2.2V)} = 10\,\Omega \qquad \boxed{0.4 < V_1 < 2.6\,V}$$

$$\boxed{W_2 = 27.3\,\mu m, \quad W_1 = 54.5\,\mu m}$$

(6) (a) $$\frac{I_{D1}}{I_{D2}} = \frac{\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{DD}-V_G-V_{TH})^2}{\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD}-V_G-V_{TH})^2} = \frac{W_1}{W_2} = \frac{1}{10}$$

(b) $$\left.\begin{aligned} I_{d1} &= I_{C1} = I_s e^{V_{BE1}/V_T} \\ I_{d2} &= I_{C2} = I_s e^{V_{BE2}/V_T} \end{aligned}\right\} \frac{I_{D1}}{I_{D2}} = \frac{1}{10} = e^{(V_{BE1}-V_{BE2})/V_T} \quad -(1)$$

$$V_{BE1} - V_{BE2} = (V_B - V_{E1}) - (V_B - 0) = -V_{E1} = I_{D1} R_1 \quad -(2)$$

Combine (1) & (2): $$\boxed{I_{D1} = \frac{kT}{qR_1}\ln(10)}$$

T	VDD	I_{D1}
300K	3V	59.5 μA
200K	3V	39.7 μA
300K	5V	59.5 μA

(c) The mobility dependence cancels for I_{D1}
The transistors are also at the same temperature