Name & SID: ____________________________

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- Open-book, two 8.5 by 11 inch page of handwritten notes (two sided)
- All exam questions have equal weight.
- Write all your work and answers on the exam sheets.
- Show your work (large and small-signal circuit diagrams, analysis/design equations).
- **Make (and verify!) appropriate assumptions.** For example, transistor $r_o$ has often—but not always—negligible (< 3%) effect on circuit operation. Ditto for intrinsic and extrinsic device capacitors.
- Clearly mark results with a box around them
- Cross out incorrect answers. If you present two or more inconsistent answers we invariably grade the wrong one.
- Notation: $V_x = V_X + v_x$, where $V_X$ is the large signal bias and $v_x$ is the small signal value.

Unless otherwise specified, use the following parameters:

<table>
<thead>
<tr>
<th>Device</th>
<th>Parameter values</th>
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<tbody>
<tr>
<td>BJT</td>
<td>$I_s = 1\ \text{fA}$, $\beta = 100$, and $V_A = 100\ \text{V}$</td>
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<tr>
<td>N/PMOS</td>
<td>$</td>
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<td></td>
<td>$C_{ox} = 10\ \text{fF}/\mu\text{m}^2$, $C_{dl} = 0.2\ \text{fF}/\mu\text{m}$, $C_{SB} = C_{DB} = 0$</td>
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<tr>
<td>NMOS</td>
<td>$\mu_n = 300\ \text{cm}^2/\text{Vs}$</td>
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<tr>
<td>PMOS</td>
<td>$\mu_p = 150\ \text{cm}^2/\text{Vs}$</td>
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<td>—</td>
<td>$V_t = 25\ \text{mV}$</td>
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1. In the circuit below, \( V_{ic} \) is adjusted such that \( V_{oc} = 0 \) V.

   a) Draw the low-frequency small-signal differential-mode half-circuit model. Calculate the values of all low-frequency small-signal parameters (\( r_o \)'s, etc.).

   b) Calculate the value of the low-frequency small-signal differential-mode gain, \( A_{dm} \), of the circuit.

   c) Draw the low-frequency small-signal common-mode half-circuit model. Specify the values of all low-frequency small-signal parameters.

   d) Calculate the value of the low-frequency small-signal common-mode gain, \( A_{cm} \), of the circuit.

   e) Because of manufacturing imperfections, the values of resistors \( R_1 \) and \( R_2 \) are slightly different: \( R_1 = R_o + \Delta R/2 \) and \( R_2 = R_o - \Delta R/2 \) with \( R_o = 10 \) k\( \Omega \) and \( \Delta R = 0.05 R_o \). Calculate the low-frequency small-signal common-mode to differential gain, \( A_{cdm} \), and the common-mode rejection ratio, CMRR.

   f) Describe a circuit modification resulting in at least a two-orders-of-magnitude improvement of the CMRR. You do not need to design the modification.
2. You are to design an 8-bit Digital-to-Analog Converter (DAC) based on the circuit shown below. It comprises 255 identical current sources $I_1$ to $I_{255}$, each generating a current $I = 10 \text{ mA} / 255 \approx 39 \mu\text{A}$. Switches $S_1$ to $S_{255}$ control the amount of this current flowing into the load $R_L$. When all switches are open, the current in $R_L$ is zero, and hence $V_o = 0 \text{ V}$. When all switches are closed, the current from all sources flows into $R_L$ and $V_o = 10 \text{ mA} \times R_L = 1 \text{ V}$. Intermediate output voltages are produced by closing some, but not all, switches.

You are to design the circuit in the dashed box shown below. All current sources $I_1$ to $I_{255}$ are identical, and the switches are ideal (you do not need to design them). Use only MOS transistors (n-type and p-type are available) in your design, and the current from the reference $I_{\text{ref}}$ (specify the value needed for your circuit to meet specifications). To meet DAC accuracy requirements, the output resistance of each current source $I_1$ to $I_{255}$ must be at least $10 \text{ M}\Omega$.

Minimize circuit area (i.e. the number and size of the transistors). For simplicity, assume that $\lambda$ does not scale as a function of channel length.

Draw the large-signal circuit diagram of sources $I_1$ and $I_2$ including how the interface to $I_{\text{ref}}$. Specify the size ($W$ and $L$) of all transistors and demonstrate that your circuit meets all requirements (e.g. calculate the output resistance).

Relevance: circuits like this one are used in the VGA interface of computers. Millions of units are shipped every month!
3. Design a circuit replacing the dashed box shown below such that the small-signal transimpedance

$$z_x = \frac{v_o}{i_s} = \frac{R_x}{1 + \frac{s}{\omega_b}}$$

for $R_x = 1 \, \text{k}\Omega$, $\omega_b = 2\pi \times 500 \, \text{MHz}$ and $C_s = 10 \, \text{pF}$. Minimize current consumption. Ignore all capacitors except $C_s$. Draw the complete large-signal circuit diagram, mark the input and output, and specify the values of all components.

Available components: BJTs (n-type and p-type), ideal constant voltage and current sources, resistors.

Relevance: circuits like this one are used in front-end circuits for applications including fiber-optic receivers and cameras.
4. The circuit below is biased such that all transistors are in saturation and the large-signal output voltage $V_O = 0$ V. Determine the minimum value of $V_{Bias}$ required to keep $M_1$ in saturation and the values of $W$ and $I_{DD}$ such that the low-frequency small-signal gain $a_{vo} = \left| \frac{v_o}{v_i} \right| = 10$ and the 3-dB bandwidth of the circuit $f_B = 800$ MHz. Minimize $I_{DD}$. 
5. In the circuit below, $M_1$ and $M_2$ are used as switches to control current flow between nodes $V_1$ and $V_2$. The control voltages $V_{c1}$ and $V_{c2}$ are set to 0 V and 3 V to turn the switch on, and 3 V and 0 V to turn the switch off.

Determine the minimum width of $M_1$ and $M_2$ required such that the maximum resistance $R_{on}$ between nodes $V_1$ and $V_2$ is $10 \, \Omega$ when the switch is on and $V_1$ varies between 0 V and 3 V for $V_2 \approx V_1$. Choose $L_1 = L_2 = 180 \, \text{nm}$. For which value of $V_1$ does $R_{on}$ reach its maximum?

*Relevance:* thousands of switches like this one tick along in the analog-to-digital and digital-to-analog converters used in audio and video cards, cameras, or radios.
6. In this problem, the sensitivity of device parameters to temperature \(T\) is relevant. Use \(V_t = \frac{k_B T}{q_e}\) with \(k_B = 1.38 \times 10^{-23}\) m\(^2\)kg sec\(^{-2}\)K\(^{-1}\) and \(q_e = 1.6 \times 10^{-19}\) C.

a) Determine the ratio of the drain currents \(I_{d1}/I_{d2}\) of \(M_1\) and \(M_2\). Assume both devices are in saturation. Note \(W_1 \neq W_2\).

b) Calculate the drain current \(I_{d1}\) of \(M_1\) as a function of temperature \(T\) and supply voltage \(V_{DD}\) and fill in the table below. Hint: \(V_{BE1} \neq V_{BE2}\).

c) Earlier in the course we have seen that electron and hole mobility depend on temperature. Explain the effect on \(I_{d1}\).

Relevance: Most integrated circuits contain a reference like this one or a variation thereof. The current in \(M_1\) is mirrored to circuit elements all over the chip.

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<thead>
<tr>
<th>(T)</th>
<th>(V_{DD})</th>
<th>(I_{d1})</th>
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<tbody>
<tr>
<td>300 K</td>
<td>3 V</td>
<td></td>
</tr>
<tr>
<td>200 K</td>
<td>3 V</td>
<td></td>
</tr>
<tr>
<td>300 K</td>
<td>5 V</td>
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![Circuit Diagram](image-url)