Level Conversion for Dual-Supply Systems

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ABSTRACT

Dual-supply voltage design using a clustered voltage scaling (CVS) scheme is an effective approach to reduce chip power. The optimal CVS design relies on a level converter (LC) implemented in a flip-flop to minimize energy, delay, and area penalties due to level conversion. Novel flip-flops presented in this paper incorporate a half-latch LC and a precharged LC. These flip-flops are optimized in the energy-delay design space to achieve over 30% reduction of energy-delay product and about 10% savings of total power in a CVS design as compared to the conventional flip-flop. These benefits are accompanied by 24% robustness improvement and 18% layout area reduction.

Categories and Subject Descriptors

B.6.1 [**Design Styles**]: Sequential circuits – *design styles*.

General Terms

Design, Performance.

Keywords

Level conversion, dual-supply voltage, flip-flop.

1. INTRODUCTION

Power dissipation is a limiting factor in both high-performance and mobile applications. Independent of application, desired performance is achieved by maximizing operating frequency under power constraints that may be dictated by battery life, chip packaging and/or cooling costs. Lowering supply voltage results in a quadratic reduction in power dissipation but significantly impacts delay. In constant-throughput applications, this performance loss is recovered by increased pipelining or parallelism [1], but it increases the latency of the design.

A multiple supply voltage design in which a reduction in supply voltage is applied only to circuits outside critical paths can save power without sacrificing either throughput or latency. A key challenge in designing efficient multiple-supply circuits involves minimizing the cost of level converters (LC) placed on the boundary between low-V_{DD} (V_{DDL}) and high-V_{DD} (V_{DDH}). A level converter restores a V_{DDH} swing from a V_{DDL} signal in order to prevent DC current due to incomplete PMOS cut-off. A PMOS cross-coupled LC [12] is widely used to suppress the DC current.

While cost-minimized level conversion has been proposed for a custom data-path design [8], an effective solution for synthesized

ASICs is necessary. Dual-supply voltage (dual-V_{DD}) design using a clustered voltage scaling (CVS) scheme proposed in [11] combines a level converter with a flip-flop in order to minimize area and delay penalties, but very few level-converting flip-flop (LCFF) structures have been investigated [3,5].

In this paper, we present several new LCFF circuits which exhibit improved energy-delay product values and reduced system-level power without incurring robustness degradation or significant area increase over a conventional flip-flop.

2. DUAL-SUPPLY DESIGN

2.1 Optimal V_{DDL} Selection

A theoretical model to investigate power reduction via CVS is proposed in [3]. We employ this top-down approach to determine the V_{DDL}/V_{DDH} ratio for LCFF optimization and comparisons. By using parameters for 0.13μm technology, the optimal V_{DDL} is found to sit between 60% and 70% of V_{DDH} regardless of path delay distribution shapes. The latter value is chosen for higher noise immunity of V_{DDL} signals against V_{DDH} noise.

2.2 Dual-V_{DD} CVS Simulation

A Perl-script-based simulator is implemented to estimate power reduction of a dual-V_{DD} CVS system. As illustrated in Fig. 1, the simulator models the initial single-V_{DD} design as a series of paths each of which consists of a chain of fanout-of-four (FO4) inverters (IV) sandwiched between two flip-flops. Three different logic depths - 12, 20, and 40 FO4 IV unit delays - are employed to evaluate their impact on power saving of a CVS system.

Initially, all flip-flops and IVs are V_{DDH} cells. The first step substitutes all V_{DDH} flip-flops with LCFFs. Since all LCFFs investigated are driven by a V_{DDL}-swing clock, this substitution can reduce clocking power significantly [12]. For negative slack
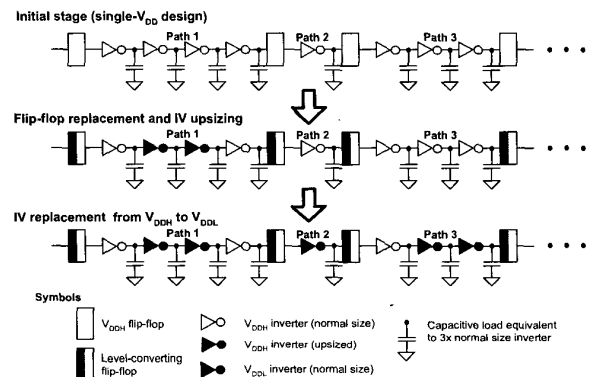

Figure 1. Dual-V_{DD} CVS simulation

paths caused by the increased delay of LCFFs, the V_{DDH} IVs are upsized to maintain the original clock cycle time. The FO3-equivalent capacitive load connected to the output of each V_{DDH} IV remains unchanged. Then, V_{DDH} IVs are replaced with V_{DDL} IVs in each non-critical path until positive slack disappears. This replacement proceeds in reverse order from the end of each path to build the CVS structure. Finally, the simulator calculates the power of the CVS structure and compares it with the power of the initial single-V_{DD} design. The impact of different LCFFs and different logic depths on power saving is quantified which is not possible using a theoretical approach [3].

3. LEVEL-CONVERTING FLIP-FLOPS

3.1 Flip-Flop Characterization Metrics

Two important metrics to characterize flip-flop timing are d-q delay, D, and race immunity, R [6]. The former parameter consists of setup time, t_{setup} and clk-q delay, t_{clk-q} while the latter is determined as a difference between t_{clk-q} and hold time, t_{hold}. We introduce another timing metric, sampling window S, which is a sum of t_{setup} and t_{hold}. Average flip-flop energy per clock cycle defined in [6], E, is employed to characterize flip-flop energy. The energy-delay product, EDP [2,6], is calculated from D and E to compare the energy-delay trade-off among the flip-flops. HSPICE is used to obtain the parameter values under the simulation conditions given as follows; channel length is $0.13\mu m$, V_{DDH} is set to 1.20V, V_{DDL} to 0.84V (= 70% of V_{DDH}), and temperature is 27°C.

3.2 Flip-Flop Optimization Method

The flip-flop test bench is similar to one in [9] with flip-flop input capacitance constrained to be less than 3fF and output load fixed at 17fF. Data transition probability for calculating E is assumed to be 10% of clock activity (for both 0→1 and 1→0) [10].

We use the HSPICE built-in optimizer to explore the E-D design space and to find the optimal transistor sizing of each LCFF circuit which gives the minimal EDP value. Transistor sizes in each flip-flop are changed by the optimizer to determine a minimal flip-flop energy under a given t_{clk-q} constraint. Figure 2 is obtained by repeating this optimization with different t_{clk-q} targets with added t_{setup} to obtain D. The plot touching the minimal EDP curve gives the optimal sizing for each LCFF as indicated by a solid symbol.

3.3 Master-Slave Level-Converting Flip-Flops

Figure 3 depicts the first of the designed LCFFs, MSHL, which is a M-S latch pair with a half-latch LC embedded on its slave side. The shaded gates in all the schematics represent V_{DDL} gates and the underlined nodes show V_{DDL}-swing signals. High-level output from the master stage experiences a V_{th} drop across the clocked NMOS (MN1) and the dropped voltage is restored by the pull-up

Figure 2. LCFF optimization in energy-delay space. Minimal *EDP* point for each LCFF is shown by a solid symbol.

inverter loop which is triggered by the series NMOS pull-down path (MN2 and MN3). This is commonly used for level restoration in pass-transistor networks. As compared to the conventional M-S LCFF [3] in which a V_{DDL} input is shifted to V_{DDH} by a cross-coupled LC, the simple half-latch implementation has smaller transistor count and reduced clock loading. The conventional LCFF is denoted as MSCC in this paper

3.4 Pulsed Level-Converting Flip-Flops

Pulsed flip-flops frequently exhibit smaller d-q delay, D than M-S flip-flops [10]. By designing a pulsed LCFF, more timing slack from the reduced D can be utilized for the additional substitution of V_{DDH} gates by V_{DDL} gates for increased power savings. Figures 4 and 5 show two types of proposed pulsed LCFFs. In both cases, the outputs are inverted in order to decouple the feedback IV loop by an output IV from the external loading. The pulsed half-latch, PHL, in Fig. 4 has the same topology as the slave portion of MSHL, but its NMOS pass gate (MN1) is driven by a pulsed clock, "ck", generated from "clk".

In contrast to PHL, the pulsed-precharged level converter, PPR, in Fig. 5 realizes level conversion by the precharged circuit where the V_{DDL} signals, "d" and "db" drive only the NMOS evaluation networks to prevent the DC current from flowing through PMOS transistors. Precharge operation on node "x" is completed by the combination of the NMOS precharge device (MN1) and the back-to-back IV loop. Since MN1 has a source-follower connection, it quickly loses its pull-up current as the voltage on node "x" approaches V_{DDL}-V_{th}. The IV loop takes over the remaining precharge operation.
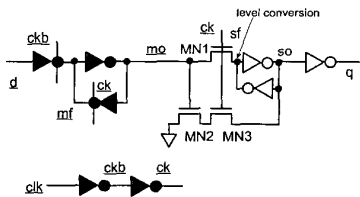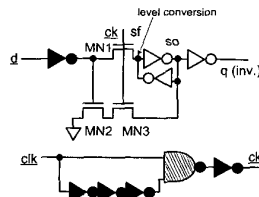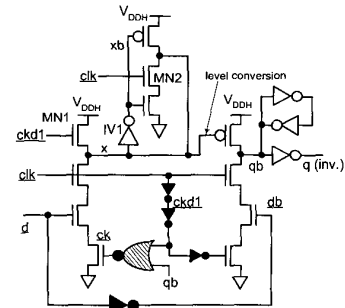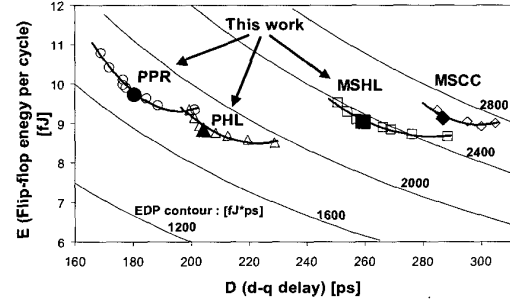

Figure 3. MSHL (M-S, half-latch LC)

Figure 4. PHL (pulsed, half-latch LC)

Figure 5. PPR (pulsed, precharged LC)

The conditional data capture capability [4] is added to avoid unnecessary discharging of "x" when the flip-flop captures two consecutive high inputs on "d".

An LCFF from [5] employs a self-precharging mechanism instead of the clocked precharge device. The circuit needs to have a non-inverting output to trigger self-precharging and incurs additional delay and power. Moreover, self-precharging is not applicable to a transparent latch unlike our source-follower NMOS precharging.

4. COMPARISON

4.1 Flip-flop Performance
Figure 6 compares the three timing metrics of the optimally sized LCFFs. The full length of each bar represents the d-q delay, D which is divided into the sampling window, S and the race immunity, R. The timing of a normal V_{DDH} D flip-flop and a V_{DDL} D flip-flop together with an asynchronous LC is also shown. The cross-coupled PMOS LC [12] is chosen as the asynchronous LC.

The delay sum of the V_{DDL} D flip-flop and the asynchronous LC is far larger than any of the LCFF delay values. This indicates that level conversion in combinational logic incurs significant delay penalty and a LC circuit should be embedded in a flip-flop. All the proposed LCFFs exhibit smaller D than the conventional MSCC. Larger reduction in D is accomplished by PHL and PPR. The delay improvement of these flip-flops is available at the expense of large S (or small R) due to their pulse-driven nature. Race caused by the widened window S, however, cannot be a serious issue in a CVS design since all the short paths preceding the LCFFs are slowed down by replacing V_{DDH} gates with V_{DDL} gates.

The unique benefit of the precharged flip-flop, PPR, is its t_{clk-q} which is comparable to that of the V_{DDH} D flip-flop. This small t_{clk-q} property of PPR is very attractive for a critical path which follows the LCFF.

As indicated by the solid symbols in Fig. 2, an 11% reduction in EDP is achieved by MSHL over MSCC. PPR has the smallest EDP due to its significant decrease in D in spite of the slightly larger E value than that of MSCC. Both of the pulsed LCFFs - PHL and PPR - show more than 30% improvement in EDP.

An evaluation of robustness of the LCFFs to supply noises is also important. Fluctuation of D value caused by ±10% bounce of V_{DDL} and V_{DDH} is shown in Fig. 7. Since the delay spread needs to be budgeted as an uncertainty component with respect to cycle time, its absolute values are compared. The figure includes the fluctuation value for the combination of the V_{DDL} D flip-flop and
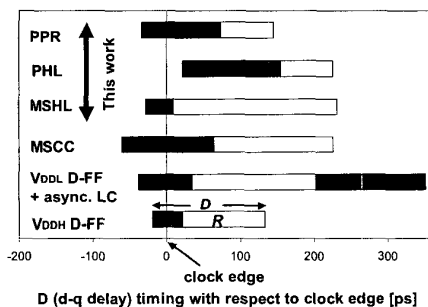

Figure 6. LCFF timing comparison

the asynchronous LC. The three proposed LCFFs yield comparable or smaller fluctuations against MSCC. The maximum of 24% reduction in delay spread is obtained for PHL.

4.2 Flip-flop Layout
Since an LCFF requires two supply voltages, its layout does not comply with the conventional ASIC standard cell layout and several choices have been investigated by previous studies [12,13]. In this work, we employ a double-cell-height architecture in which V_{DDH} and V_{DDL} supplies are available through the top and the bottom Metal-1 rails, respectively, while the ground rail travels at the center of the cell.
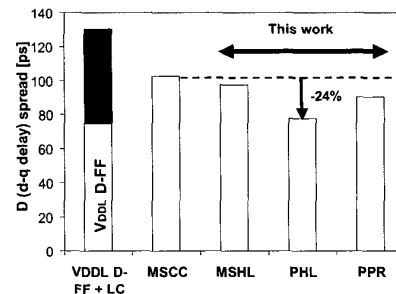

Figure 7. Delay spread for ±10% V_{DDH}/V_{DDL} bounce

Layout patterns of MSCC, MSHL, PHL, and PPR, are shown in Fig. 8. The doubled cell height (= 2 x 12 grid) is shared by all the layouts. MSHL and PHL have smaller area by 18% compared to MSCC, while PPR shows 9% area increase. The layout size is almost proportional to the transistor count which is listed in the figure captions.

4.3 Impact on System-level Performance
The impact of each LCFF on a system-level power is investigated by using the simple dual-V_{DD} CVS simulator and its results are plotted in Fig. 9. The power of the CVS structure normalized to the initial single-V_{DD} power is simulated at different logic depths. Two path delay distributions, lambda and wedge shown by the insets, are tested. Since PHL and PPR have the inverted output, FO1 IV delay and power are added in the CVS simulation for fair comparison.

For both path delay distributions, all the proposed LCFFs are found to lower the CVS power further as compared to a CVS design using the conventional MSCC. The power savings become larger as the logic depth decreases. Since high performance systems employ the reduced logic depth [7], the proposed LCFFs are found to be more attractive for more advanced designs. PHL exhibits the lowest power and its power saving over the MSCC design reaches approximately 10% for both of the delay distributions. Since the wedge-shaped delay distribution contains more critical paths, the LCFFs having smaller d-q delay, D, are more beneficial.

5. CONCLUSIONS
Smaller delay penalty of level-converting flip-flops (LCFF) than a D flip-flop plus an asynchronous level converter is presented. Based on this comparison, three new LCFF circuits are proposed. Each circuit is optimally sized to yield minimal energy-delay
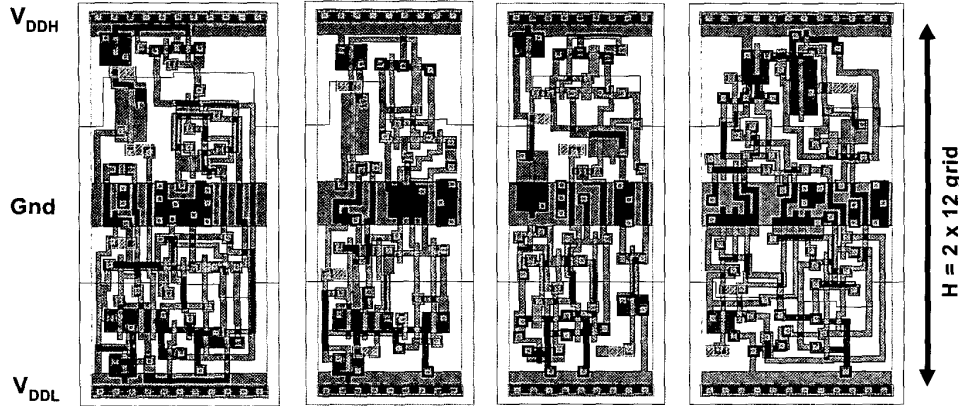
(a) MSCC(11grid, 26Tr) (b) MSHL(9grid, 23Tr) (c) PHL(9grid, 23Tr) (d) PPR(12grid, 31Tr)

Figure 8. LCFF layout patterns employing the double-height architecture. Cell width and transistor count are shown below layouts

product (*EDP*). For the optimized flip-flops, timing, energy, and robustness parameters as well as the layout size are compared with those of the conventional LCFF. Finally, a dual-V_{DD} clustered voltage scaling (CVS) simulator is employed to quantify the system-level power saving of each flip-flop structure at various logic depths. The best overall performance is achieved by the pulsed half-latch (PHL) with over 30% reduction in *EDP* and approximately 10% improvement in system-level CVS power together with 24% better robustness and 18% smaller layout size.

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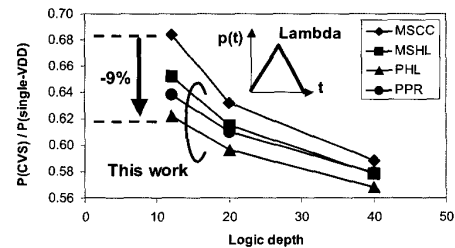
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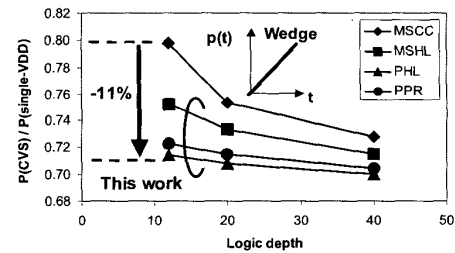
(b)

Figure 9. Dual-V_{DD} CVS system power at different logic depths for two delay distributions: (a) Lambda (b) Wedge

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