

# Use of Phase Delay Analysis for Evaluating Wideband Circuits: An Alternative to Group Delay Analysis

Woorham Bae, Borivoje Nikolić, and Deog-Kyoon Jeong

**Abstract**—A phase delay analysis is proposed against pursuing a flat group delay response for the design of wideband circuits. While it is believed that a large group delay variation introduces a large data-dependent jitter, this brief reconsiders the effectiveness of the group delay analysis in the evaluation of wideband circuits. Because of its own differentiating nature, the group delay provides a good insight on the delay variation at a vicinity of a certain frequency. However, for certain kind of wideband circuits, the group delay analysis cannot provide a sufficient insight since much of useful information is lost or distorted during the differentiating operation. In this brief, the effectiveness of the phase delay analysis is investigated and comparison with a traditional group delay analysis is presented with a theoretical approach and through a few circuit examples.

**Index Terms**—Circuit evaluation, group delay, phase delay, wideband circuit.

## I. INTRODUCTION

Recently, the required bandwidth of wire line communications has been increasing [1], and therefore a number of on-chip bandwidth extension techniques have been proposed [2]–[10]. The importance of evaluating timing distortion of a wideband circuit has also been increasing in order to evaluate such bandwidth extension techniques, because the timing accuracy is as important as the signal-to-noise ratio [11], which is related to a magnitude response of a wideband circuit. A group delay has been a widely used performance metric for evaluating wideband amplifiers and buffers, because it is believed that the group delay provides information on timing distortion caused by a wideband circuit, which is hard to be intuitively informed from a magnitude response. It has also been believed that a flat group delay response across the frequency range of interest assures the quality of the wideband circuit [5], [6], [8], [10].

However, inherently, a phase delay analysis corresponds much more with the classic theory on distortionless transmission [12], compared to the group delay analysis. In this brief, we examine the effectiveness of the group delay evaluation on a wideband circuit and suggest a more precise alternative, a phase delay, by introducing a theoretical approach and giving a few circuit examples.

The remainder of this brief is organized as follows. Section II introduces the basic concepts on the phase delay and group delay analyses, and describes theoretic drawbacks of the conventional group delay analysis. Section III presents *RLC* circuit examples, which support the theoretical examination given in Section II. In addition, a practical design example using a T-coil peaking technique is provided in Section IV. Finally, conclusions are provided in Section V.

Manuscript received April 8, 2017; revised June 12, 2017 and July 12, 2017; accepted August 25, 2017. Date of publication September 8, 2017; date of current version November 22, 2017. (Corresponding author: Deog-Kyoon Jeong.)

W. Bae and B. Nikolić are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA (e-mail: wrbae@eecs.berkeley.edu).

D.-K. Jeong is with the Department of Electrical and Computer Engineering and also with the Inter-University Semiconductor Research Center, Seoul National University, Seoul 151-742, South Korea (e-mail: dkjeong@snu.ac.kr).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TVLSI.2017.2747157

1063-8210 © 2017 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.

See [http://www.ieee.org/publications\\_standards/publications/rights/index.html](http://www.ieee.org/publications_standards/publications/rights/index.html) for more information.

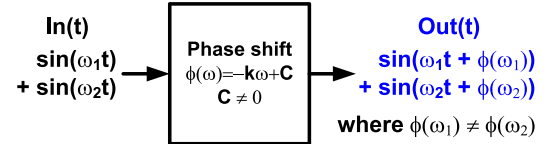


Fig. 1. Linear phase shifter.

## II. BASIC CONCEPT

By definition, the group delay and the phase delay are given as

$$\tau_g(\omega) = -\frac{d\varphi(\omega)}{d\omega} \quad (1)$$

$$\tau_p(\omega) = -\frac{\varphi(\omega)}{\omega} \quad (2)$$

where  $\omega$  is an angular frequency and  $\varphi(\omega)$  is a phase response. It is notable that the group delay is obtained by using a differentiation operation. That is, if there is a nonzero “constant” term in  $\varphi(\omega)$ , this information is lost after the differentiation. Before we decide to discard some information, we must ensure that the information is truly negligible. Let us assume an imaginary transfer function, whose magnitude response is unity across all the frequency and phase response is proportional to the frequency. It may be referred as a linear phase shifter. The phase response of this phase shifter can be expressed as

$$\varphi(\omega) = -k\omega + C \quad (3)$$

where  $k$  and  $C$  are the nonzero and arbitrary constants. Note that the group delay of the linear phase shifter is  $k$  regardless of the frequency being investigated. That is, this transfer function is perfect from the conventional standpoint, because it has a flat magnitude and a flat group delay across overall frequency range. When two combined sinusoidal signals are applied to the input of the linear phase shifter as shown in Fig. 1, however, two sinusoidal components experience a different phase shift. It is noteworthy that there is no signal distortion when the two signals experience the same delay in time. The output of the phase shifter can then be rewritten as

$$\text{Out}(t) = \sin \left\{ \omega_1 \left( t + \frac{\varphi(\omega_1)}{\omega_1} \right) \right\} + \sin \left\{ \omega_2 \left( t + \frac{\varphi(\omega_2)}{\omega_2} \right) \right\}. \quad (4)$$

That is, the first and the second sinusoidal signals experience time delays of  $-\varphi(\omega_1)/\omega_1$  and  $-\varphi(\omega_2)/\omega_2$ , respectively, which is the phase delay. In the case of a linear phase shifter, (4) becomes

$$\text{Out}(t) = \sin \left\{ \omega_1 \left( t - k + \frac{C}{\omega_1} \right) \right\} + \sin \left\{ \omega_2 \left( t - k + \frac{C}{\omega_2} \right) \right\}. \quad (5)$$

Because the time delays experienced by the sinusoid at  $\omega_1$  and  $\omega_2$  are always different from each other, except when  $C = 0$ , the waveform at the output deviates from that at the input, as shown in Fig. 2(a). On the other hand, when  $C = 0$ , the output shows exactly the same waveform as that of the input and is just delayed by  $k$ , as shown in Fig. 2(b). From this observation, it is concluded that neglecting the constant term, which usually happens during the calculation of a group delay, results in a loss of necessary information.

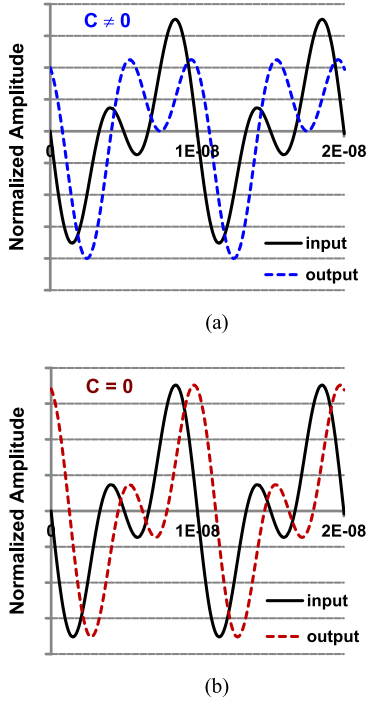


Fig. 2. Calculated waveforms of input and output of the linear phase shifter when  $C$  is (a) nonzero ( $= -\pi/2$ ) and (b) zero ( $f_1 = 100$  MHz and  $f_2 = 200$  MHz).

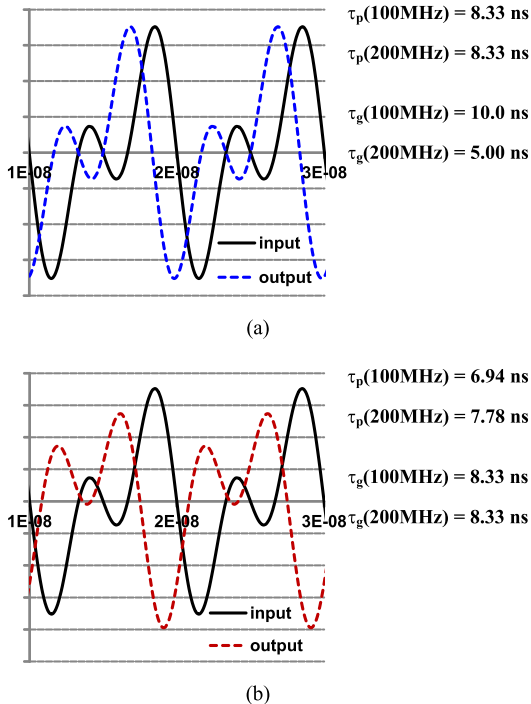
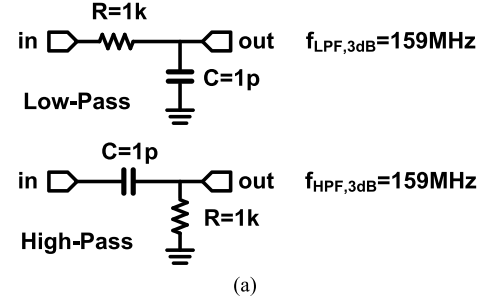


Fig. 3. Calculated waveforms of input and output of the third-order polynomial phase shifter. (a) With the same phase delay. (b) With the same group delay.

Even when  $C = 0$ , the flat group delay may fail to reflect a waveform distortion in some cases. Let us assume a phase shifter, whose phase response is given as a third-order polynomial as follows:

$$\varphi(\omega) = -k_3\omega^3 - k_2\omega^2 - k_1\omega \quad (6)$$



	Frequency	LPF	HPF
Gain	@ 100MHz	0.847	0.532
	@ 200MHz	0.622	0.782
Group Delay	@ 100MHz	717ps	717ps
	@ 200MHz	388ps	388ps
Phase Delay	@ 100MHz	893ps	1.61ns
	@ 200MHz	715ps	535ps

(b)

Fig. 4. (a) RC LPF and HPF implemented with the same  $R$  and  $C$ . (b) Gain, group delay, and phase delay at 100 and 200 MHz.

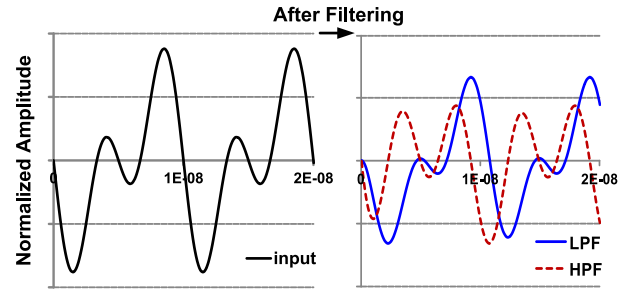


Fig. 5. Simulated waveforms with the LPF and HPF in Fig. 4.

where  $k_3$ ,  $k_2$ , and  $k_1$  are the arbitrary constants. Then, the phase delay  $\tau_p$  becomes

$$\tau_p(\omega) = -\frac{\varphi(\omega)}{\omega} = k_3\omega^2 + k_2\omega + k_1 \quad (7)$$

while the group delay is

$$\tau_g(\omega) = -\frac{d\varphi(\omega)}{d\omega} = 3k_3\omega^2 + 2k_2\omega + k_1. \quad (8)$$

With the coefficients of  $k_3 = -5 \times 10^{-25}/(12\pi^2)$ ,  $k_2 = 5 \times 10^{-17}/(2\pi)$ , and  $k_1 = 5 \times 10^{-9}$ , the phase delays at 100 and 200 MHz are made the same, whereas the same group delays are obtained with a slightly different set of coefficients of  $k_3 = -5 \times 10^{-25}/(36\pi^2)$ ,  $k_2 = 5 \times 10^{-17}/(4\pi)$ , and  $k_1 = 5 \times 10^{-9}$ . The waveforms at the output of this polynomial phase shifter are shown and compared to those at the input in Fig. 3. For the case of the same phase delay, the output waveform exactly matches with the input waveform despite the group delays differ by 5 ns, as shown in Fig. 3(a). On the other hand, the output waveform deviates from the input waveform even with the same group delay, despite the difference between the phase delays is less than 1 ns. In other words, the coefficient multiplication due to the presence of a differentiation in group delay calculation causes not only the loss of the constant term but also deformation of the original phase information. Considering the Taylor's theorem where all  $n$ -times differentiable functions can be approximated by an  $n$ th-order polynomial, it can be inferred that the failure of the group delay

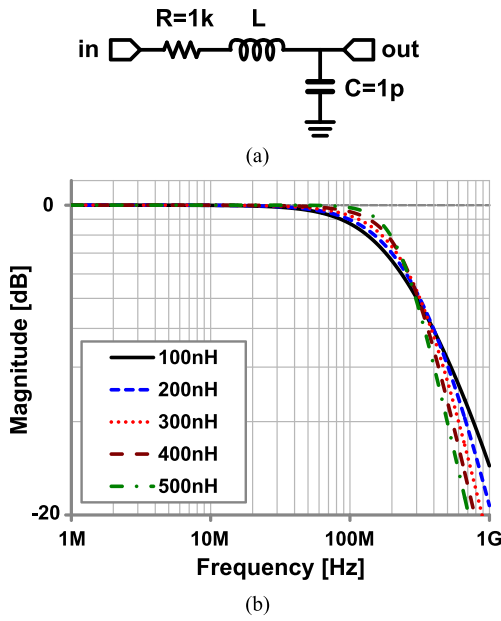


Fig. 6. (a)  $RLC$  circuit under testing. (b) Magnitude response of  $RLC$  circuit with varied inductance.

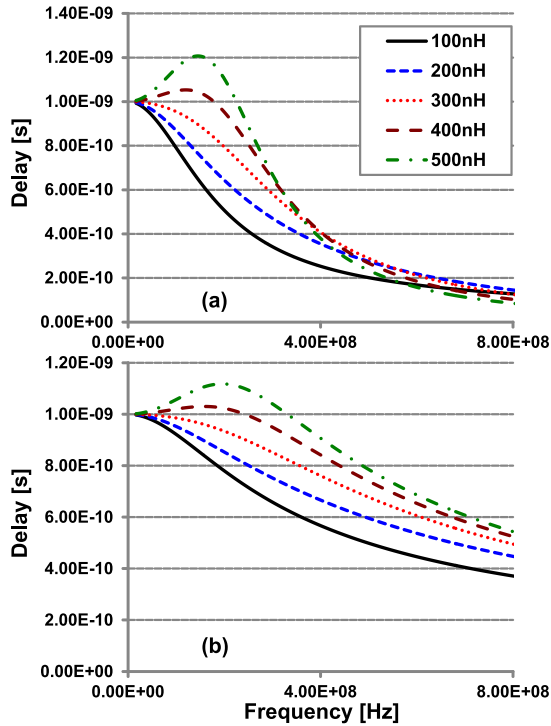


Fig. 7. Simulated (a) group delay and (b) phase delay using the  $RLC$  circuit with inductances of 100–500 nH.

analysis on this polynomial-based example may be extended to very general cases.

### III. APPLICATION ON RLC CIRCUITS

Because there is no such a linear system that exhibits a flat magnitude response and a varying phase responses simultaneously, the example case investigated in Section II may seem a bit unusual. In this section, even more general examples using  $RLC$  circuits are presented. First, let us consider an  $RC$  low-pass filter (LPF) and an  $RC$  high-pass filter (HPF) implemented with the same  $R$  and  $C$  values, as shown in Fig. 4(a). The transfer functions of these filters

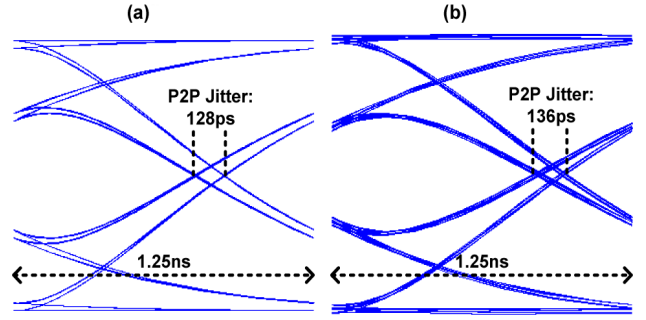


Fig. 8. Simulated eye diagrams and peak-to-peak jitter at the output of the  $RLC$  circuit with two inductance values. (a)  $L = 300$  nH,  $BW = 212$  MHz,  $PD\_var = 504$  ps, and  $GD\_var = 874$  ps. (b)  $L = 400$  nH,  $BW = 222$  MHz,  $PD\_var = 505$  ps, and  $GD\_var = 950$  ps.

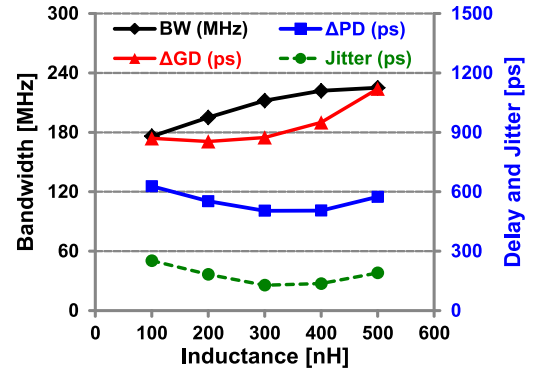


Fig. 9. Summary of the simulation results with the  $RLC$  circuit.  $\Delta GD$  and  $\Delta PD$  are the differences between the maximum and minimum values of the data plotted in Fig. 7(a) and (b), respectively.

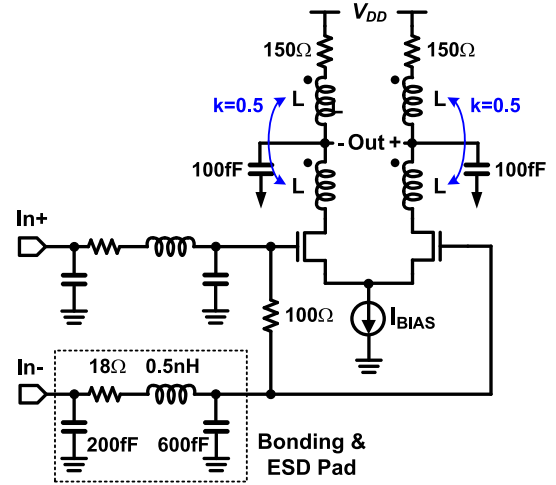


Fig. 10. Circuit diagram of a CML buffer with T-coil peaking preceded by a bonding wire and an electrostatic discharge (ESD) model.

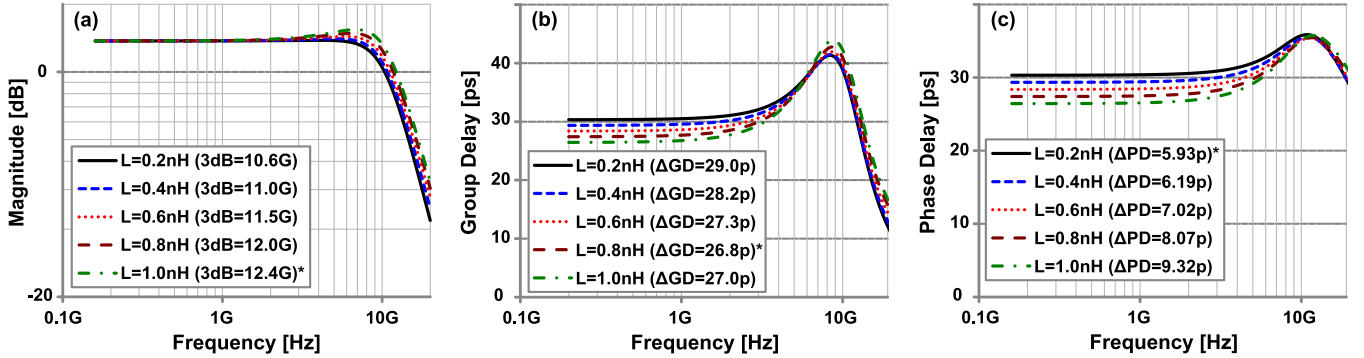
are expressed as

$$H_{LPF}(\omega) = \frac{1}{1 + j\omega RC} \quad \text{and} \quad H_{HPF}(\omega) = \frac{j\omega RC}{1 + j\omega RC}. \quad (9)$$

Then, the phase responses, phase delays, and group delays of the filters are

$$\phi_{LPF}(\omega) = -\arctan(\omega RC) \quad (10)$$

$$\phi_{HPF}(\omega) = \frac{\pi}{2} - \arctan(\omega RC) \quad (11)$$



\*The optimum design for the corresponding analysis. (Highest bandwidth, minimum group delay variation, and minimum phase delay variation)

Fig. 11. Simulated (a) magnitude response, (b) group delay, and (c) phase delay using T-coil circuit in Fig. 10 with inductances of 0.2–1 nH.

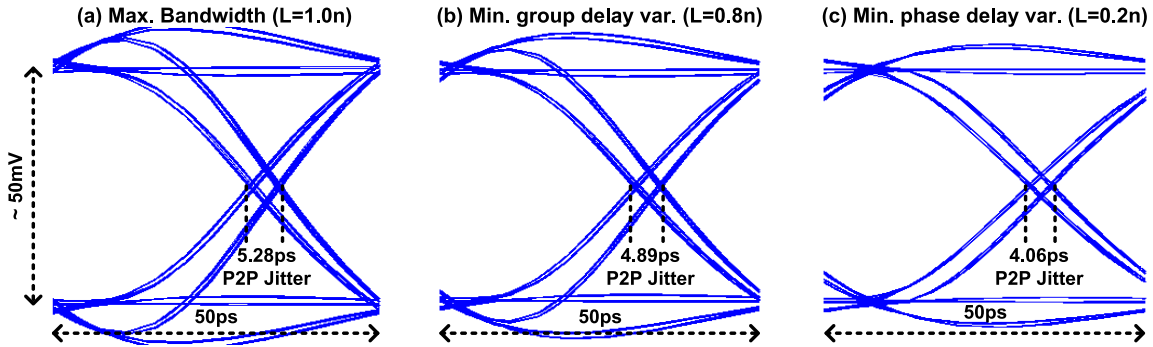


Fig. 12. Simulated eye diagrams of the T-coil circuit optimized for (a) highest bandwidth, (b) minimum group delay variation, and (c) minimum phase delay variation.

$$\tau_{p,\text{LPF}}(\omega) = \frac{\arctan(\omega RC)}{\omega} \quad (12)$$

$$\tau_{p,\text{HPF}}(\omega) = \frac{\arctan(\omega RC)}{\omega} - \frac{\pi}{2\omega} \quad (13)$$

$$\tau_{g,\text{LPF}}(\omega) = \tau_{g,\text{HPF}}(\omega) = \frac{RC}{1 + (\omega RC)^2}. \quad (14)$$

Note that the group delays of LPF and HPF are exactly the same. In the case of  $R = 1 \text{ k } \Omega$  and  $C = 1 \text{ pF}$ , gains, group delays, and phase delays that 100- and 200-MHz sinusoidal signals experience while passing through the filters are summarized in Fig. 4(b). The phase delay variation between the frequencies is much larger in the case of HPF; while the group delays are the same. Because the gain variation between the frequencies is comparable in the LPF and HPF cases, the group delay-based evaluation supposes that the degrees of signal distortions after the combined sinusoidal signals passed the filters are comparable. However, the simulation result in Fig. 5 shows that the signal after HPF experiences a bit more signal distortion. It is because, in fact, the HPF corresponds to the nonzero  $C$  case in Section II, and therefore the group delay analysis fails to give a correct expectation.

In the next example, a transient simulation with an  $RLC$  circuit and a pseudorandom binary sequence (PRBS) are presented, in order to mimic a practical bandwidth extension technique for a wideband data sequence. While a true random data sequence has a power spectral density (PSD) of

$$S(f) = T_B \left( \frac{\sin(\pi f T_B)}{\pi f T_B} \right)^2 \quad (15)$$

the PSD of an  $N$ -bit PRBS has only impulses at every  $1/(2^N - 1)T_B$ , where  $T_B$  is a bit period, because the PRBS is repeated

periodically [13]. Therefore, the frequency of interest ranges from  $1/\{(2^N - 1)T_B\}$  to  $(2^N - 1)/\{(2^N - 1)T_B\}$ , considering that there is no spectral component at  $1/T_B$ . Note that the delay variation across the signal components results in a data-dependent jitter (DDJ).

Fig. 6(a) shows an  $RLC$  circuit used in the test, which can be regarded as a series-inductive peaking circuit. Depending on the  $RLC$  values, the transfer function varies, and therefore most of the parameters including 3-dB bandwidth, phase delay, and group delay are also changed. In this simulation, the values of  $R$  and  $C$  are fixed in order to control the variables, whereas the inductance is swept from 100 to 500 nH. The simulated magnitude response of the  $RLC$  circuit is shown in Fig. 6(b). The 3-dB bandwidth ranges from 176 to 225 MHz. The simulated group delay and phase delay of the  $RLC$  are plotted in Fig. 7. Within the frequency range of interest for the 800-Mb/s PRBS-7, the group delay varies from 854 to 1120 ps as the inductance is increased from 100 to 500 nH, while that of the phase delay is within a narrow range of 504–628 ps. Specifically, the group delay variations are 874 and 950 ps, while exhibiting almost the same 3-dB bandwidth of 212 and 222 MHz, for the inductance of 300 and 400 nH, respectively. From the conventional view, where a large group delay variation results in a large DDJ [6], the  $RLC$  circuit with the inductance of 400 nH would exhibit a larger DDJ. However, from the simulated eye diagrams using the PRBS-7 shown in Fig. 8, there is no significant difference between DDJ of the two cases. The simulation result rather coincides well with the phase delay variations, which shows only a negligible difference between the two cases. The simulation results from the  $RLC$  example are summarized in Fig. 9. Definitely, the simulated deterministic jitter has a strong correlation with the variation of phase delay, whereas the variation of group delay exhibits a different tendency.

#### IV. APPLICATION TO A PRACTICAL DESIGN EXAMPLE

Fig. 10 shows a circuit diagram of a current-mode logic (CML) buffer with T-coil peaking preceded by a parasitic model including a bonding wire and an ESD parasitic. A 100- $\Omega$  resistor is placed for a differential termination, and a load capacitance of 100 fF is assumed at the output of the CML buffer. In this design example, we fixed all other parameters except for the inductance of T-coil and assumed that the two inductances in the T-coil are the same for simplicity. The simulated magnitude response, group delay, and phase delay of the circuit example with respect to the inductance are shown in Fig. 11. The simulation shows that the circuit exhibits the high 3-dB bandwidth, the minimum group delay variation, and the minimum phase delay variation when the inductance  $L$  equals 1, 0.8, and 0.2 nH, respectively. The simulated eye diagrams and deterministic jitters corresponding to the three optimized conditions are shown in Fig. 12. In order to minimize the nonlinear effect of the nMOS devices, a small swing of 20 mV is applied for the input 20-Gb/s PRBS-7 [5]. The simulation shows that the selection of the minimum phase delay variation leads to the best performance, and moreover the value of the jitter coincides with the phase delay variation a bit more.

Considering on the two circuit examples of RC filters and series peaking provided in the previous section and the practical design example provided in this section, it is highly suggested that the credibility of the group delay analysis that has been conventionally used in evaluating a wideband signal should be reconsidered. Alternately, the phase delay analysis, which gives a much more accurate evaluation, should be adopted.

#### V. CONCLUSION

This brief suggests that the effectiveness of the group delay analysis on evaluating a wideband circuit is questionable. From definition, the group delay basically represents the phase deviation between adjacent frequencies. Therefore, it has some inherent limitations in reflecting all the information required for evaluating a wideband circuit, even if it provides a partially correct estimate. Because of the involvement of differentiation, the group delay makes a constant term be disappeared and distorts the weight of each polynomial term. On the other hand, the phase delay analysis gives an exact evaluation

both theoretically and practically. Along with the theoretical analysis, this brief proves the advantages of the phase delay over the group delay by suggesting proper circuit examples.

#### REFERENCES

- [1] W. Bae, H. Ju, K. Park, S.-Y. Cho, and D.-K. Jeong, "A 7.6 mW, 414 fs RMS-jitter 10 GHz phase-locked loop for a 40 Gb/s serial link transmitter based on a two-stage ring oscillator in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2357–2367, Oct. 2016.
- [2] S. Galal and B. Razavi, "Broadband ESD protection circuits in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2334–2340, Dec. 2003.
- [3] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, Aug. 2004.
- [4] S. Shekhar, J. S. Walling, and D. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, Nov. 2006.
- [5] J. Kim, J.-K. Kim, B.-J. Lee, and D.-K. Jeong, "Design optimization of on-chip inductive peaking structures for 0.13- $\mu$ m CMOS 40-Gb/s transmitter circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 12, pp. 2544–2555, Dec. 2009.
- [6] J. Kim and J. F. Buckwalter, "Bandwidth enhancement with low group-delay variation for a 40-Gb/s transimpedance amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1964–1972, Aug. 2010.
- [7] D. Pi, B.-K. Chun, and P. Heydari, "A synthesis-based bandwidth enhancement technique for CMOS amplifiers: Theory and design," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 392–402, Feb. 2011.
- [8] S.-H. Chu *et al.*, "A 22 to 26.5 Gb/s optical receiver with all-digital clock and data recovery in a 65 nm CMOS process," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2603–2612, Nov. 2015.
- [9] I. Kwon, T. Kang, B. R. Wells, L. J. D'Aries, and M. D. Hammig, "A high-gain 1.75-GHz dual-inductor transimpedance amplifier with gate noise suppression for fast radiation detection," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 4, pp. 356–360, Apr. 2016.
- [10] Y. Kim, G.-S. Jeong, J.-E. Park, J. Park, G. Kim, and D.-K. Jeong, "20-Gb/s 5-V<sub>pp</sub> and 25-Gb/s 3.8-V<sub>pp</sub> area-efficient modulator drivers in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 11, pp. 1034–1038, Nov. 2016.
- [11] W. Bae, G.-S. Jeong, K. Park, and S.-Y. Cho, "A 0.36 pJ/bit, 0.025 mm<sup>2</sup>, 12.5 Gb/s forwarded-clock receiver with a stuck-free delay-locked loop and a half-bit delay line in 65-nm CMOS technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1393–1403, Sep. 2016.
- [12] A. B. Carlson, P. B. Crilly, and J. C. Rutledge, *Communication Systems*. New York, NY, USA: McGraw-Hill, 2002.
- [13] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York, NY, USA: McGraw-Hill, 2002.