

# Discrete-Time, Linear Periodically Time-Variant Phase-Locked Loop Model for Jitter Analysis

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**Abstract**—Timing jitter is one of the most significant phase-locked loop (PLL) characteristics, which directly affects the performance of the system in which the PLL is used. It is, therefore, important to develop the tools necessary to study and predict PLL jitter performance at design time. In this paper a discrete-time, linear, periodically time-variant integer- $N$  PLL model for jitter analysis is proposed, which accounts for the periodically time-varying effect of noise injected into the loop at various PLL components, such as VCO, charge pump, VCO buffer, VCO control node, and divider. The model also predicts the aliasing of jitter due to the downsampling and upsampling of the jitter signal around the PLL loop. Closed-form expressions are derived for the output jitter spectrum and match well with results of event-driven simulations of a third-order PLL.

**Index Terms**—Cyclostationary analysis, discrete time analysis, impulse sensitivity function, jitter, modeling, noise, phase jitter, phase locked loops (PLL), phase noise, timing jitter.

## I. INTRODUCTION

**T**IMING jitter is one of the most important performance metrics for the steady-state operation of a phase-locked loop (PLL) circuit. It contributes to synchronization problems and is a major source of bit error rate in wireless and wireline communication systems. It is, therefore, crucial to develop the analytical and modeling tools necessary to accurately study and predict the jitter performance of the PLL output clock.

Various approaches have been developed for the analysis of PLL jitter. Continuous- or discrete-time, linear PLL models are popular with designers, because they give insight into the PLL jitter optimization process. Other methods that have been developed are based on stochastic differential equations [1] or stochastic sensitivity analysis [2]. These approaches may be more general and mathematically elegant, but are often too complex for use in practical designs.

A conventional approach for studying PLL jitter is by assuming a continuous-time, linear, time-invariant model for the PLL circuit, e.g., [3]–[5]. This method relates the PLL jitter performance to basic parameters of the PLL components, such as VCO gain or loop filter characteristics, and thus gives powerful insight into various design trade-offs associated with jitter optimization [6]. There are, however, two important issues with the continuous-time, linear time-invariant model, which are discussed below.

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The issue with the continuous-time approach is that it fails to capture the frequency aliasing on the PLL output jitter spectrum, which can occur when the divide ratio  $N$  of the PLL is larger than unity. When the divide ratio is larger than unity, then the divide-by- $N$  circuit essentially acts as a downsampling block by outputting one out of every  $N$  transitions of the PLL output clock. When analyzing the PLL in discrete-time, this situation corresponds to downsampling and upsampling of the discrete-time jitter signal around the PLL loop. As a result of the downsampling/upsampling process, the jitter signal may get aliased. In order for such an effect to become apparent, it is necessary to consider a discrete-time model of the PLL. Even though discrete-time PLL models exist in the literature, they either only consider PLL circuits with a frequency multiplication factor  $N$  equal to one [7]–[10] or model the divide-by- $N$  circuit simply as a  $1/N$  phase divider [11]–[13]. As explained above, neither of these approaches captures the jitter aliasing effects in a general integer- $N$  PLL. In [14], the feedback divider is modeled as a moving-average filter, which also masks the jitter aliasing effect. In [15], the effect of frequency folding is considered when calculating the phase noise contribution of a divider in a PLL, but only in the case of white noise with a constant power spectral density.

The issue with the time-invariant approach is that it does not consider the effect of the periodically time-varying (PTV) nature of the PLL system on the output jitter. It is known that the mechanism, which converts the supply/substrate and device noise produced at PLL components like voltage-controlled oscillator (VCO), charge pump, VCO output buffer, and divider into noise injected into the PLL loop, is not time-invariant, but rather periodically time-varying. This PTV mechanism has been examined in the literature in the case of standalone circuits, such as general oscillators [16]–[18], ring oscillator VCOs [19]–[21] and mixers, samplers, and logic [17], [18]. In [16], a general approach is developed based on the concept of the Impulse Sensitivity Function (ISF), which quantifies the effect of the periodically time-varying nature of oscillators on phase noise. However, limited attempts have been made to develop a PLL model that deals with the PTV effect of the noise injected into the PLL loop. In [22], [23], cyclostationary approaches to PLL jitter analysis due to substrate noise coupling are presented. The investigation is mainly about substrate noise coupling through the VCO and limited theoretical analysis is presented. The analysis in [24], [25] also concentrates on the effect of periodicity on the VCO phase noise, and it does not address the effects on the charge pump current noise, VCO buffer phase noise or other noise sources. Furthermore, the analysis is based on the specific circuit topology for the VCO stages, which somewhat limits its scope. By generalizing the circuit-independent description of the periodically time-varying nature of VCOs introduced in [16] to other PLL components, a more general study of the effects on PLL jitter can be made.

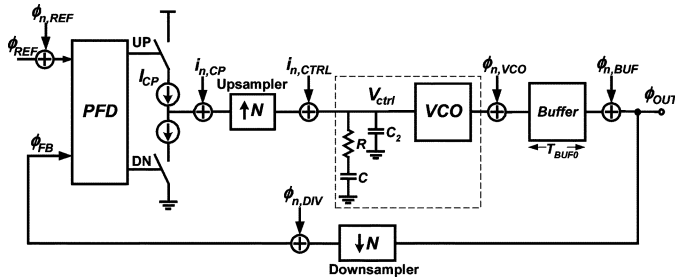


Fig. 1. Discrete-time model of third-order PLL with noise sources.

This can be especially useful, since the ISF of PTV circuits can be efficiently extracted using simulators like SpectreRF<sup>TM</sup>[18], [26], [27]. In [27], [28] an extensive analysis of the contributions of various PLL components on PLL output jitter is presented, which is accompanied by several examples of PLL block implementations in Verilog-A[29]. However, neither the analysis nor the Verilog-A implementations include phase information about the noise waveforms, which is necessary for a PTV analysis.

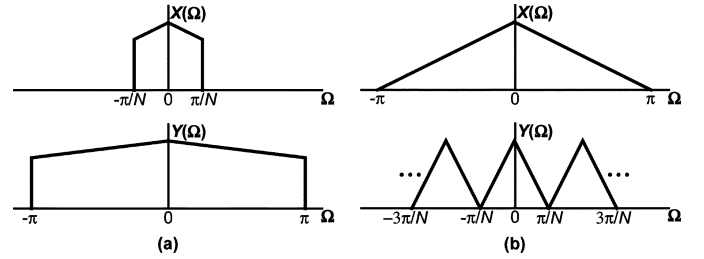
This paper presents an extension of PLL jitter theory, which accounts for the effects of aliasing in the PLL loop and also provides a general approach to incorporate the periodically time-varying nature of PLL blocks in the jitter analysis [30]. Section II develops the discrete-time, linear, periodically time-variant jitter model for the third-order PLL. This is accomplished in three steps: First, the discrete-time equations, which describe the individual PLL components, are derived in Section II-A. Then, the PTV mechanism, which converts supply or device noise to PLL loop-injected noise, is described for the VCO, charge pump, VCO output buffer, VCO control node, and divider, and the spectral characteristics of the resulting noise sources are derived in Section II-B. To complete the model, the transfer functions from the various noise sources to the output jitter are calculated for the discrete-time PLL model in Section II-B1. The theoretical results are verified using Verilog-A behavioral simulations of third-order PLL circuits in various noise scenarios in Section III.

## II. DISCRETE-TIME, PERIODICALLY TIME-VARIANT PLL MODEL

This section develops the discrete-time, linear, periodically time-variant model for a third-order PLL. Fig. 1 shows the discrete-time model of the third-order PLL used in the subsequent analysis along with the main PLL noise sources. The divide-by- $N$  component is modeled as a downsampling-by- $N$  block. The upsampling block introduces  $N - 1$  zeros between successive pulses of charge pump current. This block does not correspond to a physical circuit in the PLL. Instead it models the fact that the charge pump is activated only once every  $N$  PLL clock cycles, in order to adjust the VCO control voltage, while it remains off during the rest of the time. The combination of the downsampling and upsampling blocks keeps the sampling frequencies consistent around the PLL loop. The block diagram also shows the noise signals that are introduced at the various PLL components. Table I summarizes the main PLL parameters that are used in the following analysis.

### A. Discrete-Time Equations for PLL Components

This subsection derives the discrete-time transfer functions for the various PLL components in Fig. 1. It should be noted


 Fig. 2. Signal spectra for: a) downsampling-by- $N$  and b) upsampling-by- $N$  blocks.

that the Fourier transforms shown in the following are periodic functions with period equal to  $2\pi$ . The digital angular frequency  $\Omega$  is defined in the interval  $[-\pi, \pi]$  and relates to the analog frequency  $f$  through the equation  $\Omega = 2\pi f/F_s$ ,  $-F_s/2 < f \leq F_s/2$ , where  $F_s$  is the sampling frequency.

The output spectrum  $Y(\Omega)$  of the downsampling-by- $N$  block is related to its input spectrum  $X(\Omega)$  through the following equation [31]:

$$Y(\Omega) = \frac{1}{N} \cdot \sum_{k=0}^{N-1} X\left(\frac{\Omega - 2\pi k}{N}\right). \quad (1)$$

The output spectrum of the upsampling-by- $N$  block is related to its input spectrum as follows [31]:

$$Y(\Omega) = X(\Omega \cdot N). \quad (2)$$

Fig. 2 graphically depicts the relationship between input and output spectra for the downsampling and upsampling blocks.

The conversion gain of the combination of the phase-frequency detector (PFD) and the charge pump is given by [8]

$$K_p = \frac{I_{CP}}{f_{PLL}}. \quad (3)$$

The discrete-time transfer function of the combination of the loop filter and VCO is obtained through the impulse-invariant transformation technique [8], [12] and is equal to

$$H_{LF,VCO}(\Omega) = \frac{A \cdot e^{-j\Omega}}{(1 - e^{-j\Omega})^2} + \frac{B}{1 - e^{-j\Omega}} + \frac{E}{1 - e^{-(C+C_2/CC_2R)T} \cdot e^{-j\Omega}} \quad (4)$$

where the coefficients are given by the following equations:

$$A = \frac{K_V \cdot T}{C + C_2}, \quad (5)$$

$$B = \frac{K_V \cdot C^2 R}{(C + C_2)^2} + \frac{K_V \cdot T_{BUF0}}{C + C_2} \quad (6)$$

$$E = -\frac{K_V \cdot C^2 R}{(C + C_2)^2} \cdot e^{-(C+C_2/CC_2R)T_{BUF0}} \quad (7)$$

In the above expressions,  $K_V$  is the frequency gain of the VCO in Hz/V,  $T$  is the period of the PLL output clock and  $T_{BUF0}$  is the nominal buffer delay. The parameters  $C$ ,  $C_2$ ,  $R$  are as shown in Fig. 1. The details of the derivation are shown in Appendix A.

Finally, the discrete-time transfer function of the output buffer is all-pass and given by

$$H_{BUF}(\Omega) = 1. \quad (8)$$

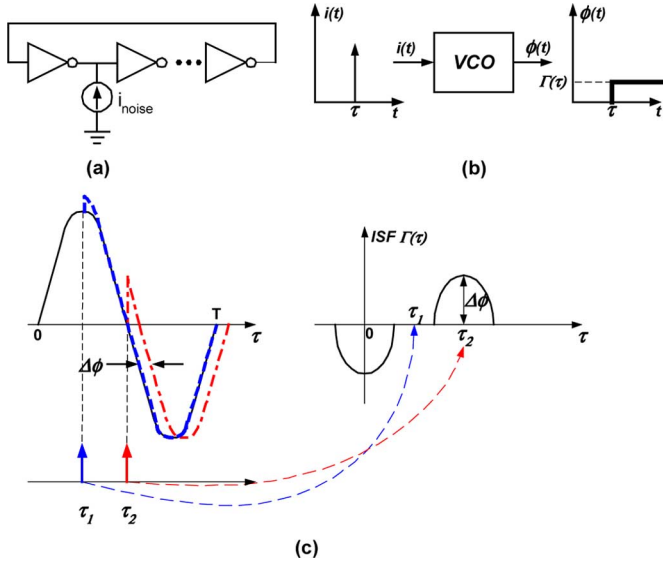


Fig. 3. ISF mechanism for VCO device noise. (a) Current impulse injected into a VCO node. (b) Phase step response of the VCO to the injected current impulse. (c) Current impulses injected at different time instants produce different phase step magnitudes.

The delay  $T_{\text{BUF0}}$  of the buffer is taken into account in the derivation of  $\tilde{H}_{\text{LF,VCO}}(\Omega)$  above.

### B. Periodically Time-Varying Behavior of PLL Blocks

The periodically time-varying mapping of supply/ground and device noise from various PLL components into noise injected into the PLL loop can be described by generalizing the concept of the ‘‘Impulse Sensitivity Function’’ (ISF) [18], [30]. The concept of the ISF was introduced by Hajimiri and Lee [16] to describe the effect of the periodically time-varying nature of VCOs on phase noise. The following subsections describe how the noise at the VCO, charge pump, VCO buffer, VCO control node, and divider can be modeled using the generalized ISF concept:

1) *VCO*: Fig. 3 explains the ISF concept in the case of device noise injected into a standalone VCO. Assuming that the injected noise is a current impulse, it will produce a step response in the VCO phase, because the momentary phase disturbance produced by the current impulse circulates around the VCO stages ad infinitum. The magnitude of this step response is dependent on the time instant within a VCO oscillation period, at which the current impulse is applied. A similar response is produced by a voltage impulse on the VCO supply.

The phase impulse response of a standalone VCO to either supply or device noise is given by the following expression:

$$h_{\phi_n, \text{VCO}}(t, \tau) = \Gamma_{p, \text{VCO}}(\tau) \cdot u(t - \tau) \quad (9)$$

where  $\tau$  is the time instant at which the noise impulse is applied and  $u(t)$  is the step function. For low noise levels  $\Gamma_{p, \text{VCO}}(\tau)$  is approximately a periodic function with period equal to that of the VCO oscillation, and whose value at  $\tau$  is the magnitude of the phase step produced by the noise impulse. The function  $\Gamma_{p, \text{VCO}}(\tau)$  is the ISF of the VCO and can be written as

$$\Gamma_{p, \text{VCO}}(\tau) = \sum_{n=-\infty}^{\infty} \Gamma_{\text{VCO}}(\tau - nT) \quad (10)$$

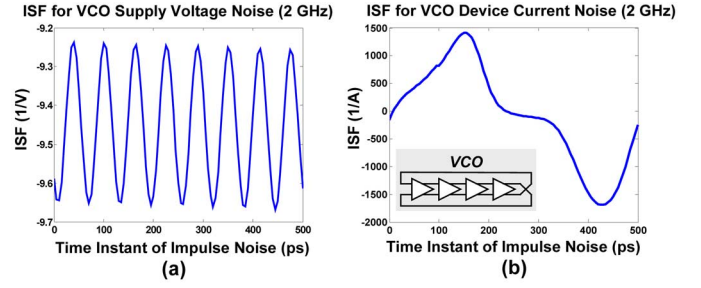


Fig. 4. VCO impulse sensitivity functions. (a) Supply noise. (b) Device noise in one VCO node. The VCO is comprised of four differential stages.

where  $\Gamma_{\text{VCO}}(\tau)$  denotes one period of the ISF, see Fig. 3(c). The phase response of the VCO to an arbitrary noise disturbance can then be approximated by the following superposition integral for low noise taking into account the periodicity of the ISF

$$\begin{aligned} \phi_{n, \text{VCO}}[k] &\equiv \phi_{n, \text{VCO}}(kT) = \int_{-\infty}^{kT} \Gamma_{p, \text{VCO}}(\tau) \cdot i(\tau) d\tau \\ &= \phi_{n, \text{VCO}}[k - 1] \\ &\quad + \int_0^T \Gamma_{\text{VCO}}(\tau) \cdot i(\tau + (k - 1)T) d\tau \quad (11) \end{aligned}$$

where  $i(\tau)$  denotes the supply or device noise waveform. Fig. 4 shows one period of the ISFs that correspond to supply and device noise of a VCO designed in  $0.13 \mu\text{m}$  CMOS. The ISFs were extracted using transistor-level simulations for a VCO comprised of 4 differential stages and operating at 2 GHz by measuring the magnitudes of the phase steps when applying impulses on the VCO supply or internal nodes at different instances during the VCO period. As mentioned above, the ISFs can also be extracted efficiently in some simulators, such as SpectreRF [18], [26].

Using the above equations, it is possible to derive the spectrum of the noise injected into the PLL loop for some important types of supply or device noise, such as impulse, step, or sinusoidal:

- a) *Impulse function*: Let the supply or device noise  $i(\tau)$  be a deterministic impulse function given by  $i(\tau) = A \cdot \delta(\tau - \tau'_0)$  where  $\tau'_0 = (k_0 - 1)T + \tau_0$  with  $0 \leq \tau_0 < T$  and  $k_0$  integer. Then, from (11), the VCO output phase is  $\phi_{n, \text{VCO}}[k] = A \cdot \Gamma_{\text{VCO}}(\tau_0) \cdot u[k - k_0]$  where  $u[\cdot]$  is the step function. Hence, the discrete-time Fourier transform (DTFT) of the injected phase noise into the PLL loop at the output of the VCO is

$$\Phi_{n, \text{VCO}}^{\text{Imp}}(\Omega) = A \cdot \Gamma_{\text{VCO}}(\tau_0) \cdot e^{-j\Omega k_0} \cdot U(\Omega) \quad (12)$$

where  $U(\Omega) = (1/1 - e^{-j\Omega}) + \pi \cdot \delta(\Omega)$  the DTFT of  $u[k]$ .

- b) *Step function*: Let the supply or device noise  $i(\tau)$  be a step function given by  $i(\tau) = A \cdot u(\tau - \tau'_0)$  where  $\tau'_0 = (k_0 - 1)T + \tau_0$  with  $0 \leq \tau_0 < T$  and  $k_0$  integer. It can be seen from (11) that the first time difference of the VCO phase step response can be written as

$$\begin{aligned} \phi'_{n, \text{VCO}}[k] &\equiv \phi_{n, \text{VCO}}[k] - \phi_{n, \text{VCO}}[k - 1] \\ &= A \cdot Q(\tau_0, T) \cdot u[k - k_0] \\ &\quad + A \cdot Q(0, \tau_0) \cdot u[k - k_0 - 1] \quad (13) \end{aligned}$$

where  $Q(\tau_0, T) \equiv \int_{\tau_0}^T \Gamma_{\text{VCO}}(\tau) d\tau$  and  $Q(0, \tau_0) \equiv \int_0^{\tau_0} \Gamma_{\text{VCO}}(\tau) d\tau$ . Therefore, the DTFT of the VCO phase response to the step input is

$$\Phi_{n,\text{VCO}}^{\text{Step}}(\Omega) = \left[ A \cdot Q(\tau_0, T) \cdot \frac{e^{-j\Omega k_0}}{1 - e^{-j\Omega}} + A \cdot Q(0, \tau_0) \cdot \frac{e^{-j\Omega(k_0+1)}}{1 - e^{-j\Omega}} \right] \cdot U(\Omega) \quad (14)$$

where  $U(\Omega)$  the DTFT of  $u[k]$ .

It should be noted that this analysis can also be used to model finite-duration pulse noise functions of the form  $i(\tau) = A \cdot u(\tau - \tau'_1) - A \cdot u(\tau - \tau'_2)$  or piecewise constant noise functions. Due to the linearity of the DTFT, the resulting noise spectrum will be the sum of the individual spectra.

- c) *Sinusoidal function*: Let  $i(\tau)$  be a deterministic sinusoidal function given by  $i(\tau) = A_1 \cdot \cos(\omega'_1 \tau + \theta_1)$ . The DTFT of the VCO noise injected into the PLL loop can be shown to be (see Appendix B)

$$\Phi_{n,\text{VCO}}^{\text{Sin}}(\Omega) = \frac{\pi}{1 - e^{-j\Omega}} \cdot \left\{ \begin{aligned} &Q_1(\omega'_1, \theta_1) \cdot \delta(\Omega - \omega_1 T) \\ &+ Q_2(\omega'_1, \theta_1) \cdot \delta(\Omega + \omega_1 T) \end{aligned} \right\} \quad (15)$$

where

$$\omega_1 T = \text{mod}(\omega'_1 T, 2\pi) \quad (16)$$

$$Q_1(\omega'_1, \theta_1) = \int_0^T \Gamma_{\text{VCO}}(\tau) \cdot [Q_c(\tau, \omega'_1, \theta_1) - jQ_s(\tau, \omega'_1, \theta_1)] d\tau \quad (17a)$$

$$Q_2(\omega'_1, \theta_1) = \int_0^T \Gamma_{\text{VCO}}(\tau) \cdot [Q_c(\tau, \omega'_1, \theta_1) + jQ_s(\tau, \omega'_1, \theta_1)] d\tau \quad (17b)$$

$$Q_c(\tau, \omega'_1, \theta_1) = A_1 \cdot \cos[\omega'_1 \cdot \tau - \omega'_1 \cdot T + \theta_1] \quad (18a)$$

$$Q_s(\tau, \omega'_1, \theta_1) = A_1 \cdot \sin[\omega'_1 \cdot \tau - \omega'_1 \cdot T + \theta_1]. \quad (18b)$$

From (15)–(18) it can be seen that the phase relationship between the sinusoidal input  $i(\tau)$  and the impulse sensitivity function of the VCO may affect the magnitude of the factors  $Q_1$  and  $Q_2$ , which in turn may affect the magnitude of the periodic jitter at the output. The effect of the finite duration of the sinusoidal noise in simulations is considered in Appendix B.

2) *Charge Pump*: A similar approach using the generalized ISF concept can be used to model the periodically time-varying effect of the charge pump supply or device noise on the output current of the charge pump. Fig. 5 gives a graphical interpretation of the charge pump ISF concept in the case of supply voltage injected into a stand-alone charge pump. The noise current response can be approximated by an impulse function, whose magnitude is determined by the time integral of the current response. This is in contrast to the VCO case, where the phase impulse response was approximated by a step function. Therefore, in contrast to the VCO case, the charge pump noise accumulates over a single reference clock period. Fig. 5(c) shows that the noise current response is approximately constant during the ON period of the charge pump and is approximately zero otherwise.

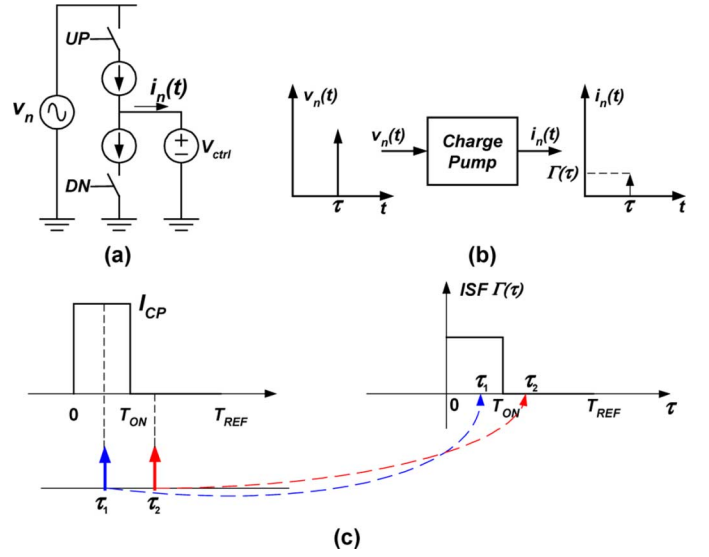


Fig. 5. ISF mechanism for charge pump current noise. (a) Voltage impulse injected into charge pump supply. (b) Current impulse response of the charge pump due to the injected supply voltage impulse. (c) Supply voltage impulses injected at different time instants produce different noise current magnitudes. When the charge pump is ON, the noise current impulses are constant and when the charge pump is OFF, the current impulses are zero.

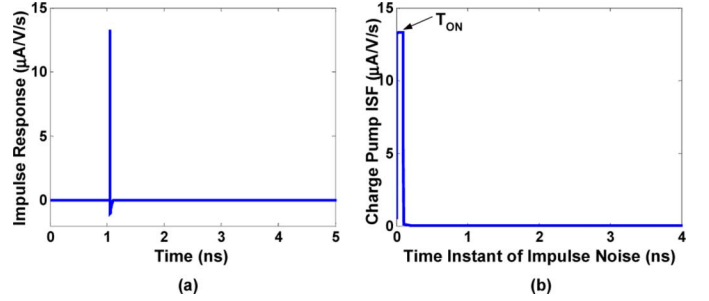


Fig. 6. (a) Normalized charge pump current impulse response. (b) Charge pump Impulse Sensitivity Function due to supply voltage noise.

Fig. 6(a) shows transistor-level simulation results of the current response of a standalone charge pump to an impulse on the supply voltage. It can be seen that the current response can be approximated by an impulse function. The charge pump ISF can be obtained by measuring the magnitude of the output current impulses in response to voltage impulses on the charge pump supply at different times during the reference clock period. Fig. 6(b) shows one period of the extracted charge pump ISF due to supply voltage noise. In steady-state operation, the charge pump generates current every reference clock period for approximately 100 ps. The reference clock period is 4 ns. The ISF in Fig. 6(b) is nonzero and approximately constant during the ON time of the charge pump, while it is approximately zero for the rest of the reference clock period, as expected intuitively. The charge pump ISF due to device noise has similar shape.

From the preceding discussion, the ISF-based model for the charge pump is as follows. For low noise levels, the charge pump ISF is approximately a periodic function with period equal to the reference clock period  $T_{\text{REF}}$ , so it can be written as

$$\Gamma_{p,\text{CP}}(\tau) = \sum_{n=-\infty}^{\infty} \Gamma_{\text{CP}}(\tau - nT_{\text{REF}}) \quad (19)$$

where  $\Gamma_{\text{CP}}$  is one period of the ISF as shown in Fig. 6(b). The additive noise to the current at the output of the charge pump

accumulates approximately over a single period. Therefore, the charge pump output noise current can be approximated by the following superposition integral for low noise and taking into account the periodicity of the ISF:

$$\begin{aligned} i_{n,CP}[k] &\equiv i_{n,CP}(kT_{REF}) = \int_{(k-1)T_{REF}}^{kT_{REF}} \Gamma_{p,CP}(\tau) \cdot i(\tau) d\tau \\ &= \int_0^{T_{REF}} \Gamma_{CP}(\tau) \cdot i(\tau + (k-1)T_{REF}) d\tau \quad (20) \end{aligned}$$

Using (20), we can determine the current noise spectrum at the charge pump when the supply or device noise is impulse, step, white, or sinusoidal:

- a) *Impulse function*: Let the supply or device noise signal  $i(\tau)$  be a deterministic impulse function given by  $i(\tau) = A \cdot \delta(\tau - \tau'_0)$  where  $\tau'_0 = (k_0 - 1)T_{REF} + \tau_0$  with  $0 \leq \tau_0 < T_{REF}$  and  $k_0$  integer. Then from (20), the noise current at the output of the charge pump is

$$i_{n,CP}[k] = A \cdot \Gamma_{CP}(\tau_0) \cdot \delta[k - k_0] \quad (21)$$

Hence, the Fourier transform of the injected noise to the PLL loop at the output of the charge pump is

$$I_{n,CP}^{Imp}(\Omega) = A \cdot \Gamma_{CP}(\tau_0) \cdot e^{-j\Omega k_0} \quad (22)$$

- b) *Step function*: Let the noise signal  $i(\tau)$  be a step function given by  $i(\tau) = A \cdot u(\tau - \tau'_0)$  where  $\tau'_0 = (k_0 - 1)T_{REF} + \tau_0$  with  $0 \leq \tau_0 < T_{REF}$  and  $k_0$  integer. It can be seen from (20) that the current step response can be written as

$$\begin{aligned} i_{n,CP}[k] &= A \cdot Q(\tau_0, T_{REF}) \cdot u[k - k_0] \\ &\quad + A \cdot Q(0, \tau_0) \cdot u[k - k_0 - 1] \quad (23) \end{aligned}$$

where  $Q(\tau_0, T_{REF}) \equiv \int_{\tau_0}^{T_{REF}} \Gamma_{CP}(\tau) d\tau$  and  $Q(0, \tau_0) \equiv \int_0^{\tau_0} \Gamma_{CP}(\tau) d\tau$ . Therefore, the DTFT of the current response to the step input is

$$\begin{aligned} I_{n,CP}^{Step}(\Omega) &= \left( A \cdot Q(\tau_0, T_{REF}) \cdot e^{-j\Omega k_0} \right. \\ &\quad \left. + A \cdot Q(0, \tau_0) \cdot e^{-j\Omega(k_0+1)} \right) \cdot U(\Omega) \quad (24) \end{aligned}$$

where  $U(\Omega)$  the DTFT of the step function  $u[k]$ .

- c) *White noise*: Let the noise signal  $i(\tau)$  be random white noise with power spectral density  $N_0$ . Then from (20) it can be seen that the samples  $i_{n,CP}[k]$  form an independent, identically distributed (i.i.d.) sequence. The variance of each sample is

$$\sigma_X^2 \equiv \text{Var}[i_{n,CP}[k]] = N_0 \cdot \int_0^{T_{REF}} \Gamma_{CP}^2(\tau) d\tau \quad (25)$$

The power spectral density (PSD) of the injected noise to the current at the output of the charge pump is therefore [33]

$$I_{n,CP}^{White}(\Omega) = \frac{\sigma_X^2}{2\pi} = \frac{N_0}{2\pi} \cdot \int_0^{T_{REF}} \Gamma_{CP}^2(\tau) d\tau, |\Omega| \leq \pi \quad (26)$$

- d) *Sinusoidal function*: Let the noise signal be a deterministic sinusoidal function given by  $i(\tau) = A_1 \cdot \cos(\omega'_1 \tau + \theta_1)$ .

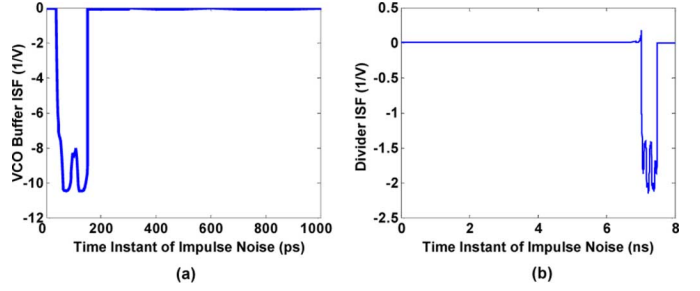


Fig. 7. Impulse Sensitivity Functions due to supply voltage noise. (a) VCO buffer. (b) Divider. The divide ratio is 8.

The DTFT of the charge pump current noise injected into the PLL loop can be shown to be (see Appendix B)

$$\begin{aligned} I_{n,CP}^{Sin}(\Omega) &= \pi \cdot \left\{ Q_1(\omega'_1, \theta_1) \cdot \delta(\Omega - \omega_1 T_{REF}) \right. \\ &\quad \left. + Q_2(\omega'_1, \theta_1) \cdot \delta(\Omega + \omega_1 T_{REF}) \right\} \quad (27) \end{aligned}$$

where

$$\omega_1 T_{REF} = \text{mod}(\omega'_1 T_{REF}, 2\pi) \quad (28)$$

$$\begin{aligned} Q_1(\omega'_1, \theta_1) &= \int_0^{T_{REF}} \Gamma_{CP}(\tau) \\ &\quad \cdot [Q_c(\tau, \omega'_1, \theta_1) - jQ_s(\tau, \omega'_1, \theta_1)] d\tau \quad (29a) \end{aligned}$$

$$\begin{aligned} Q_2(\omega'_1, \theta_1) &= \int_0^{T_{REF}} \Gamma_{CP}(\tau) \\ &\quad \cdot [Q_c(\tau, \omega'_1, \theta_1) + jQ_s(\tau, \omega'_1, \theta_1)] d\tau \quad (29b) \end{aligned}$$

$$Q_c(\tau, \omega'_1, \theta_1) = A_1 \cdot \cos[\omega'_1 \cdot \tau - \omega'_1 \cdot T_{REF} + \theta_1] \quad (30a)$$

$$Q_s(\tau, \omega'_1, \theta_1) = A_1 \cdot \sin[\omega'_1 \cdot \tau - \omega'_1 \cdot T_{REF} + \theta_1] \quad (30b)$$

From (27)–(30) it can be seen that the phase relationship between the sinusoidal input  $i(\tau)$  and the impulse sensitivity function of the charge pump may affect the magnitude of the factors  $Q_1$  and  $Q_2$ , which in turn may affect the magnitude of the periodic jitter at the output.

- 3) *VCO Buffer*: The ISF concept can be used to model the periodically time-varying effect of the VCO buffer supply or device noise on the output phase of the VCO buffer. Without loss of generality we assume that the VCO buffer delay is less than the VCO period, which is the case in most practical designs. Fig. 7(a) shows one period of the extracted buffer ISF due to supply voltage noise. The buffer contains two stages and has nonzero ISF only during the time that the signal propagates through the buffer. The buffer ISF due to device noise has similar shape.

For low noise levels, the VCO buffer ISF can be approximated by a periodic function with period equal to the VCO period  $T$  as follows:

$$\Gamma_{p,BUF}(\tau) = \sum_{n=-\infty}^{\infty} \Gamma_{BUF}(\tau - nT) \quad (31)$$

where  $\Gamma_{BUF}(\cdot)$  is one ISF period, see Fig. 7(a). As in the charge pump case, the noise accumulates only during a single period  $T$ , and therefore the jitter at the buffer output can be written as

$$\begin{aligned} \phi_{n,BUF}[k] &\equiv \phi_{n,BUF}(kT) = \int_{(k-1)T}^{kT} \Gamma_{p,BUF}(\tau) \cdot i(\tau) d\tau \\ &= \int_0^T \Gamma_{BUF}(\tau) \cdot i(\tau + (k-1)T) d\tau \quad (32) \end{aligned}$$

Following a parallel analysis as in the charge pump case, the spectrum of the phase noise injected into the PLL loop at the buffer output can be found for the following noise types [32]:

- a) *Impulse function*: Let the device or supply noise signal  $i(\tau)$  be a deterministic impulse function given by  $i(\tau) = A \cdot \delta(\tau - \tau'_0)$  where  $\tau'_0 = (k_0 - 1)T + \tau_0$  with  $0 \leq \tau_0 < T$  and  $k_0$  integer. The DTFT of the injected noise to the PLL loop at the output of the buffer is

$$\Phi_{n,\text{BUF}}^{\text{Imp}}(\Omega) = A \cdot \Gamma_{\text{BUF}}(\tau_0) \cdot e^{-j\Omega k_0}. \quad (33)$$

- b) *Step function*: Let the noise signal  $i(\tau)$  be a step function given by  $i(\tau) = A \cdot u(\tau - \tau'_0)$  where  $\tau'_0 = (k_0 - 1)T + \tau_0$  with  $0 \leq \tau_0 < T$  and  $k_0$  integer. The DTFT of the phase response to the step input is

$$\begin{aligned} \Phi_{n,\text{BUF}}^{\text{Step}}(\Omega) &= \left( A \cdot Q(\tau_0, T) \cdot e^{-j\Omega k_0} + A \cdot Q(0, \tau_0) \cdot e^{-j\Omega(k_0+1)} \right) \\ &\quad \cdot U(\Omega) \end{aligned} \quad (34)$$

where  $Q(\tau_0, T) \equiv \int_{\tau_0}^T \Gamma_{\text{BUF}}(\tau) d\tau$ ,  $Q(0, \tau_0) \equiv \int_0^{\tau_0} \Gamma_{\text{BUF}}(\tau) d\tau$  and  $U(\Omega)$  the DTFT of  $u[k]$ .

- c) *White noise*: Let the noise signal  $i(\tau)$  be random white noise with power spectral density  $N_0$ . Then the power spectral density of the injected noise at the output of the buffer is

$$\Phi_{n,\text{BUF}}^{\text{White}}(\Omega) = \frac{N_0}{2\pi} \cdot \int_0^T \Gamma_{\text{BUF}}^2(\tau) d\tau. \quad (35)$$

- d) *Sinusoidal function*: Let the noise signal be a deterministic sinusoidal function given by  $i(\tau) = A_1 \cdot \cos(\omega'_1 \tau + \theta_1)$ . The DTFT of the buffer phase noise injected into the PLL loop can be shown to be

$$\begin{aligned} \Phi_{n,\text{BUF}}^{\text{Sin}}(\Omega) &= \pi \cdot \left\{ Q_1(\omega'_1, \theta_1) \cdot \delta(\Omega - \omega_1 T) \right. \\ &\quad \left. + Q_2(\omega'_1, \theta_1) \cdot \delta(\Omega + \omega_1 T) \right\} \end{aligned} \quad (36)$$

where  $\omega_1 T$  satisfies (16) and

$$\begin{aligned} Q_1(\omega'_1, \theta_1) &= \int_0^T \Gamma_{\text{BUF}}(\tau) \\ &\quad \cdot [Q_c(\tau, \omega'_1, \theta_1) - jQ_s(\tau, \omega'_1, \theta_1)] d\tau \end{aligned} \quad (37a)$$

$$\begin{aligned} Q_2(\omega'_1, \theta_1) &= \int_0^T \Gamma_{\text{BUF}}(\tau) \\ &\quad \cdot [Q_c(\tau, \omega'_1, \theta_1) + jQ_s(\tau, \omega'_1, \theta_1)] d\tau \end{aligned} \quad (37b)$$

$$Q_c(\tau, \omega'_1, \theta_1) = A_1 \cdot \cos[\omega'_1 \cdot \tau - \omega'_1 \cdot T + \theta_1] \quad (38a)$$

$$Q_s(\tau, \omega'_1, \theta_1) = A_1 \cdot \sin[\omega'_1 \cdot \tau - \omega'_1 \cdot T + \theta_1]. \quad (38b)$$

The same considerations discussed in Appendix B regarding the finite duration of the sinusoidal noise in simulations also hold here.

- 4) *VCO Control Node*: It is assumed that the coupling noise on the VCO control node is due to current noise injection, as shown in Fig. 1. The effect of this current noise is the same as that of the charge pump current noise, if the charge pump

ISF is equal to unity. Thus, the DTFT of the VCO control node current noise injected into the PLL loop is given by the same analysis and equations as in the charge pump case, where it is assumed that the ISF is constant and equal to  $1s^{-1}$ . It should be noted that unlike charge pump current noise, the VCO control node current noise is not upsampled. Hence, the noise transfer function is different, as shown in Section II-B1.

- 5) *Divider*: The extracted divider ISF due to supply noise is shown in Fig. 7(b). The divider is implemented as a ripple counter and the divide ratio is 8. As in the buffer case, the divider accumulates noise only during one reference clock period  $T_{\text{REF}}$ . The noise calculations can be derived from the buffer case by substituting  $\Gamma_{\text{BUF}}(\tau)$  with  $\Gamma_{\text{DIV}}(\tau)$  and  $T$  with  $T_{\text{REF}}$ .

### C. Closed Loop Noise Transfer Functions

In order to complete the PLL jitter model, it is necessary to calculate the closed-loop transfer functions from the reference clock, charge pump, VCO, and the other noise sources to the PLL output. The corresponding calculations are presented in Appendix C.

In the case when the noise source is the reference clock jitter, the spectrum of the PLL output jitter is given by the following expression (Appendix C):

$$Y_{\text{REF}}(\Omega) = \frac{H(\Omega)}{1 + \frac{1}{N} \sum_{k=0}^{N-1} H\left(\Omega - \frac{2\pi k}{N}\right)} \cdot \Phi_{n,\text{REF}}(N \cdot \Omega) \quad (39)$$

where

$$H(\Omega) = K_p \cdot H_{\text{LF,VCO}}(\Omega) \cdot H_{\text{BUF}}(\Omega) \quad (40)$$

is the forward gain of the PLL with  $K_p$ ,  $H_{\text{LF,VCO}}(\Omega)$ ,  $H_{\text{BUF}}(\Omega)$  as defined in Section II-A. The quantity  $\Phi_{n,\text{REF}}(\Omega)$  is the reference clock jitter spectrum. Equation (39) indicates that spectral images will be present at the output jitter spectrum due to upsampling of the input noise, as shown by the term  $\Phi_{n,\text{REF}}(N \cdot \Omega)$ .

The transfer function from the charge pump current noise to the output jitter is given by the following expression:

$$Y_{\text{CP}}(\Omega) = \frac{\frac{1}{f_{\text{PLL}}} \cdot \frac{H(\Omega)}{K_p}}{1 + \frac{1}{N} \sum_{k=0}^{N-1} H\left(\Omega - \frac{2\pi k}{N}\right)} \cdot I_{n,\text{CP}}(N \cdot \Omega) \quad (41)$$

where  $H(\Omega)$  is given by (40).

In the case of VCO noise, the output jitter is given by the following expression:

$$\begin{aligned} Y_{\text{VCO}}(\Omega) &= \Phi_{n,\text{VCO}}(\Omega) \cdot H_{\text{BUF}}(\Omega) \\ &\quad - \frac{1}{N} \frac{\sum_{k=0}^{N-1} \Phi_{n,\text{VCO}}\left(\Omega - \frac{2\pi k}{N}\right) \cdot H_{\text{BUF}}\left(\Omega - \frac{2\pi k}{N}\right)}{1 + \frac{1}{N} \sum_{k=0}^{N-1} H\left(\Omega - \frac{2\pi k}{N}\right)} \\ &\quad \times H(\Omega) \end{aligned} \quad (42)$$

where  $H(\Omega)$  as defined above and  $\Phi_{n,\text{VCO}}(\Omega)$  the VCO noise spectrum. In this case the jitter aliasing is apparent due to the  $\sum_{k=0}^{N-1} \Phi_{n,\text{VCO}}(\Omega - (2\pi k/N))$  term.

The output jitter due to VCO buffer noise is given by

$$\begin{aligned} Y_{\text{BUF}}(\Omega) &= \Phi_{n,\text{BUF}}(\Omega) \\ &\quad - \frac{1}{N} \frac{\sum_{k=0}^{N-1} \Phi_{n,\text{BUF}}\left(\Omega - \frac{2\pi k}{N}\right)}{1 + \frac{1}{N} \sum_{k=0}^{N-1} H\left(\Omega - \frac{2\pi k}{N}\right)} \times H(\Omega). \end{aligned} \quad (43)$$

TABLE I  
PLL PARAMETER VALUES

Parameter	Symbol	Value		Units
Reference clock frequency	$f_{REF}$	200		MHz
VCO gain	$K_V$	1.2		GHz/V
Charge pump current	$I_{CP}$	100		$\mu$ A
Loop filter resistance	$R$	2		K $\Omega$
Loop filter series capacitance	$C$	150		pF
Loop filter parallel capacitance	$C_2$	2		pF
Nominal buffer delay	$T_{BUF0}$	200		ps
Divide ratio	$N$	4	5	-
PLL frequency	$f_{PLL}$	0.8	1	GHz
Closed-loop bandwidth	$f_{3dB}$	12.5	9.7	MHz
Phase margin	$PM$	74	75	deg
Damping factor	$\zeta$	2.1	1.9	-
Peaking	$H_{max}$	0.4	0.5	dB

The output jitter due to the current noise injected into the VCO control node is given by

$$Y_{CTRL}(\Omega) = I_{n,CTRL}(\Omega) \cdot \frac{H(\Omega)}{K_p \cdot f_{PLL}} - \frac{1}{N} \frac{\sum_{k=0}^{N-1} I_{n,CTRL}(\Omega - \frac{2\pi k}{N}) \cdot H(\Omega - \frac{2\pi k}{N})}{1 + \frac{1}{N} \sum_{k=0}^{N-1} H(\Omega - \frac{2\pi k}{N})} \times \frac{H(\Omega)}{K_p \cdot f_{PLL}}. \quad (44)$$

Finally, the PLL output jitter due to the divider jitter is calculated in the same way as in the case of the reference clock jitter and is given by

$$Y_{DIV}(\Omega) = \frac{-H(\Omega)}{1 + \frac{1}{N} \sum_{k=0}^{N-1} H(\Omega - \frac{2\pi k}{N})} \cdot \Phi_{n,DIV}(N \cdot \Omega). \quad (45)$$

Since the PLL model is linear, superposition applies when more than one types of noise are present.

### III. SIMULATION RESULTS

This section presents results from event-driven behavioral PLL simulations using Verilog-A by Cadence [29]. The outputs of the Verilog-A simulations are compared to the results from the theoretical expressions derived in Section II. Two simulations of the PLL are performed, one without any external noise sources and the other with the external noise source to be analyzed. The zero crossings of the PLL output clock in the quiet simulation are subtracted from the corresponding zero crossings of the noisy simulation. The resulting waveform is the excess jitter signal, which corresponds to the external noise source alone. The PLL parameters used in simulations are shown in Table I.

The PLL blocks are implemented in Verilog-A and incorporate the ISF functions—or approximations thereof—that were derived from circuit-level simulations in Section II. This allows the effect of the supply or device noise sources to be dependent on their phase relationship to the PLL output clock and other signals.

As an example of the implementation of the PLL components, Appendix D shows the simplified Verilog-A code corresponding to the VCO. The phase of the VCO is computed as the sum of two terms. The first is simply the integral of the frequency as a function of time and corresponds to the case of a noiseless VCO. The second term is the integral of the VCO noise waveform weighted by the VCO impulse sensitivity function. When

the total phase reaches multiples of  $\pi$ , a transition of the VCO voltage waveform occurs (either low-to-high or high-to-low). The form of the ISF function is based on Fig. 4. E.g. for VCO supply noise, the ISF function used in the simulation is a sinusoid with a dc value. The frequency of the sinusoidal part of the ISF is  $8 \times$  the VCO frequency (assuming 4 VCO stages, as shown in Fig. 4).

The charge pump output current is implemented as the nominal current plus the current noise term, which is equal to the noise waveform multiplied by the charge pump ISF. The ISF value during the pull-up or pull-down operation is assumed constant, as in Fig. 6(b). Similar implementation of the ISF is used for the rest of the PLL components. It should be noted that any ISF shape can be implemented in the Verilog-A model and used in the numerical calculations.

#### A. Reference Clock Jitter

In order to verify the PLL model developed in the previous sections, we first apply sinusoidal jitter on the PLL reference clock. Fig. 8 shows the normalized PLL output jitter spectrum with 190 MHz sinusoidal jitter applied on the reference clock, i.e., the zero-crossing instances of the reference clock are modulated by a sinusoidal perturbation of frequency 190 MHz. The reference clock frequency is 200 MHz and the divide ratio is  $N = 5$ , so that the PLL clock frequency is  $f_{PLL} = 1$  GHz. The theoretical plot is obtained by using (39) for the PLL loop behavior. The simulation plot is obtained by calculating the FFT of the excess jitter signal. The PLL jitter in Fig. 8 is normalized with respect to the magnitude of the sinusoidal reference clock jitter. The various spurs that appear in the spectrum can be justified as follows: The PLL jitter spectrum is periodic with a frequency equal to 1 GHz and it is also symmetric around dc. Therefore, the spectrum is fully characterized by its content in the frequency range from dc to 500 MHz as shown in Fig. 8. The reference clock jitter at 190 MHz is sampled at the reference clock frequency of 200 MHz and therefore it is aliased back to a spur at  $f_0 = 10$  MHz. According to (39), the reference clock spectrum is upsampled by a factor of  $N = 5$ , in order to produce the PLL output spectrum. Therefore, the following spurs appear in addition to  $f_0$ , as predicted by (39) and shown in Fig. 8:  $f_{k\mp} = k \cdot f_{REF} \mp f_0 = 190, 210, 390, 410$  MHz for  $k = 1, 2$ . The presence of additional spurs cannot be predicted by a continuous-time PLL model. The agreement in the magnitudes of the main spurs (10 MHz) between simulation and theory is within 2%. The agreement in the magnitudes of the secondary spurs is within 25%. It should be noted here that the finite simulation time is taken into account in the analysis by multiplying the sinusoidal noise with an appropriate box function  $\Pi_M(t)$  as described in Appendix B. This accounts for the fact that the analytical spectrum is not composed of individual impulse functions.

Fig. 9 shows the normalized PLL output jitter spectrum when in-band sinusoidal jitter of frequency 3 MHz is applied on the reference clock. The PLL frequency is again 1 GHz and the divide ratio  $N = 5$ . In this case, in addition to the spur at  $f_0 = 3$  MHz, spurs at the following frequencies appear, as shown in Fig. 9:  $f_{k\mp} = k \cdot f_{REF} \mp f_0 = 197, 203, 397, 403$  MHz for  $k = 1, 2$ .

#### B. Charge Pump Noise

In order to verify the PLL model with respect to the charge pump noise, we apply sinusoidal noise on the charge pump voltage supply. The ISF is modeled according to the extracted

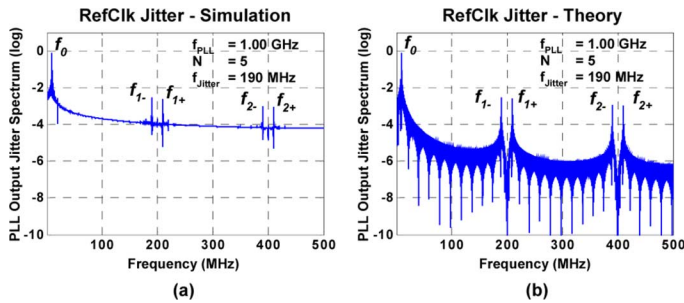


Fig. 8. Normalized output jitter spectrum due to reference clock sinusoidal jitter at 190 MHz. (a) Simulation. (b) Theory.

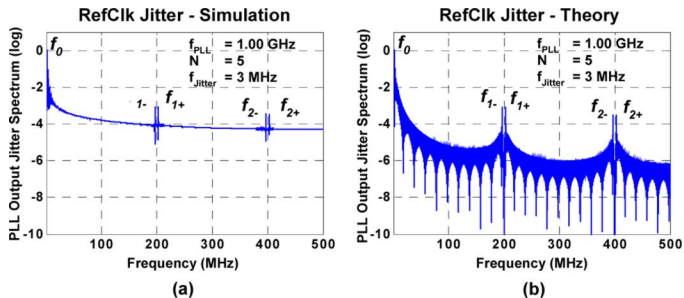


Fig. 9. Normalized output jitter spectrum due to reference clock sinusoidal jitter at 3 MHz. (a) Simulation. (b) Theory.

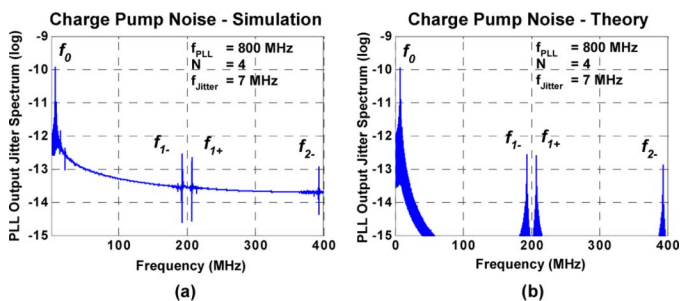


Fig. 10. Normalized output jitter spectrum due to charge pump sinusoidal supply noise at 7 MHz. (a) Simulation. (b) Theory.

ISF of Fig. 6(b), i.e., it is constant while the charge pump is ON and zero while the charge pump is OFF. The output jitter spectrum is calculated by using (71) and (41).

Fig. 10 shows the simulation and theoretical results when sinusoidal noise of frequency 7 MHz is applied on the charge pump voltage supply. The divide ratio is  $N = 4$  and the PLL output frequency is 800 MHz. In addition to the spur at  $f_0 = 7$  MHz, (41) predicts that there are additional spurs at 193, 207, and 393 MHz, as shown in Fig. 10. The PLL jitter is normalized with respect to the magnitude of the sinusoidal charge pump supply noise.

Fig. 11 depicts graphically the effect of the phase relationship between supply voltage noise and charge pump ISF. The example examines the case where the supply noise is sinusoidal with a frequency that is an integer multiple of the reference clock frequency. In Fig. 11(a) the effect of the supply noise is maximized, while in Fig. 11(b) the effect of the noise is minimized. In order to show the effect of the alignment of the noise waveform to the charge pump ISF, we apply sinusoidal noise of 1 GHz on the charge pump supply. The divide ratio is  $N = 4$  and the PLL output frequency is 800 MHz, as before. Because the noise frequency is an integer multiple of the reference clock frequency, it can be seen that the accumulated jitter is the same in each cycle, which means that the output jitter response is constant in the

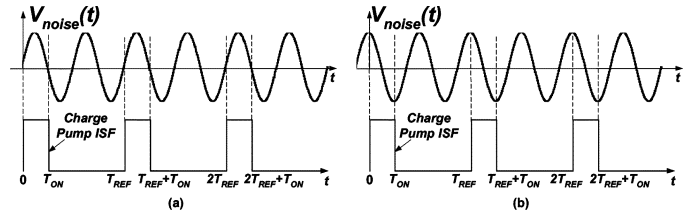


Fig. 11. Graphical interpretation of the effect of supply noise phase on charge pump current noise. The supply voltage noise is sinusoidal with a frequency that is an integer multiple of the reference clock frequency. Phase relationship to charge pump ISF for: (a) maximum noise; (b) minimum noise.

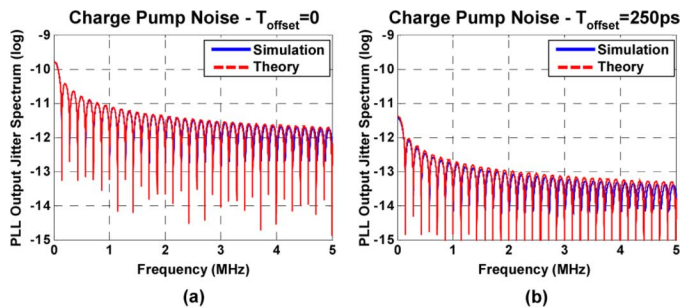


Fig. 12. Normalized output jitter spectrum due to charge pump sinusoidal supply noise at 1 GHz. The sinusoidal noise in (b) is shifted with respect to the sinusoidal noise in (a) by approximately 250 ps.

time domain. Fig. 12 shows the dc of the normalized PLL output jitter spectrum for two cases. In Fig. 12(b) the noise waveform is shifted by approximately 250 ps with respect to the noise waveform in Fig. 12(a). We can see that this affects the magnitude of the dc component in the spectrum, which is reduced by approximately 98%. This is an effect that cannot be captured by a time-invariant PLL model, yet is critical to consider in digital applications where most of the noise events are synchronized to a clock and are not time-invariant.

Fig. 13 shows the normalized output jitter power spectral density due to white noise on the charge pump supply. The PSD of the current noise injected into the PLL loop is calculated using (26). The output jitter PSD is calculated using (46), which is derived from (41). The simulation plot is calculated by finding the power spectral density of the excess jitter signal

$$S_{CP}(\Omega) = \left| \frac{\frac{1}{f_{PLL}} \cdot \frac{H(\Omega)}{K_p}}{1 + \frac{1}{N} \sum_{k=0}^{N-1} H\left(\Omega - \frac{2\pi k}{N}\right)} \right|^2 \cdot \frac{I_{n,CP}^{White}(\Omega)}{N} \quad (46)$$

### C. VCO Noise

In order to verify the PLL model with respect to the VCO noise, we first apply impulse noise on the VCO supply at two different time instances as shown in Fig. 14. The simulation plot is obtained from the FFT of the impulse response, while the theoretical plot is calculated from (42) with  $\Phi_{n,VCO}(\Omega)$  given in (12). Fig. 14 shows the spectrum of the PLL output jitter in the two cases when a VCO supply noise impulse is applied at the maximum and 40% of the maximum of the VCO ISF. Comparing the plots of Fig. 14(a) and (b) shows a change in the magnitude of the jitter spectrum as a result of the periodically time-varying nature of the VCO circuit.

In order to study the aliasing effects of jitter, sinusoidal voltage noise at 190 MHz is applied on the VCO supply at a PLL operating frequency of  $f_{PLL} = 1$  GHz and divide ratio  $N = 5$ . The loop bandwidth of the PLL is 9.7 MHz. Fig. 15



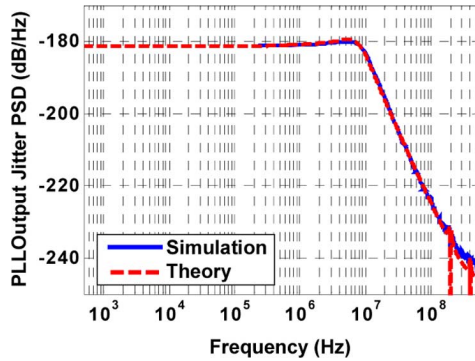


Fig. 13. Normalized output jitter power spectral density due to charge pump white supply noise. The PLL operating frequency is 1 GHz and the divide ratio  $N = 5$ .

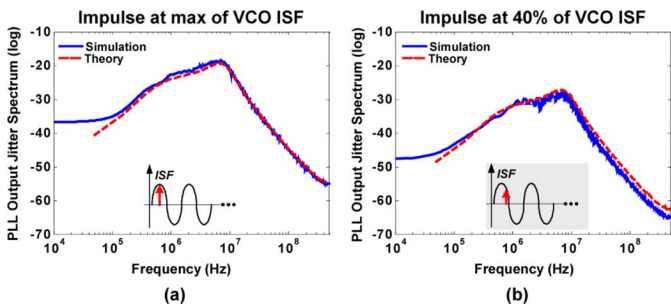


Fig. 14. Normalized spectrum of PLL output jitter when applying a VCO supply noise impulse. The PLL operating frequency is 1 GHz and the divide ratio is  $N = 5$ . The VCO supply noise impulse is applied: (a) at the ISF maximum; (b) at 40% of the ISF maximum.

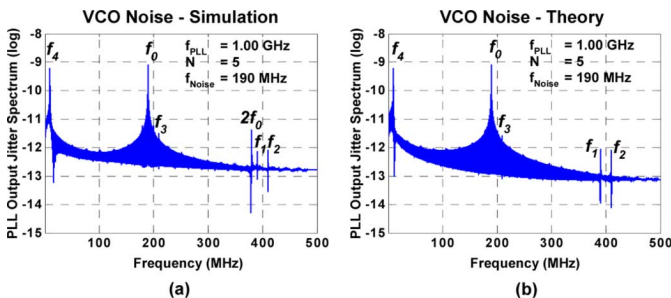


Fig. 15. Normalized output jitter spectrum due to VCO sinusoidal supply noise at 190 MHz. (a) Simulation. (b) Theory.

shows the PLL output jitter spectrum normalized to the amplitude of the VCO supply noise. The theoretical plot is obtained by using (67) for the input noise spectrum and (42) for the PLL loop behavior. From (42) it can be seen that there are  $N - 1 = 4$  spurs that are predicted by the theory in addition to the spur at the input noise frequency of  $f_0 = 190$  MHz. From (42) and taking again the periodicity and symmetry of the spectrum into account, these spurs appear at the following frequencies:  $f_k = f_0 + k \times \frac{f_{PLL}}{N} = 390, 410, 210, 10$  MHz for  $k = 1, \dots, 4$ .

These frequencies are denoted in Fig. 15. It should be noted here that the jitter spectrum in Fig. 15(a), which is obtained through simulation, exhibits a harmonic spur at  $2 \cdot f_0 = 380$  MHz. This harmonic is due to nonlinearities in the simulation process and cannot be predicted by the PLL model, since it is linear. Fig. 15 shows that even when the VCO supply noise frequency is out-of-band (as is the case with wideband supply noise), one of the resulting frequencies can fall in-band, thus potentially affecting the system performance. This behavior cannot be predicted by a continuous-time model.

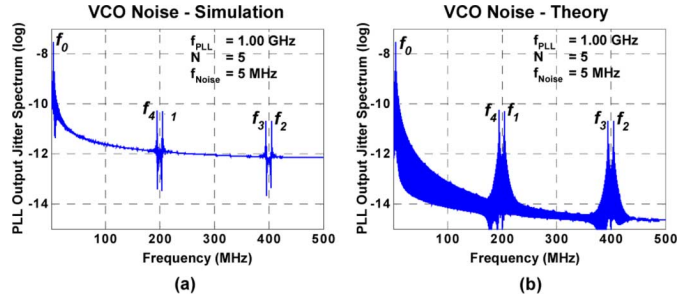


Fig. 16. Normalized output jitter spectrum due to VCO sinusoidal supply noise at 5 MHz. (a) Simulation. (b) Theory.

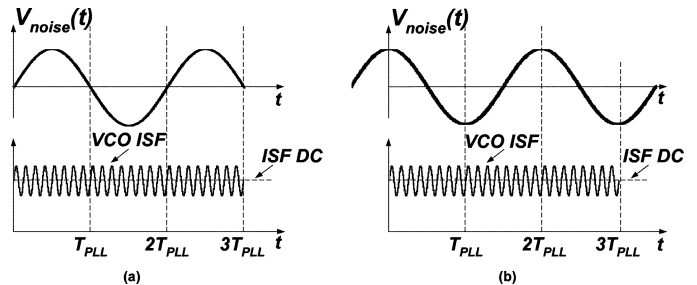


Fig. 17. Graphical interpretation of the effect of supply noise phase on VCO phase noise. The supply noise is sinusoidal with a frequency that is half of the VCO frequency. (a) and (b) show two extreme phase relationships between supply noise and VCO ISF.

Fig. 16 shows the normalized output jitter spectrum when the sinusoidal VCO supply noise has an in-band frequency of  $f_0 = 5$  MHz. The PLL output frequency is 1 GHz and the divide ratio  $N = 5$  as before. The additional spurs according to (42) appear at the following frequencies, as shown in Fig. 16:  $f_k = f_0 + k \times \frac{f_{PLL}}{N} = 205, 405, 395, 195$  MHz for  $k = 1, \dots, 4$ .

Fig. 17 illustrates the effect of the phase relationship between supply voltage noise and VCO ISF. The example examines the case where the supply noise is sinusoidal with a frequency that is half of the VCO frequency. Fig. 17(a) and (b) show two extremes of this phase relationship. In order to show the effect of the phase relationship of the noise waveform to the VCO ISF, we apply sinusoidal noise of 500 MHz on the VCO supply. The PLL frequency is again 1 GHz and the divide ratio  $N = 5$ , as before. Fig. 18 shows the magnitude of the normalized PLL output jitter spectrum at 500 MHz for two cases. In Fig. 18(b) the noise waveform is shifted by 500 ps with respect to the noise waveform in Fig. 18(a). We can see that this affects the magnitude of the 500 MHz component in the spectrum, which is reduced by approximately 99%. As before, this effect can not be captured by a time-invariant PLL model.

#### D. VCO Buffer

The ISF of the VCO buffer is modeled as a sinusoidal function with a dc component when the VCO signal edges travel through the buffer and zero otherwise, see Fig. 7(a). Fig. 19 shows the simulation and theoretical plots when sinusoidal noise of frequency  $f_0 = 190$  MHz is applied on the VCO buffer supply. The PLL behavior is calculated according to (43). The additional spurs predicted by (43) are the same as in the VCO case and shown in Fig. 19:  $f_k = f_0 + k \times \frac{f_{PLL}}{N} = 390, 410, 210, 10$  MHz for  $k = 1, \dots, 4$ .

As in the VCO case, the harmonic spur at  $2f_0 = 380$  MHz present in the simulation plot cannot be predicted by the linear PLL model.

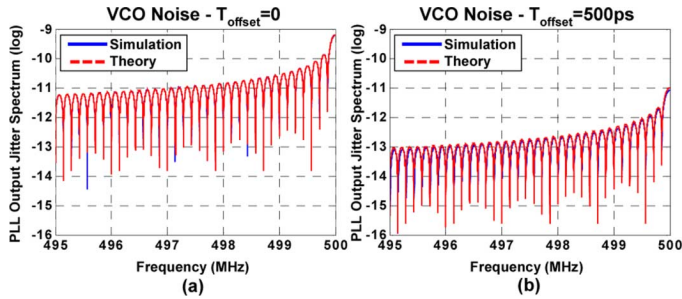


Fig. 18. Normalized output jitter spectrum due to VCO sinusoidal supply noise at 500 MHz. The PLL operating frequency is 1 GHz and the divide ratio  $N = 5$ . The sinusoidal noise in (b) is shifted with respect to the sinusoidal noise in (a) by 500 ps.

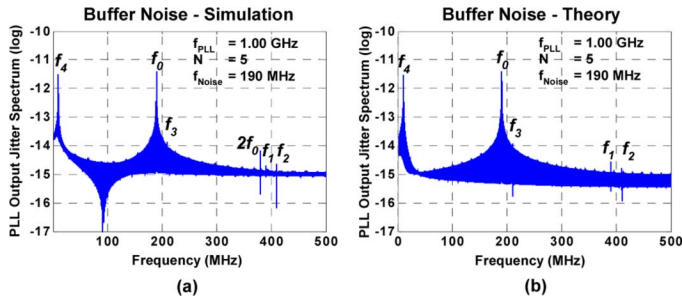


Fig. 19. Normalized output jitter spectrum due to VCO buffer sinusoidal supply noise at 190 MHz. (a) Simulation. (b) Theory.

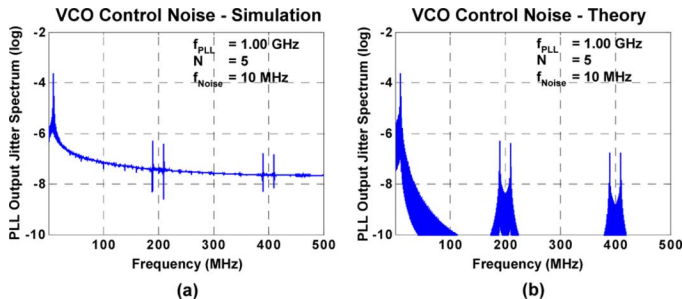


Fig. 20. Normalized output jitter spectrum due to sinusoidal current noise at 10 MHz injected into the VCO control node. (a) Simulation. (b) Theory.

### E. VCO Control Node

Fig. 20 shows the simulation and theoretical results for the normalized PLL output jitter spectrum when sinusoidal current noise of frequency 10 MHz is injected into the VCO control node. The additional spurs are predicted by (44).

### F. Divider

Fig. 21 shows the simulation and theoretical results for the normalized PLL output jitter spectrum when sinusoidal supply noise of frequency 10 MHz is applied on the divider supply voltage. The spurs are predicted by (45).

## IV. CONCLUSION

A discrete-time, linear, periodically time-variant PLL model for jitter analysis is proposed. It accounts for the periodically time-varying nature of PLL components, and also captures the aliasing of jitter due to downsampling and upsampling of the jitter signal around the PLL loop, when the divide ratio  $N$  is greater than unity. Expressions were derived for the noise spectra injected into the loop by generalizing the mapping concept of the Impulse Sensitivity Function. Capturing these periodically time-varying and aliasing effects is

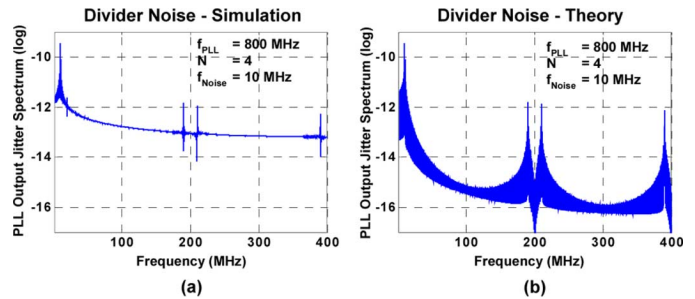


Fig. 21. Normalized output jitter spectrum due to divider sinusoidal supply noise at 10 MHz. (a) Simulation. (b) Theory.

critical in highly integrated digital applications where most noise sources (supply, ground, substrate) are time-variant with spurious frequency content. In addition, accurate determination of the frequency content of the PLL output clock can be used in frequency planning and coexistence analysis. Behavioral simulations of a third-order PLL verify the theoretical results.

## APPENDIX A

This appendix presents the derivation of the discrete-time model for the loop filter/VCO combination. The combination of the loop filter and VCO is modeled using the impulse invariant transformation technique [8], [12]. The idea behind this technique is that in steady-state operation the phase error between the feedback clock and the reference clock at the input of the phase-frequency detector (PFD) is small. Therefore, the corrective current pulses produced by the charge pump are short and can be approximated by weighted impulse functions. Hence, in translating the PLL model from continuous to discrete time, it is only necessary to preserve the impulse response of the loop filter and VCO combination. This process is shown in what follows.

The continuous-time transfer function of the loop filter and VCO in the  $s$ -domain is

$$H_{\text{LF,VCO}}(s) = H_{\text{LF}}(s) \times \frac{K_V}{s} = \frac{K_V \cdot (1 + sCR)}{s^2 \cdot [sCC_2R + (C + C_2)]} \quad (47)$$

where  $K_V$  is the VCO frequency gain and  $R, C, C_2$  are as defined in Fig. 1. We would like to express the above transfer function in the form

$$H_{\text{LF,VCO}}(s) \equiv \frac{A'}{s^2} + \frac{B'}{s} + \frac{E'}{sCC_2R + (C + C_2)}. \quad (48)$$

By equating the numerator coefficients in (47) and (48) for the corresponding powers of  $s$ , we have the following results:

$$A' = \frac{K_V}{C + C_2}, B' = \frac{K_V C^2 R}{(C + C_2)^2}, E' = -\frac{K_V C^3 C_2 R^2}{(C + C_2)^2}. \quad (49)$$

Hence, the transfer function can be written as

$$H_{\text{LF,VCO}}(s) = \frac{A'}{s^2} + \frac{B'}{s} + \frac{E''}{s + \frac{C+C_2}{CC_2R}} \quad (50)$$

where  $E'' = -\frac{K_V C^2 R}{(C + C_2)^2}$ .

The continuous time impulse response that corresponds to the above transfer function is

$$h_{\text{LF,VCO}}(t) = A' \cdot t \cdot u(t) + B' \cdot u(t) + E'' \cdot e^{-(C+C_2)t/(CC_2R)} \cdot u(t) \quad (51)$$

where  $u(t)$  is the step function.

Taking into account the nominal buffer delay  $T_{\text{BUF0}}$ , the corresponding discrete time impulse response at the time instants  $nT + T_{\text{BUF0}}$ , is

$$\begin{aligned} h_{\text{LF,VCO}}[n] &\equiv h_{\text{LF,VCO}}(nT + T_{\text{BUF0}}) \\ &= A' \cdot T \cdot n \cdot u[n] + (B' + A' \cdot T_{\text{BUF0}}) \cdot u[n] \\ &\quad + E'' \cdot e^{-((C+C_2)/(CC_2R))T_{\text{BUF0}}} \\ &\quad \cdot e^{-((C+C_2)/(CC_2R))T \cdot n} \cdot u[n], \end{aligned} \quad (52)$$

The discrete-time Fourier transform of  $h_{\text{LF,VCO}}[n]$  is given by

$$\begin{aligned} H_{\text{LF,VCO}}(\Omega) &= \frac{A \cdot e^{-j\Omega}}{(1 - e^{-j\Omega})^2} + \frac{B}{1 - e^{-j\Omega}} \\ &\quad + \frac{E}{1 - e^{-((C+C_2)/(CC_2R))T} \cdot e^{-j\Omega}} \end{aligned} \quad (53)$$

where the coefficients  $A$ ,  $B$ ,  $E$  are given by (5)–(7).

## APPENDIX B

This appendix gives the procedure for calculating the noise spectrum injected into the PLL loop when the noise waveform is sinusoidal. We consider the separate cases of VCO and charge pump below:

- a) *VCO*: Let the VCO supply or device noise  $i(\tau)$  be a deterministic sinusoidal function given by  $i(\tau) = A_1 \cdot \cos(\omega'_1 \tau + \theta_1)$ . From (11) we have

$$\begin{aligned} \Phi_{n,\text{VCO}}(\Omega) &= \Phi_{n,\text{VCO}}(\Omega) \cdot e^{-j\Omega} \\ &\quad + \int_0^T \Gamma_{\text{VCO}}(\tau) \cdot \left[ \sum_{k=-\infty}^{\infty} e^{-j\Omega k} \cdot i(\tau + (k-1)T) \right] d\tau. \end{aligned} \quad (54)$$

The quantity in brackets is the DTFT of the sequence  $i[k] \equiv i(\tau + (k-1)T)$ , which can be written as

$$\begin{aligned} i[k] &= i(\tau + (k-1)T) \\ &= A_1 \cdot \cos[\omega'_1 \cdot \tau + (k-1) \cdot \omega'_1 \cdot T + \theta_1] \\ &= A_1 \cdot \cos[k \cdot \omega'_1 \cdot T] \cdot \cos[\omega'_1 \cdot \tau - \omega'_1 \cdot T + \theta_1] \\ &\quad - A_1 \cdot \sin[k \cdot \omega'_1 \cdot T] \cdot \sin[\omega'_1 \cdot \tau - \omega'_1 \cdot T + \theta_1] \\ &\equiv Q_c(\tau, \omega'_1, \theta_1) \cdot \cos[k \cdot \omega'_1 \cdot T] \\ &\quad - Q_s(\tau, \omega'_1, \theta_1) \cdot \sin[k \cdot \omega'_1 \cdot T] \end{aligned} \quad (55)$$

where

$$Q_c(\tau, \omega'_1, \theta_1) = A_1 \cdot \cos[\omega'_1 \cdot \tau - \omega'_1 \cdot T + \theta_1] \quad (56a)$$

$$Q_s(\tau, \omega'_1, \theta_1) = A_1 \cdot \sin[\omega'_1 \cdot \tau - \omega'_1 \cdot T + \theta_1]. \quad (56b)$$

Therefore, the DTFT of the sequence is given by

$$\begin{aligned} I(\Omega, \tau) &= Q_c(\tau, \omega'_1, \theta_1) \cdot \pi \cdot \{\delta(\Omega - \omega_1 T) + \delta(\Omega + \omega_1 T)\} \\ &\quad - j Q_s(\tau, \omega'_1, \theta_1) \cdot \pi \cdot \{\delta(\Omega - \omega_1 T) - \delta(\Omega + \omega_1 T)\} \\ \Rightarrow I(\Omega, \tau) &= \pi [Q_c(\tau, \omega'_1, \theta_1) - j Q_s(\tau, \omega'_1, \theta_1)] \cdot \delta(\Omega - \omega_1 T) \\ &\quad + \pi [Q_c(\tau, \omega'_1, \theta_1) + j Q_s(\tau, \omega'_1, \theta_1)] \cdot \delta(\Omega + \omega_1 T) \end{aligned} \quad (57)$$

where  $\omega_1 T$  satisfies (16). Using the previous results we have

$$\begin{aligned} \Phi_{n,\text{VCO}}(\Omega) &= \Phi_{n,\text{VCO}}(\Omega) \cdot e^{-j\Omega} + \pi \cdot \delta(\Omega - \omega_1 T) \\ &\quad \cdot \int_0^T \Gamma_{\text{VCO}}(\tau) \cdot [Q_c(\tau, \omega'_1, \theta_1) - j Q_s(\tau, \omega'_1, \theta_1)] d\tau \\ &\quad + \pi \cdot \delta(\Omega + \omega_1 T) \\ &\quad \cdot \int_0^T \Gamma_{\text{VCO}}(\tau) \cdot [Q_c(\tau, \omega'_1, \theta_1) + j Q_s(\tau, \omega'_1, \theta_1)] d\tau \end{aligned} \quad (58)$$

or finally

$$\begin{aligned} \Phi_{n,\text{VCO}}(\Omega) &= \frac{\pi}{1 - e^{-j\Omega}} \\ &\quad \cdot \left\{ Q_1(\omega'_1, \theta_1) \cdot \delta(\Omega - \omega_1 T) \right. \\ &\quad \left. + Q_2(\omega'_1, \theta_1) \cdot \delta(\Omega + \omega_1 T) \right\} \end{aligned} \quad (59)$$

where

$$\begin{aligned} Q_1(\omega'_1, \theta_1) &= \\ &\quad \int_0^T \Gamma_{\text{VCO}}(\tau) \cdot [Q_c(\tau, \omega'_1, \theta_1) - j Q_s(\tau, \omega'_1, \theta_1)] d\tau \end{aligned} \quad (60a)$$

$$\begin{aligned} Q_2(\omega'_1, \theta_1) &= \\ &\quad \int_0^T \Gamma_{\text{VCO}}(\tau) \cdot [Q_c(\tau, \omega'_1, \theta_1) + j Q_s(\tau, \omega'_1, \theta_1)] d\tau. \end{aligned} \quad (60b)$$

The finite duration of the sinusoidal waveform needs also to be taken into account in the analysis, in order to get better agreement with simulation. Instead of an ideal sinusoid, the supply/device noise waveform should be expressed as

$$i(\tau) = A_1 \cdot \cos(\omega'_1 \tau + \theta_1) \times \Pi_M(\tau) \quad (61)$$

where  $\Pi_M(t) \equiv u(t) - u(t - M \cdot T)$  is the box function extending from 0 to  $M \cdot T$ . Therefore, the discrete-time noise waveform in (55) is expressed as

$$\begin{aligned} i[k] &= Q_c(\tau, \omega'_1, \theta_1) \cdot \cos[k \cdot \omega'_1 \cdot T] \cdot \Pi_M[k] \\ &\quad - Q_s(\tau, \omega'_1, \theta_1) \cdot \sin[k \cdot \omega'_1 \cdot T] \cdot \Pi_M[k] \end{aligned} \quad (62)$$

where  $\Pi_M[k] \equiv u[k] - u[k - M]$ . The discrete-time Fourier transform of the term  $\cos[k \cdot \omega'_1 \cdot T] \cdot \Pi_M[k]$  is given by the following convolution integral [31]:

$$\begin{aligned} G_1[\Omega] &= \frac{1}{2\pi} \cdot \int_{-\pi}^{\pi} \pi \cdot [\delta(\theta - \omega_1 T) + \delta(\theta + \omega_1 T)] \\ &\quad \cdot \frac{\sin[(M+1) \cdot \frac{\Omega - \theta}{2}]}{\sin[\frac{\Omega - \theta}{2}]} \cdot e^{-jM(\Omega - \theta)/2} d\theta \\ &\equiv \frac{1}{2} \cdot [V_1(\Omega) + V_2(\Omega)] \end{aligned} \quad (63)$$

where again  $\omega_1 T$  satisfies (16) and

$$V_1(\Omega) \equiv \frac{\sin \left[ (M+1) \cdot \frac{\Omega - \omega_1 T}{2} \right]}{\sin \left[ \frac{\Omega - \omega_1 T}{2} \right]} \cdot e^{-jM((\Omega - \omega_1 T)/2)} \quad (64a)$$

$$V_2(\Omega) \equiv \frac{\sin \left[ (M+1) \cdot \frac{\Omega + \omega_1 T}{2} \right]}{\sin \left[ \frac{\Omega + \omega_1 T}{2} \right]} \cdot e^{-jM((\Omega + \omega_1 T)/2)}. \quad (64b)$$

Similarly, the DTFT of the term  $\sin [k \cdot \omega'_1 \cdot T] \cdot \Pi_M[k]$  is equal to

$$G_2(\Omega) = -\frac{j}{2} \cdot [V_1(\Omega) - V_2(\Omega)]. \quad (65)$$

Hence, (57) becomes

$$I(\Omega, \tau) = \frac{1}{2} [Q_c(\tau, \omega'_1, \theta_1) - jQ_s(\tau, \omega'_1, \theta_1)] \cdot V_1(\Omega) + \frac{1}{2} [Q_c(\tau, \omega'_1, \theta_1) + jQ_s(\tau, \omega'_1, \theta_1)] \cdot V_2(\Omega). \quad (66)$$

Finally, (59) becomes

$$\Phi_{n,\text{VCO}}(\Omega) = \frac{0.5}{1 - e^{-j\Omega}} \cdot \{Q_1(\omega'_1, \theta_1) \cdot V_1(\Omega) + Q_2(\omega'_1, \theta_1) \cdot V_2(\Omega)\}. \quad (67)$$

- b) *Charge Pump*: Let the charge pump supply or device noise  $i(\tau)$  be a deterministic sinusoidal function given by the expression  $i(\tau) = A_1 \cdot \cos(\omega'_1 t + \theta_1)$ . From (20) we have

$$I_{n,\text{CP}}(\Omega) = \int_0^{T_{\text{REF}}} \Gamma_{\text{CP}}(\tau) \cdot \left[ \sum_{k=-\infty}^{\infty} e^{-j\Omega k} \cdot i(\tau + (k-1)T_{\text{REF}}) \right] d\tau. \quad (68)$$

The quantity in brackets is the DTFT  $I(\Omega, \tau)$  of the sequence  $i[k] \equiv i(\tau + (k-1)T_{\text{REF}})$ . Using the same derivation as in the VCO case,  $I(\Omega, \tau)$  is given by

$$I(\Omega, \tau) = \pi [Q_c(\tau, \omega'_1, \theta_1) - jQ_s(\tau, \omega'_1, \theta_1)] \cdot \delta(\Omega - \omega_1 T_{\text{REF}}) + \pi [Q_c(\tau, \omega'_1, \theta_1) + jQ_s(\tau, \omega'_1, \theta_1)] \cdot \delta(\Omega + \omega_1 T_{\text{REF}}) \quad (69)$$

where  $Q_c, Q_s$  are given by (30) and  $\omega_1 T_{\text{REF}}$  satisfies (28). Using the previous results we have

$$I_{n,\text{CP}}(\Omega) = \pi \cdot \left\{ Q_1(\omega'_1, \theta_1) \cdot \delta(\Omega - \omega_1 T) + Q_2(\omega'_1, \theta_1) \cdot \delta(\Omega + \omega_1 T) \right\} \quad (70)$$

where  $Q_1, Q_2$  are given by (29).

As in the case of the VCO, the finite duration of the sinusoidal waveform needs to be taken into account in the analysis, in order to obtain better agreement with simulation. Using a similar analysis as in the VCO case, (70) becomes

$$I_{n,\text{CP}}(\Omega) = \frac{1}{2} \{Q_1(\omega'_1, \theta_1) \cdot V_1(\Omega) + Q_2(\omega'_1, \theta_1) \cdot V_2(\Omega)\} \quad (71)$$

where  $V_1, V_2$  are given by (64).

## APPENDIX C

In this appendix the closed-loop transfer functions from the noise sources of Fig. 1 to the PLL output jitter are derived.

In order to calculate the closed-loop transfer function from the reference clock jitter to the PLL output jitter, we remove all other noise sources except  $\phi_{n,\text{REF}}$  in Fig. 1. The resulting block diagram can be simplified as shown in Fig. 22(a), where  $\Phi_{n,\text{REF}}(\Omega)$  denotes the reference clock jitter,  $Y_{\text{REF}}(\Omega)$  is the PLL output jitter due to reference clock jitter and the transfer function  $H(\Omega)$  is given by (40).

The relationship between the input and output spectrum in Fig. 22(a) is given by

$$(\Phi_{n,\text{REF}}(N \cdot \Omega) - Y_{FB}(N \cdot \Omega)) \cdot H(\Omega) = Y_{\text{REF}}(\Omega). \quad (72)$$

The feedback signal  $Y_{FB}$  is the downsampled version of the output  $Y_{\text{REF}}$  and can therefore be written as

$$Y_{FB}(\Omega) = \frac{1}{N} \sum_{k=0}^{N-1} Y_{\text{REF}} \left( \frac{\Omega - 2\pi k}{N} \right). \quad (73)$$

Hence, we get

$$\left( \Phi_{n,\text{REF}}(N \cdot \Omega) - \frac{1}{N} \sum_{k=0}^{N-1} Y_{\text{REF}} \left( \Omega - \frac{2\pi k}{N} \right) \right) \cdot H(\Omega) = Y_{\text{REF}}(\Omega). \quad (74)$$

We let  $\Omega = \Omega - \frac{2\pi q}{N}, q = 0, 1, 2, \dots, N-1$  in (74). Then we get the following set of equations by noting that  $\Phi_{n,\text{REF}}(\Omega)$  and  $Y_{\text{REF}}(\Omega)$  are periodic with period  $2\pi$ :

$$\left( \Phi_{n,\text{REF}}(N \cdot \Omega) - \frac{1}{N} \sum_{k=0}^{N-1} Y_{\text{REF}} \left( \Omega - \frac{2\pi k}{N} \right) \right) \cdot H \left( \Omega - \frac{2\pi q}{N} \right) = Y_{\text{REF}} \left( \Omega - \frac{2\pi q}{N} \right). \quad (75)$$

By summing the left and right parts of (75) for  $q = 0, 1, 2, \dots, N-1$ , we get

$$\left( \Phi_{n,\text{REF}}(N \cdot \Omega) - \frac{1}{N} \sum_{k=0}^{N-1} Y_{\text{REF}} \left( \Omega - \frac{2\pi k}{N} \right) \right) \cdot \sum_{k=0}^{N-1} H \left( \Omega - \frac{2\pi k}{N} \right) = \sum_{k=0}^{N-1} Y_{\text{REF}} \left( \Omega - \frac{2\pi k}{N} \right). \quad (76)$$

We can solve the above equation for the aliased spectrum

$$\sum_{k=0}^{N-1} Y_{\text{REF}} \left( \Omega - \frac{2\pi k}{N} \right) = \frac{\sum_{k=0}^{N-1} H \left( \Omega - \frac{2\pi k}{N} \right)}{1 + \frac{1}{N} \sum_{k=0}^{N-1} H \left( \Omega - \frac{2\pi k}{N} \right)} \cdot \Phi_{n,\text{REF}}(N \cdot \Omega). \quad (77)$$

Using (77) in (74), we obtain (39) for the output spectrum due to the reference clock jitter.

Fig. 22(b) shows the block diagram used for calculating the transfer function from the charge pump current noise  $I_{n,\text{CP}}$  to the output jitter. The quantity  $H(\Omega)$  is given by (40). The  $1/f_{\text{PLL}}$  block is due to the fact that the charge pump current noise is weighted by the same factor as shown in the expression for  $K_P$  in (3). Using the same procedure as in the case of reference clock jitter, we obtain (41) for the output jitter spectrum due to charge pump current noise. The charge pump current noise spectrum  $I_{n,\text{CP}}(\Omega)$  is calculated in Section II-B for various cases.

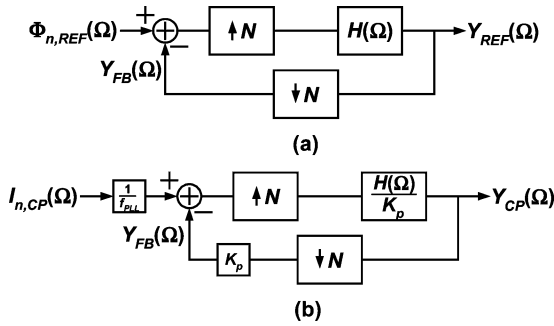


Fig. 22. Block diagrams for calculating closed-loop noise transfer functions. (a) Reference clock jitter. (b) Charge pump current noise.

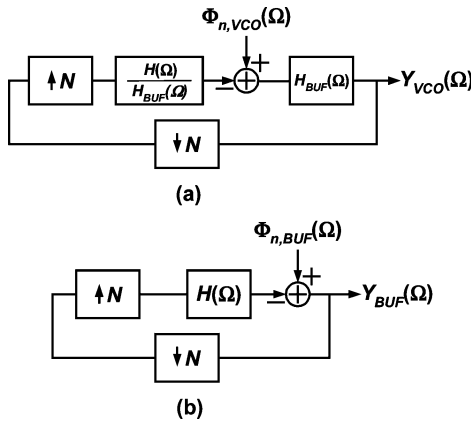


Fig. 23. Block diagrams for calculating closed-loop noise transfer functions. (a) VCO phase noise. (b) Buffer phase noise.

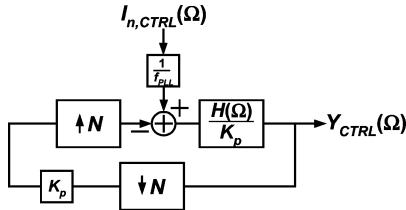


Fig. 24. Block diagram for calculating the closed-loop noise transfer function for the VCO control node noise.

In order to calculate the closed-loop transfer function from the VCO phase noise to the PLL output jitter, the block diagram of Fig. 23(a) can be used, where the quantity  $H(\Omega)$  is again given by (40). From this block diagram we get

$$\left( \Phi_{n,VCO}(\Omega) - \frac{1}{N} \sum_{k=0}^{N-1} Y_{VCO} \left( \Omega - \frac{2\pi k}{N} \right) \cdot \frac{H(\Omega)}{H_{BUF}(\Omega)} \right) \cdot H_{BUF}(\Omega) = Y_{VCO}(\Omega). \quad (78)$$

Using a similar process as in the case of the reference clock jitter, we can solve for the aliased spectrum and eventually obtain (42) for the PLL output jitter spectrum due to VCO phase noise [32]. The VCO phase noise spectrum  $\Phi_{n,VCO}(\Omega)$  is calculated in Section II-B for various cases.

Fig. 23(b) shows the block diagram for calculating the transfer function from the VCO buffer noise to the PLL output jitter. Using the same procedure as previously, the output jitter spectrum due to the VCO buffer noise is given by (43).

Fig. 24 shows the block diagram for calculating the transfer function from the VCO control node noise to the PLL output jitter. Using a similar procedure as in the previous cases, the

```

#include "discipline.h"
#include "constants.h"

module VCO(vctrl, vnoise, vout);
input vctrl, vnoise;
output vout;
electrical vctrl, vout, vnoise;
parameter real VDD = 1.0; // supply voltage
parameter real center_freq=1.0e9; // VCO center frequency
parameter real vco_gain = 1.2e9; // VCO gain
parameter real vctrl0 = 0.5*VDD; // Vctrl corresponding to VCO center frequency
parameter real tdel = 0 from (0:inf); // Delay of output transition
parameter real trf = 20p from (0:inf); // Rise/Fall time of output transition
parameter real A_ISF = 0.2 from (0:inf); // Amplitude of sinusoidal part of ISF
parameter real Adc_ISF = 9 from (0:inf); // DC value of ISF
parameter real K_ISF = 8 from (0:inf); // Ratio of ISF frequency to VCO frequency

real freq; // VCO frequency
real vout_val; // VCO output
real PhaseVal0; // Noiseless VCO phase
real NoiseVal; // Instantaneous VCO phase noise
real PhaseVal; // Total VCO phase
real ISFVal; // Instantaneous ISF value
real Nperiod; // Number of periods, half-periods

analog begin
    @ ( initial_step ) begin
        vout_val = VDD;
        PhaseVal = 0.0;
        Nperiod = 1.0;
        Nhalfperiod = 0.5;
    end

    // Instantaneous VCO frequency:
    freq = center_freq + vco_gain*(V(vctrl)-Vctrl0);

    // Noiseless VCO phase:
    PhaseVal0 = idt(freq, 0);

    // VCO phase noise:
    ISFVal = Adc_ISF + A_ISF*cos(2*M_PI*K_ISF*PhaseVal);
    NoiseVal = idt(freq*vnoise)*ISFVal, 0);

    // Total VCO phase:
    PhaseVal = PhaseVal0 + NoiseVal;

    // Positive transition when phase crosses Nperiod:
    @ (cross(PhaseVal - Nperiod, +1)) begin
        vout_val = VDD;
        Nperiod = Nperiod + 1.0;
    end

    // Negative transition when phase crosses Nhalfperiod:
    @ (cross(PhaseVal - Nhalfperiod, +1)) begin
        vout_val = 0;
        Nhalfperiod = Nhalfperiod + 1.0;
    end

    V(vout) <+ transition(vout_val, tdel, trf, trf);
end
endmodule
    
```

Fig. 25. Verilog-A implementation of VCO.

output jitter spectrum due to the current noise injected into the VCO control node is given by (44).

## APPENDIX D

Fig. 25 shows a simplified version of the Verilog-A code used for the modeling of the VCO. The VCO ISF is modeled as a sinusoid with a dc value, as in Fig. 4(a).

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## REFERENCES

- [1] A. Mehrotra, "Noise analysis of phase-locked loops," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 9, pp. 1309–1316, Sep. 2002.
- [2] J. Kim, J. Ren, and M. A. Horowitz, "Stochastic steady-state and AC analyses of mixed-signal systems," in *Proc. 46th ACM/IEEE Design Autom. Conf. (DAC)*, 2009, pp. 376–381.
- [3] J. G. Maneatis, "Design of high-speed CMOS PLLs and DLLs," in *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan, Ed. *et al.* New York: IEEE Press, 2001, pp. 235–260.
- [4] D. C. Lee, "Analysis of jitter in phase-locked loops," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 11, pp. 704–711, Nov. 2002.
- [5] F. Herzel, S. A. Osmany, and J. C. Scheytt, "Analytical phase-noise modeling and charge pump optimization for fractional- $N$  PLLs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1914–1924, Aug. 2010.
- [6] M. Mansuri and C.-K. K. Yang, "Jitter optimization based on phase-lock loop design parameters," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1375–1382, Nov. 2002.

- [7] F. M. Gardner, "Charge-pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, pp. 1849–1858, Nov. 1980.
- [8] J. P. Hein and J. W. Scott, "Z-domain model for discrete-time PLL's," *IEEE Trans. Circuits Syst.*, vol. 35, pp. 1393–1400, Nov. 1988.
- [9] B. Kim, T. C. Weigandt, and P. R. Gray, "PLL/DLL system noise analysis for low jitter clock synthesizer design," in *Proc. 1994 IEEE Int. Symp. Circuits Syst. (ISCAS'94)*, vol. 4, pp. 31–34.
- [10] P. K. Hanumolu, M. Brownlee, K. Mayaram, and U. K. Moon, "Analysis of charge-pump phase-locked loops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, pp. 1665–1674, Sep. 2004.
- [11] K. Lim, C.-H. Park, D.-S. Kim, and B. Kim, "A low-noise phase-locked loop design by loop bandwidth optimization," *IEEE J. Solid-State Circuits*, vol. 35, pp. 807–815, Jun. 2000.
- [12] J. Lu, B. Grung, S. Anderson, and S. Rokhsaz, "Discrete z-domain analysis of high order phase locked loops," in *Proc. 2001 IEEE Int. Symp. Circuits Syst. (ISCAS'01)*, vol. 1, pp. 260–263.
- [13] J. Kim, M. A. Horowitz, and G.-Y. Wei, "Design of CMOS adaptive-bandwidth PLL/DLLs: A general approach," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 11, pp. 860–869, Nov. 2003.
- [14] J. Kovacs, "Analyze PLLs with discrete-time modeling," *Microw. RF*, pp. 224–229, May 1991.
- [15] M. Terrovitis, Simulating the phase noise contribution of the divider in a phase lock loop [Online]. Available: <http://www.designers-guide.org>
- [16] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, pp. 179–194, Feb. 1998.
- [17] J. Phillips and K. Kundert, "Noise in mixers, oscillators, samplers and logic: An introduction to cyclostationary noise," in *Proc. IEEE Custom Integr. Circuit Conf.*, May 2000, pp. 20.1.1–20.1.8.
- [18] J. Kim, B. S. Leibowitz, and M. Jeeradi, "Impulse sensitivity function analysis of periodic circuits," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2008, pp. 386–391.
- [19] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 790–804, Jun. 1999.
- [20] N. Barton, D. Öziş, T. Fiez, and K. Mayaram, "Analysis of jitter in ring oscillators due to deterministic noise," in *Proc. 2002 IEEE Int. Symp. Circuits Syst. (ISCAS'02)*, vol. 4, pp. 393–396.
- [21] N. Barton, D. Öziş, T. Fiez, and K. Mayaram, "The effect of supply and substrate noise on jitter in ring oscillators," in *Proc. IEEE Custom Integr. Circuit Conf.*, 2002, pp. 25.3.1–25.3.4.
- [22] H. H. Y. Chan and Z. Zilic, "Estimating phase-locked loop jitter due to substrate coupling: A cyclostationary approach," in *Proc. 5th Int. Symp. Quality Electron. Design (ISQED)*, 2004, pp. 309–314.
- [23] J. W. Kim, Y.-C. Lu, and R. W. Dutton, "Modeling and simulation of jitter in phase-locked loops due to substrate noise," in *Proc. 2005 IEEE Int. Behav. Model. Simul. Workshop (BMAS)*, pp. 25–30.
- [24] P. Heydari, "Analysis of the PLL jitter due to power/ground and substrate noise," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 12, pp. 2404–2416, Dec. 2004.
- [25] P. Heydari and M. Pedram, "Analysis of jitter due to power-supply noise in phase-locked loops," in *Proc. IEEE Custom Integr. Circuit Conf.*, May 2000, pp. 20.3.1–20.3.4.
- [26] SpectreRF Simulation Option, Cadence Design Systems Inc. [Online]. Available: <http://www.cadence.com>
- [27] K. Kundert, Predicting the phase noise and jitter of PLL-based frequency synthesizers [Online]. Available: <http://www.designers-guide.org>
- [28] K. Kundert, Modeling jitter in PLL-based frequency synthesizers [Online]. Available: <http://www.designers-guide.org>
- [29] Affirma Verilog-A Language Reference, Cadence Design Systems Inc., May 2001 [Online]. Available: <http://www.cadence.com>
- [30] S. D. Vamvakos, V. Stojanović, and B. Nikolić, "Discrete-time cyclostationary phase-locked loop model for jitter analysis," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2009, pp. 637–640.
- [31] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms and Applications*, 2nd ed. New York: Macmillan, 1992, ch. 10.
- [32] S. D. Vamvakos, "Analysis, measurement and optimization of jitter in phase-locked loops," Ph.D. dissertation, Univ. California, Berkeley, CA, 2005.
- [33] A. Leon-Garcia, *Probability and Random Processes for Electrical Engineering*, 2nd ed. Reading, MA: Addison-Wesley, 1994, p. 409.



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