On-Chip Spur and Phase Noise Cancellation Techniques

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***Abstract*—Two techniques for spur and phase noise cancellation have been proposed. A fully integrated design achieves a measured spur cancellation of 15dB at 250MHz and 750MHz offset as well as phase noise cancellation from 4MHz to 200MHz offset with maximum 25dB cancellation depth for a 1-GHz clock. The proposed ideas have been verified through a fabricated 65nm CMOS prototype with power consumption of 11mW from a supply voltage of 1.2V.**

***Index Terms*—Spur, phase noise, cancellation, notches, and delay-line discriminator.**

I. Introduction

Spur and phase noise are two of the most critical specifications that can ultimately limit the performance of communication system. For example, spurs resulting from device mismatches in the LO generation circuit could cause a transmitter to fail its spectral mask requirement. On the receiver side, blocker induced reciprocal mixing of phase noise is the ultimate sensitivity limit, even for a perfectly linear receive chain. As a result, we tend to spare more power budget on clock sources to meet the worse case corners and scenarios, which might, in fact, rarely happen. Therefore, it would be beneficial to have a post-process module cascaded after the clock source and turned active only when needed. Our goals are to generate notches against far-out spurs, and to produce high-pass filtering on the phase noise of the clock to suppress close-in phase noise, as conceptually shown in Fig. 1. In this way, we can relax the specifications of the clock source and achieve lower power design to potentially extend battery life considerably.

II. Proposed Idea

A. Spur Cancellation

To simplify illustrations, we can first consider a special case that a clock has spurs with offset frequency of half carrier frequency, as shown in Fig. 2. The spurs affect the clock by fluctuating clock edges periodically. Thus, if we can delay this clock by half of the jitter period (i.e. one clock period in this case), and interpolate it with the original clock, then the periodic jitter can be cancelled out. Such an operation in the time domain is an average on the past and present phase, which can be described in frequency domain as

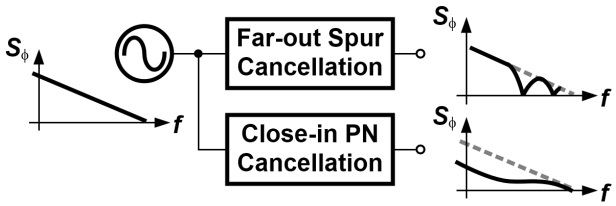

Fig. 1. Spur and phase noise cancellation goals.

$$|\Phi_{\text{out}}(s)| = \frac{|\Phi_{\text{in}}(s)\cdot(1+e^{-sT})|}{2} = |\Phi_{\text{in}}(s)|\cdot|\cos \pi f T| \quad (1)$$

, where $\Phi_{in}(s)$ is input phase noise and T is the delay time. We notice that this transfer function create notches at the offset frequencies of $1/2T$, $3/2T$…, etc. By programming the time delay, we can line up the notch frequencies on top of the spurs to reject them. Note that such rejection not only applies to spurs, but also applies to phase noise.

Although it is possible to push the notches into low offset frequency with large delay, for close-in phase noise cancellation, the notch bandwidth (which is proportional to $1/T$) shrinks and therefore has little impact on the integrated phase noise. In addition, the noise accumulated by the long delay line also limits the notch depth. Nevertheless, it is still effective for far-out spurs that only require short delay. The issues above can be circumvented if we can change $1+e^{-sT}$ into $1-e^{-sT}$. In this way, the transfer function becomes $|\sin \pi f T|$, which has its first notch locating at dc and is more suitable for close-in phase noise cancellation. To realize such a transfer function, we will introduce a delay line discriminator method in next section.

B. Phase Noise Cancellation

In order to perform phase noise cancellation, the first step is to extract the phase noise information from the clock source, and then apply it back to the original clock with opposite polarity [1]. The delay line discriminator is a good candidate to serve this function and is used widely in spectrum analyzers with high sensitivity for phase noise measurement [2]. When a clock, $\cos(\omega t+\phi_{\text{in}}(t))$, passes through a delay line of delay T_1, a frequency dependent phase shift is then applied on its spectrum. By comparing the phase difference between the two ends of delay line,

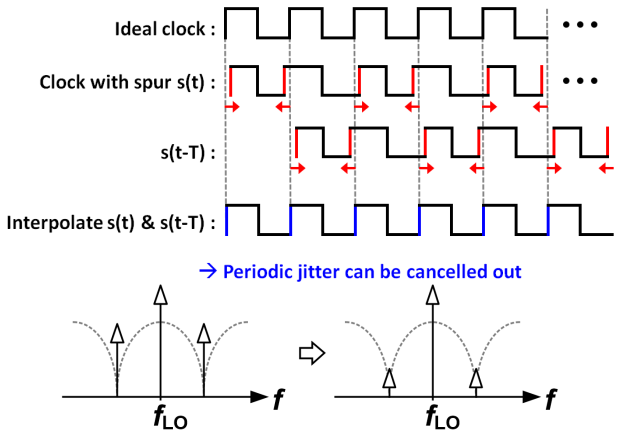

Fig. 2. Delay-and-interpolate spur cancellation technique.

the resulting signal at the output of the phase detector (PD) is given by

$$\Delta\Phi_{PD}(s) = \Phi_{in}(s)\cdot(1-e^{-sT_1}) \cong \Phi_{in}(s)\cdot sT_1. \quad (2)$$

This signal is a differentiated version of input phase information and is down-converted into baseband. We can then recover such a signal by an integrator and then feed-forward it to modulate a voltage control delay line (VCDL) where the same clock is passing through. In this way, the baseband phase noise information can be up-converted back to the clock frequency to cancel out the original phase noise. The operations above can be realized in a simplified circuit shown in Fig. 3(a), which incorporates a VCDL and a PD for phase comparison, a charge pump (CP), a capacitor as an integrator, and another VCDL at output for phase noise cancellation. In this circuit, the output phase noise can be expressed as

$$|\Phi_{out}(s)| \cong \left|-\Phi_{in}(s)\cdot sT_1\cdot\frac{K_P K_D}{sC}+\Phi_{in}(s)\cdot e^{-sT_2}\right| \quad (3)$$

, where K_P, T_2, and K_D are the gain of PD/CP, the delay of $VCDL_2$, and the gain of $VCDL_2$, respectively. When the cancellation condition is met (i.e. $T_1K_PK_D/C = 1$), it can be further reduced to

$$|\Phi_{out}(s)| \cong |\Phi_{in}(s)\cdot(1-e^{-sT_2})| = |\Phi_{in}(s)|\cdot|2\sin\pi fT_2|. \quad (4)$$

In this way, the close-in phase noise can be cancelled out largely by the high-pass filtering on original phase noise. Note that, although (2) and (4) have the same form, they are totally different, since the signal in (2) is at the baseband, whereas the signal in (4) is at clock frequency.

III. Non-ideality Considerations

Although the result in (4) looks promising theoretically, there are some possible issues in circuit realization. Therefore, it is worthwhile to analyse how they impact the performance and how to work around them.

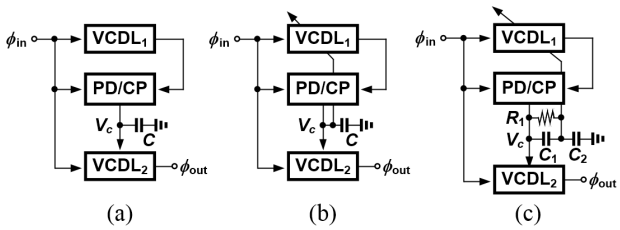

Fig. 3. Evolutions of phase noise cancellation architecture: (a) basic design (b) with DLL to avoid V_C from saturating, and (c) using series C_1 and C_2 to break the trade-off on loop capacitance value selection.

A. Mismatch

First, since we perform the cancellation in the analog domain, the cancellation depends on the device matching and would be limited by mismatches and variations over PVT. Fortunately, for >20dB cancellation depth (Fig. 4), the mismatch only needs to be controlled within 10%, which is not difficult to achieve with careful design and layout. Furthermore, calibration knobs can be added, if needed, to track over PVT.

B. DC Balancing Loop

Second, due to the nature of integrator, any small constant phase offset will finally pump the control voltage (V_C) into saturation. Since we already have PD, CP, and VCDL, we can mitigate this issue by looping them into a delay-locked loop (DLL), as shown in Fig. 3(b), such that V_C would settle to a proper voltage level by the feedback. Rather than introduce another CP and variable-gain amplifier (VGA) [5] for the dc balancing loop, this sharing method shows zero power and minimum area penalty. It is worth noting that the DLL locks the phases at two ends of the delay line within its bandwidth, which in turn wipes out low frequency phase information and makes the phase noise cancellation at low offset frequency malfunction, as

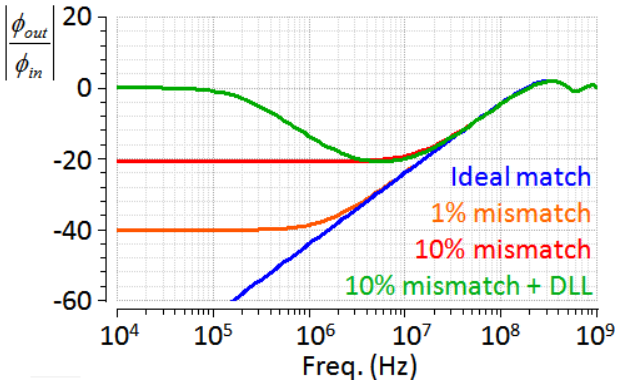

Fig.4. Non-ideal effects on phase noise cancellation.

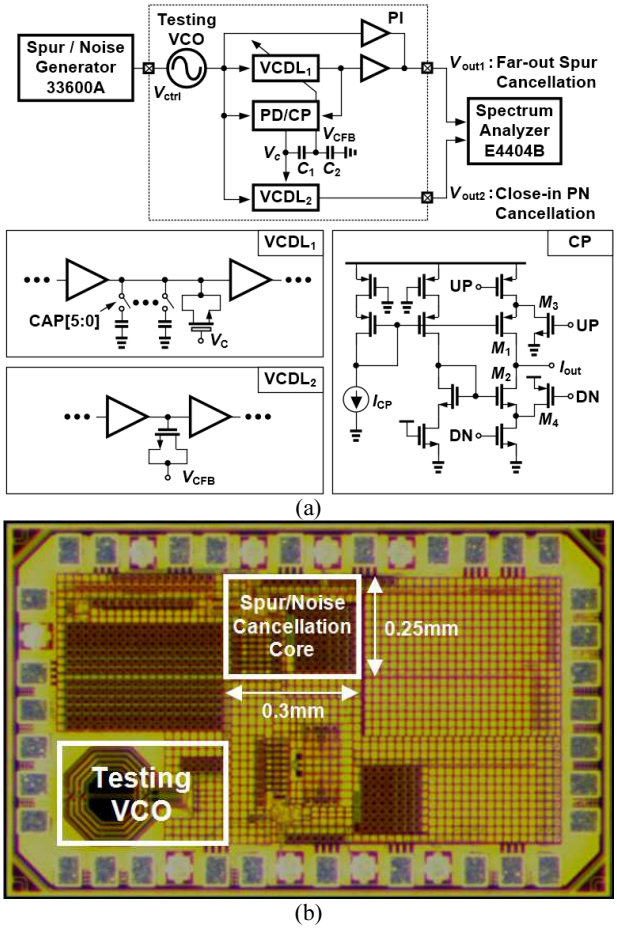

Fig.5. (a) Overall architecture and testing setup. (b) Test chip die photo.

can be shown by the green curve in Fig. 4. Such an impact might be less critical within a PLL, where the close-in phase noise will be cleaned by the phase noise of external reference clock. Nevertheless, we still prefer to keep the DLL bandwidth as small as possible in this design.

IV. Circuit Implementation

According to the analysis above, we have to meet the cancellation condition and to keep low DLL bandwidth simultaneously. However, it would lead to a trade-off on capacitance value. To break this trade-off, we proposed a new loop filter composed of series capacitors C_1 and C_2, shown in Fig 3(c). In this way, the DLL loop sees a large C_2 to achieve small bandwidth, and the feed forward path sees a capacitance of $C_1C_2/(C_1+C_2)$ that can still meet the cancellation conditions by this extra freedom. Also, in order to define the dc voltage and compensate any possible leakage with minimum effect on the transfer function, a tuneable large resistor R_1 (from 100k to 1MΩ) is connected in shunt with C_1.

The final architecture is shown in Fig. 5(a), which combines both spur and phase noise cancellation techniques with a shared delay line. The phase interpolator (PI) for spur cancellation can be easily implemented by directly shorting the two inverters' outputs that are driven by the clocks to be interpolated, since the DLL has aligned them nominally. Note that in this test chip, the output of the two techniques are separated for testing purpose, and can be implemented in cascade by feeding V_{out1} into the input of VCDL$_2$. The delay line of VCDL$_1$ can cover the delay range from 1.25nsec to 2.75nsec by 6-bit capacitor banks switching and +/−70psec by varactor tuning. To minimize possible leakage on the internal node between C_1 and C_2, we use thick oxide varactor in VCDL$_1$. The resulting low tuning sensitivity is not an issue, since small varactor gain is desired to minimize DLL bandwidth. The output VCDL$_2$ is also made of the inverter chain loaded by normal varactors, but with opposite varactor polarity and much larger tuning gain to achieve cancellation. In addition to DLL bandwidth, the output resistance of CP also limit the cancellation at low offset frequency. Therefore, long channels are selected for the M_1/M_2 in CP to keep high output resistance, and M_3/M_4 are added to help driving the extra capacitance loading (Fig. 5(a)).

V. Experimental Result

This chip has been fabricated in 65nm CMOS technology, which occupies 0.3×0.25mm^2 core area (Fig. 5(b)). The circuit consumes a total power of 11mW, of which 5mW dissipates in the delay line, 2mW in the PD/CP, and 4mW in the output VCDL. Fig. 5(a) shows the measurement setup. The spur and white noise waveforms are generated externally by 33600A waveform generator and then modulate the control line of a 1-GHz testing voltage-controlled oscillator (VCO) on the chip to mimic a low power VCO with relaxed performance. The

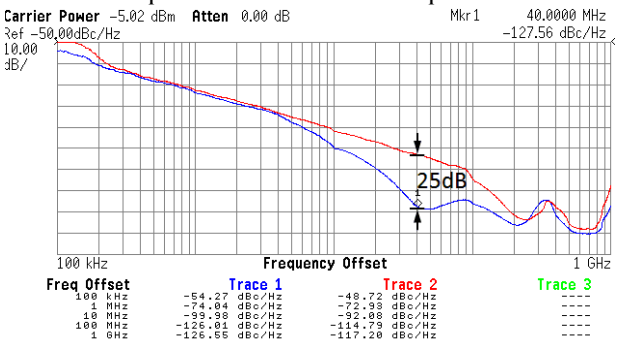

Fig.6. Phase noise is cancelled from 4MHz to 200MHz offset with maximum cancellation of 25dB on a 1-GHz clock.

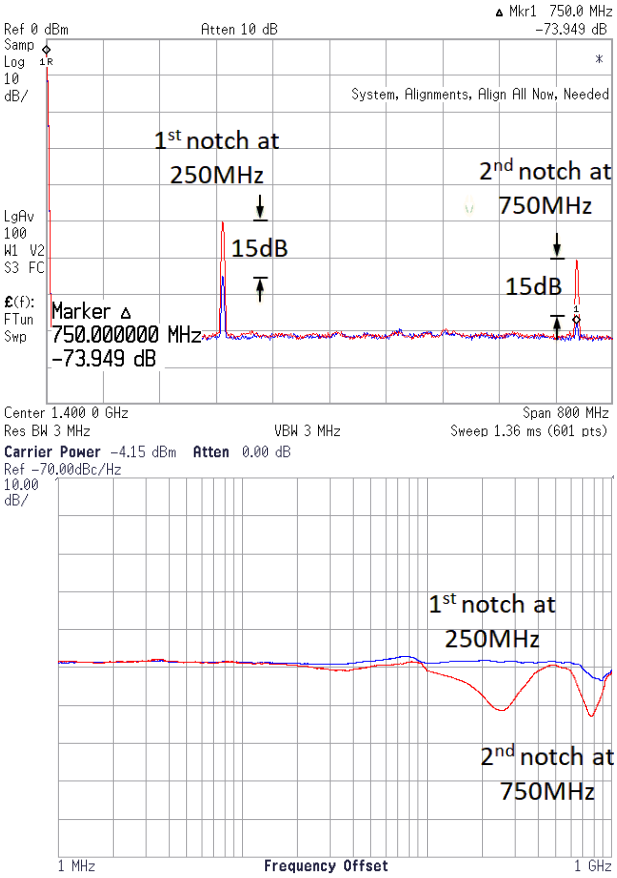

Fig.7. (a) Far-out spurs at 250MHz and 750MHz offset frequencies can be cancelled up to 15dB by the notches. (Blue curve). (b) Far-out noise can also be attenuated by notches. (Red curve).

TABLE I
PERFORMANCE SUMMARY

	TMTT 2015[3]	RFIC 2012[4]	IMS 2016[6]	This work
Frequency	1.5GHz	5GHz	10GHz	1GHz
Delay Line Type	Off-chip FBAR	On-chip inverter	On-chip LC + Off-chip SAW	On-chip inverter
Phase Noise Cancellation BW	1k ~ 2MHz	100k ~ 20MHz	100k ~ 10MHz	4M ~ 200MHz
Max Phase Noise Cancellation Depth	40dB	12.5dB	15.5dB	25dB
Far-out Spur Cancellation	N/A	N/A	N/A	15dB
Power Consumption (excluding VCO)	340mW	20.9mW	102mW	11mW
Core Area	1.8×1.2 mm²	0.38×0.32 mm²	1.68×1.5 mm²	0.3×0.25 mm²
Technology	130nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS

phase noise cancellation with delay-line-discriminator method is demonstrated in Fig. 6. The cancellation applies from 4MHz to 200MHz offset frequency and achieves a maximum of 25dB cancellation at 40MHz offset frequency. On the other hand, the delay-and-interpolate method for spur cancellation is also verified. Fig. 7(a) shows the results of spur cancellation. In this design, the delay line is set to be 2nsec, which generates notches at 250MHz (1/2T) and 750MHz (3/2T) offset frequency. The spurs at those two offset frequencies can be rejected by 15dB (from -56 to -71dBc). Such rejections also apply to phase noise. To felicitate the observation at high offset frequencies, we use external clock with broadband noise as testing clock instead of on-chip VCO. As shown in Fig. 7(b), two notches at 250MHz and 750MHz are clearly shown on phase noise plot after applying the technique. Table I summarizes and compares our work with recent publications.

VI. CONCLUSION

Two novel techniques to generate transfer functions of $|\cos \pi fT|$ and $|\sin \pi fT|$ for spur and phase noise cancellation has been proposed and verified in the test chip. For spur cancellation, the delay-and-interpolate technique can generate notches that are able to reduce the spur level by 15dB. For phase noise cancellation, a delay-line-discriminator and feed-forward technique can cancel the phase noise on the offset frequency from 4MHz to 200MHz with maximum cancellation depth of 25dB. This cancellation module can be cascaded after the clock source targeted for low power with relax the specifications and turned active only when high performance scenarios occur, allowing extended battery life by optimum power and performance trade-off management .

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