A Low-Voltage Low-Offset Dual Strong-Arm Latch Comparator

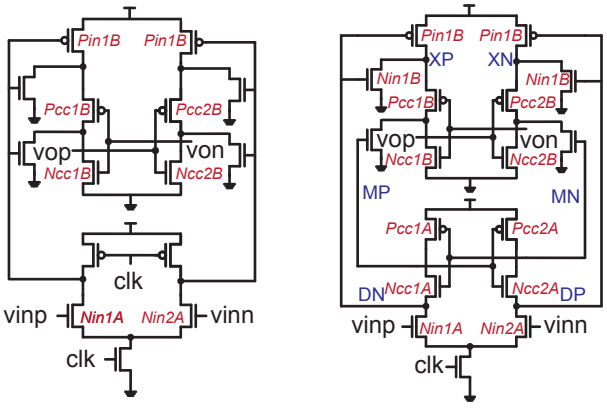
Aikaterini Papadopoulou, Vladimir Milovanović† and Borivoje Nikolić
University of California at Berkeley, CA
†now with University of Kragujevac, Serbia
Email: katerina@eecs.berkeley.edu

***Abstract*—A dual strong-arm (DSA) comparator is designed targeting at low-voltage operation in deeply-scaled technologies. The addition of a second regenerative latch helps reduce both offset sensitivity and offset while maintaining comparable or better performance as a conventional double-tail latch across a wide range of voltages. A large comparator offset measurement array is fabricated in a 28nm FDSOI process. The DSA offset is measured to be 8.5mV across 6 dies, approximately 30% lower than the conventional topology at iso-area and iso-capacitance conditions. It is also shown to scale well with supply and common-mode voltage, achieving up to 65% lower offset across the voltage range.**

I. Introduction

A high-speed, low-offset, and low-power comparator is a very versatile circuit, used in many applications such as analog-to-digital conversion, memory sensing circuits and data receivers. Voltage-mode comparators are particularly popular due to their zero static power consumption and rail-to-rail output.

One of the most common comparator designs is the strong-arm (SA) latch comparator [1] [2]. Although a low-power and robust circuit, the SA comparator is not necessarily the most appropriate choice for low-voltage operation due to increased mismatch in scaled technology nodes. Various techniques have been proposed, such as offset compensation or SA redundancy [3] [4], but those introduce additional design complexity and often require multiple clock phases. Two-stage comparator topologies, the state-of-the-art of which is shown in Figure 1a, generally combine an integrating first-stage and a regenerating second stage, and have been shown to be more appropriate for low-voltage operation, maintaining lower offset and larger design flexibility [5]–[7].



(a) Double-tail sense amp (DTSA) [5] (b) Dual strong-arm (DSA)

Fig. 1. Conventional and proposed 2-stage comparator topologies. Precharge devices not shown.

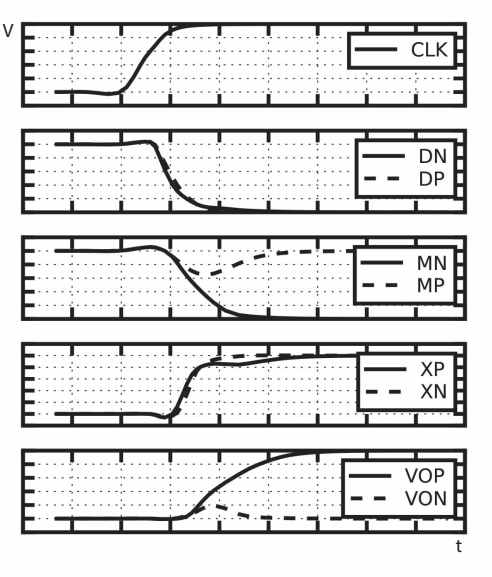
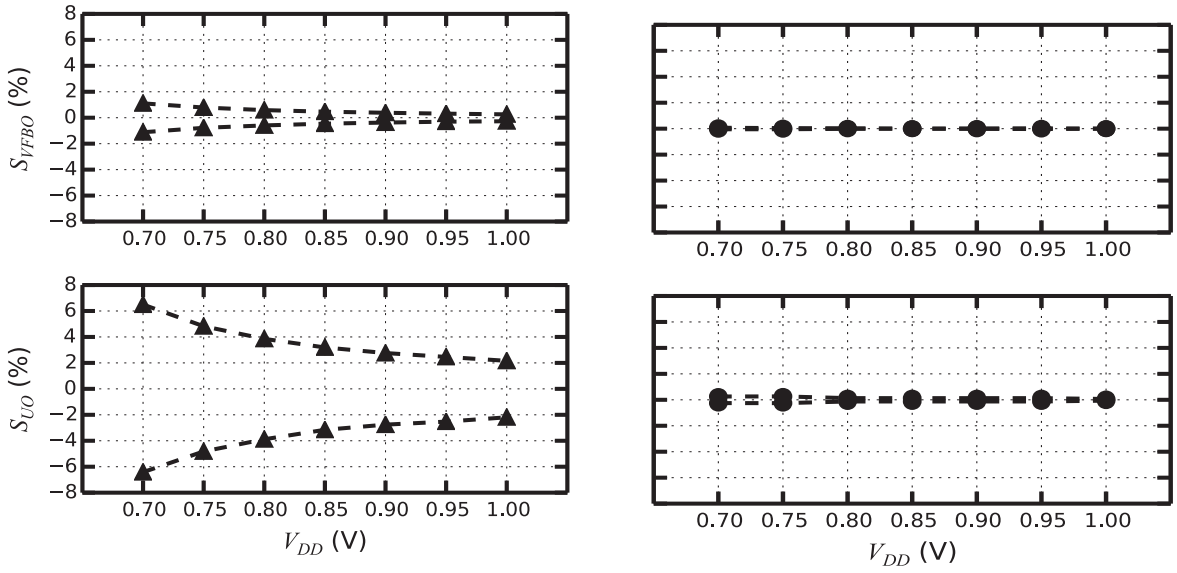


Fig. 2. Timing diagrams of the DSA comparator.

In this work, we present a dual strong-arm two-stage comparator topology, designed to desensitize offset from device variations, and demonstrating exceptional scaling with voltage.

II. Dual Strong-Arm comparator

The schematic of the DSA is shown in Figure 1b. The timing diagrams of the comparator for an input voltage difference of $\Delta V_{in} = 50$mV are shown in Figure 2. During the reset phase when CLK=0, the precharge devices charge nodes DN, DP and MN, MP to V_{DD} and therefore nodes XP, XN and VOP, VON are discharged to ground. During the amplification stage, when CLK becomes 1, the timing difference between nodes DN,DP and MN,MP enables the first stage to integrate the input while MN,MP hold the second latch in the precharged state, allowing it to see the larger signal and therefore reducing the impact of offset. When the second stage starts integrating, gain is provided through the input pair Nin1A, Nin2A as well as through the inverter pairs (Nin1B, Pin1B) and (Nin2B,



(a) DTSA

(b) DSA

Fig. 3. Comparison of simulated offset sensitivities to model parameters of device pairs (Pcc1B, Pcc2B) for two comparator topologies. The selected (Pcc1B, Pcc2B) is the most sensitive device pair of DTSA.

Pin2B) of the second stage. As soon as the voltage difference between the gate and source of Ncc1/2A or Pcc1/2B becomes larger than a V_{TH}, the corresponding latch quickly regenerates and the output is evaluated.

The comparator essentially consists of two regenerative latches, resulting in lower offset, based on the observation that the joint error probability of two half-sized sense amplifiers is lower than that of a unit-sized sense amplifier [8]. This allows for smaller individual devices to be used which desensitizes the offset from device variations, especially current variations. Furthermore, the input of the second regenerative latch is an integrated version of the comparator differential input, and it provides additional gain therefore reducing the offset contributions of device pairs in the second stage.

Offset sensitivity of a comparator is defined with respect to each comparator device as $S_{p_i} = \partial V_{offset}/\partial p_i$, where i indicates each statistical parameter of the model. The derivative is approximated using finite differences in simulation. Figure 3 shows the simulated offset sensitivity for device pair (Pcc1B, Pcc2B) for both the DTSA and the DSA comparators. All device lengths are minimum size and total active device width is $14.26\mu m$ for each latch. The comparators are sized to deliver approximately equal speed for an input voltage difference $\Delta V_{in} = 25$mV at nominal supply. Input capacitance and load capacitance are kept the same for the two cases, in order to enable fair comparison of speed at various supplies. The tail device has been determined to significantly affect offset as it determines the current through the first stage, and unequal sizing can skew the results. Therefore, it is also kept equal in

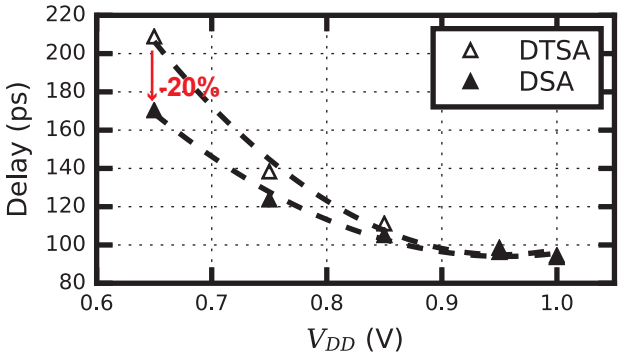


Fig. 4. Simulated delay scaling across supply voltage and least-square best-fit lines (dashed) for equal fanout DTSA and DSA.

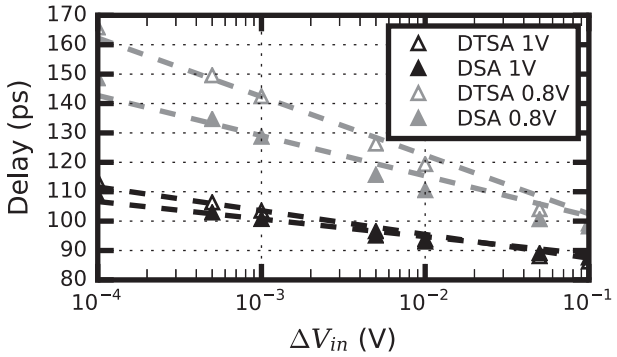


Fig. 5. Simulated delay across input voltage difference and least-square best-fit lines (dashed) for equal fanout DTSA and DSA.

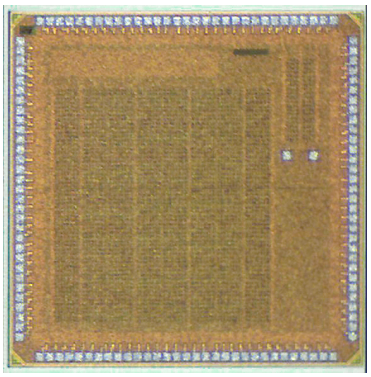


Fig. 6. Die photo of the chip.

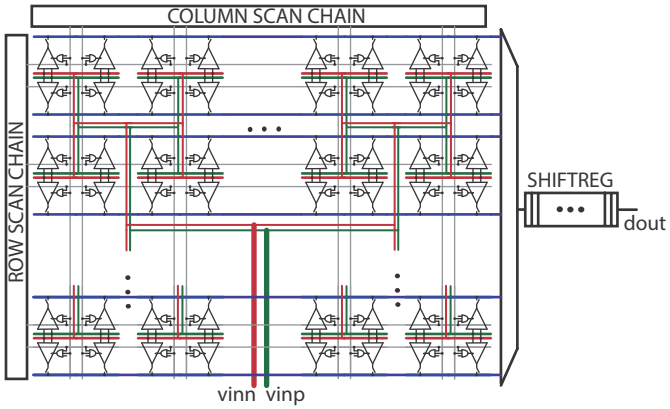
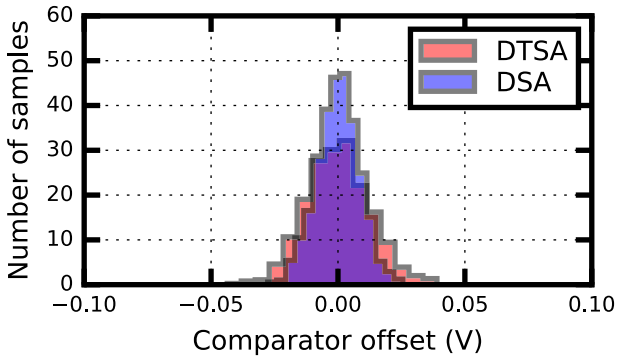


Fig. 7. Detailed block diagram of the comparator array, scan chains and output shift register.



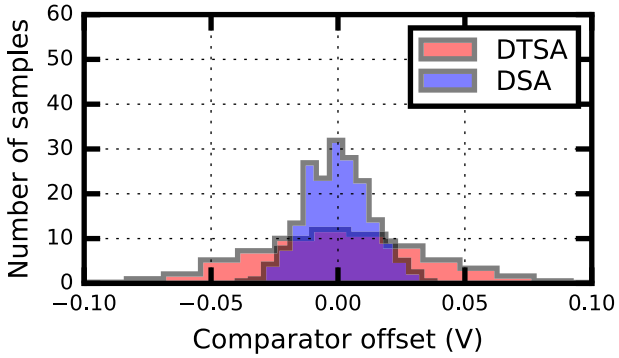


Fig. 8. Measured offset of DTSA and DSA for $V_{DD} = 1V$ (top) and $V_{DD} = 0.7V$ (bottom).

both cases. While the DTSA exhibits increased sensitivity to current variations as supply is scaling, ranging from 2.2% to 6.5 %, the DSA comparator maintains a low sensitivity ranging from 0.06% to 0.25%. Sensitivity improvement is achieved in all corresponding device pairs, but only the DTSA worst-case pair is shown in order to illustrate the improvement.

Figure 4 compares the two types of comparators in terms of speed. The DSA is shown to scale much better with supply voltage, maintaining a delay $\sim 20\%$ smaller that the DTSA at $V_{DD} = 0.65$V. Figure 5 shows a nominal simulation of the delay with respect to the input voltage difference ΔV_{in} at nominal and at scaled supply. The performance of the DSA is comparable or better than the DTSA for input differences that are smaller that 25mV, and its advantage becomes more pronounced at the scaled supply voltage.

III. Silicon Measurement Results

A large array of comparators was fabricated in a 28nm FDSOI process. The die photo is shown in Figure 6 and chip details are outlined in [9]. Figure 7 shows a detailed block diagram of the chip. A total of 224 comparators per die were fabricated for each comparator design. Comparator sizing follows the rules presented in Section II to ensure fair comparison, and layout was carefully performed to avoid systematic effects that can affect the measurements. The comparators are arranged in an array addressed by scan chains, with shared inputs. The input and buffered clock buses are delivered to each comparator through an H-tree in order to eliminate systematic offsets. The outputs are then multiplexed out to a 30kbit shift register. The design overall allows for a large sample size to be tested using a limited number of pads, while noise averaging and fast testing is possible through the use of the output shift register.

A slow ramp is applied at the input by using a programmable high-precision Keithley 2612A voltage source. The resolution of the input is set to 2μV and the swing is limited to 100mV to reduce the number of measurements. The source, all digital signals and the clock are controlled by the FPGA. The digital output of the shift register is read out and noise is averaged over the 30000 samples. A total of 1344 comparators across 6 dies were measured for each design. A measurement is assumed to fail when more than 10% of the measured samples are outside the input range.

Figure 8 shows the histogram distributions of the measured offsets at nominal and scaled supply, across all 6 dies. The measured standard deviation of the offset at nominal supply for the DSA is 8.5mV comparing to 12.7mV for the DTSA, a 33% improvement. The improvement is even more dramatic at $V_{DD} = 0.7$V, where the measured offsets for the DSA and DTSA are 13.1mV and 34.9mV, respectively, showing a 62.5% lower offset for the DSA. Figure 9 shows the measured offsets across supply voltage for a single die, in order to visualize the scaling advantage of the proposed topology. At $V_{DD} = 0.65$V

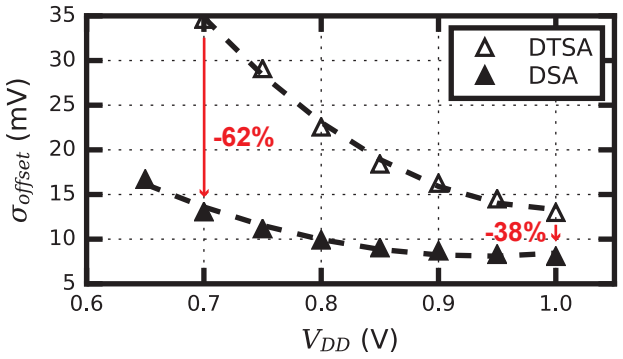


Fig. 9. Measured offset standard deviation across supply voltage for a single die.

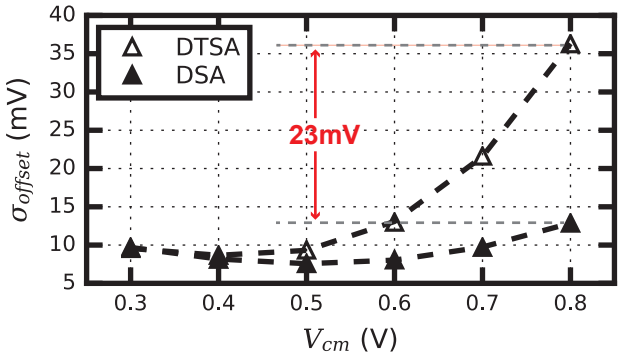


Fig. 10. Measured offset standard deviation across input common-mode for a single die.

the DTSA fails.

Figure 10 examines the operation of the two latches for various common mode voltages. Across the voltage range the offset of the DSA varies only by 5.3mV, in comparison with the DTSA offset which varies by 27.3mV. In addition, the offset of the DSA remains low at high input common-mode voltages, making it more appropriate for applications like memory. At the highest common-mode measured, the DSA has 23mV lower offset than the DTSA.

Figure 11 shows the spread of the measured standard deviation of the offset across all measured dies, showing that the DSA varies a lot less across dies. The contributors of random mismatch do not change from die to die, but systematic variation can cause, for example, all device lengths to be a little different in a different die, which in turn affects the device mismatch through the Pelgrom equation. The standard deviation of the offset for the DSA varies by < 1mV, showing exceptional tolerance to variations because of its reduced sensitivity to them.

IV. Conclusion

A dual strong-arm sense amplifier is presented as a variation-tolerant low-offset comparator for low-voltage applications. The comparator has reduced offset sensitivity to device variations, outperforms conventional topologies and is shown to scale well with supply voltage. Measurements in a 28nm FDSOI technology reveal a very low offset of 8.5mV at nominal supply voltage, which varies only by 7.5mV across supply and 5.3mV across common-mode voltage.

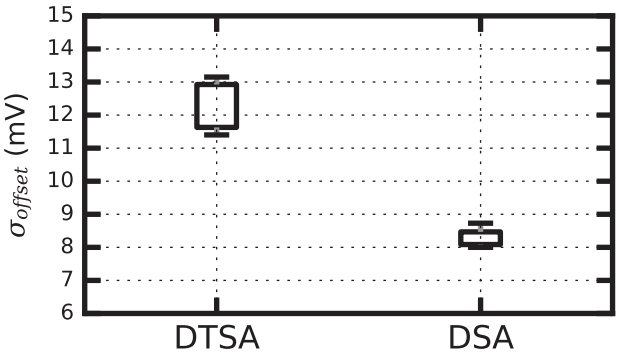


Fig. 11. Spread of the measured standard deviation of the offset across all dies for each comparator type.

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