A 65nm CMOS Transceiver with Integrated Active Cancellation Supporting FDD from 1GHz to 1.8GHz at +12.6dBm TX Power Leakage

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Abstract

This paper presents an active transmitter (TX) cancellation scheme for FDD that synthesizes a replica of the TX current in shunt with the receiver (RX), virtually shorting out the TX signal for the RX while having minimal impact on TX insertion loss. The prototype in 65nm CMOS demonstrates >50dB cancellation of a +12.6dBm peak 20MHz modulated TX signal. A receiver integrated on the same prototype is able to down-convert the RX signal at 40MHz offset with <4.3dB noise figure (NF) degradation in the presence of the residual TX.

Introduction

Continuing growth in wireless connectivity has resulted in a proliferation of frequency bands that use frequency-division duplexing (FDD), requiring a large number of bulky and expensive off-chip duplexers. Analog subtraction of the transmit (TX) signal at the receive (RX) port [1-4] has been explored as an alternative for integration. However, the maximum cancelled leakage power has been limited to <+2dBm; accordingly, such systems still require 30dB of TX-RX isolation from off-chip filters. Furthermore, many cancellation schemes passively couple a portion of the TX signal into the RX to perform cancellation, degrading TX efficiency. Matching the time-varying, frequency selective TX-RX leakage channel over a wide TX bandwidth presents another challenge for electronic subtraction systems.

This paper presents a fully integrated transceiver with a single antenna interface providing >50dB of isolation for 20MHz modulated TX signal from 1.0-1.8GHz up to +12.6dBm. This is accomplished by connecting the antenna to the TX and RX via a series stacked transformer (Fig. 1.1). An RF current DAC is placed in shunt with the RX input, cancelling the TX current and creating a virtual ground across the RX for the TX signal (Fig. 1.2). The virtual ground shields the TX from RX port loading, preserving high TX efficiency. As the TX is designed with low output impedance, and the DAC has high output impedance relative to the RX, the RX signal experiences minimal loss (Fig 1.3). In order to track nonlinearity and time variance in the leakage signal over wide bandwidth, the DAC is driven with a digitally processed version of the TX data (Fig. 9).

Circuit Implementation

The chip top level (Fig. 2) includes an integrated TX, RX chain, cancellation current-steering DAC, and the TX/RX matching networks. The TX (Fig. 3.4) is a 500MS/s, 8-bit switched-capacitor power amplifier, [5-6] which provides a low, amplitude-independent output impedance to minimize RX insertion loss and amplitude-dependent TX/RX mixing products. A 25% duty cycle I/Q cell-sharing architecture [5], in which the TX unit cells are time-interleaved between I and Q phases, is used to maximize I/Q combination efficiency. This is implemented through data-dependent NAND gates (Fig. 3.1), which drive each unit cell in one of the ±I, ±Q, or ±I±Q phases. The maximum measured TX output power is +18.8dBm at 1.2GHz.

The 10-bit 500MS/s RF current DAC is segmented with 5 thermometer and 5 binary bits. It is important to note that the DAC cancels the TX signal in the current domain, rather than the power domain, substantially lowering its power consumption relative to the TX. The DAC can cancel up to 20dBm TX power, using an RX transformer with 2:1 turns ratio and a full-scale current of 60mA from a 1V supply. A single balanced current-switching DAC is used (Fig. 3.3), with Class-A operation for good dynamic linearity. DAC and TX phase noise skirts can fall in the RX band and desensitize the RX. However, phase noise correlated between DAC and TX LOs is cancelled [4]. Accordingly, the DAC is implemented in a Cartesian architecture with similar 25% duty-cycle I/Q cell sharing as the PA. This allows sharing of DAC and TX LO paths, to maximize correlation and minimize RX noise figure (NF) degradation.

In order to characterize the proposed cancellation architecture in a realistic environment, a receiver is realized on the same die. To enable multi-mode broadband testing, the receiver was designed for maximal linearity and re-configurability over NF performance. The RX is comprised of a low-noise trans-conductance amplifier (LNTA) (Fig. 3.2), current-mode passive mixers, and baseband trans-impedance amplifiers with programmable first-order filtering. The measured RX performance is summarized in Fig. 8. The chip, shown in Fig. 12, was designed in TSMC65nm process and measures 2.5mm x 2.5mm.

Measurement Results

Single tone cancellation is measured over TX output power ranging from -21.7dBm to +12.6dBm (Fig. 5), and varying TX center frequency from 1GHz to 1.8GHz at fixed 0dBm TX power (Fig. 6). In all cases, the post-cancellation residual TX is limited by the DAC LSB current and is independent of TX power. A cancellation of >50dB is achieved at a maximum TX output power of +12.6dBm, an order of magnitude higher power over the state of the art [1].

An off-chip adaptive digital filter on the DAC data (Fig. 4) is used to track the frequency-selective TX-RX leakage channel for modulated TX signals (Fig. 7). Over 50dB of isolation is achieved for a 20MHz modulated bandwidth TX signal with average power 6.6dBm and 6dB peak to average power ratio, a >20dB improvement over prior work [2,3].

Antenna load was varied to create a VSWR from 1:1 to 5:1 (Fig. 6). By adapting the filter coefficients, the residual leakage remains flat and is limited by DAC LSB over the entire range. The tested impedance region represents the measurement set up, rather than any cancellation limitations.

The RX NF degradation is measured as a function of TX output power for a TX-RX center frequency spacing of 40MHz (Fig. 10). For low TX power (below -5dBm), the NF is dominated by RX noise. For high TX power, the NF is dominated by *uncorrelated* phase noise between the TX and DAC. Cancellation of correlated phase noise by sharing a common TX/DAC LO path is measured at 19dB at 40MHz duplex offset through injection of spurs and white

noise into the shared LO input port (Fig. 11).

When cancellation is enabled, the NF is improved by over 15dB, demonstrating the proposed scheme's ability to cancel the TX's RX-band noise. The RX NF is degraded by 1.1dB at the highest previously reported TX output power of +2dBm, and by 4.3dB at +10.6dBm.

Note that while the nominal RX NF is 7.6dB, 2.9dB is due to matching network loss (Fig. 8). Improvement of the matching network would leave NF degradation (Fig. 10) unchanged, as it is independent of this loss.

Acknowledgements

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References

[1] J. Zhou et al, ISSCC, 2014. [2] J. Zhou et al, ISSCC, 2015. [3] D.-J. van den Broek et al, ISSCC, 2015. [4] D.-J. van den Broek et al, RFIC, 2015. [5] H. Jin et al, ISSCC, 2015. [6] S.-M. Yoo et al, JSSC, 2011.

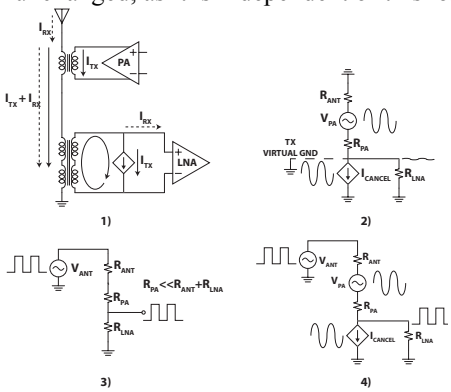

Fig. 1 (1) Proposed interface (2) TX equivalent (3) RX equivalent (4) Simultaneous operation of RX/TX

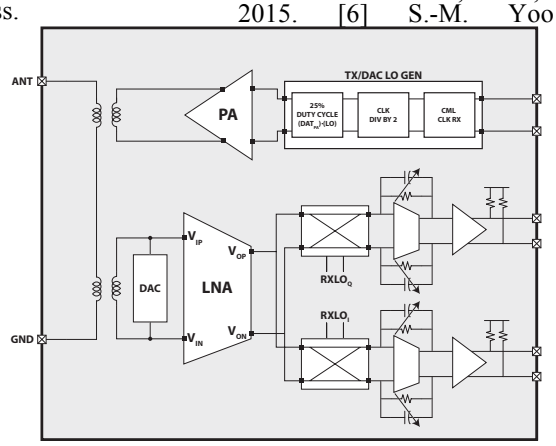

Fig. 2 Top level transceiver schematic

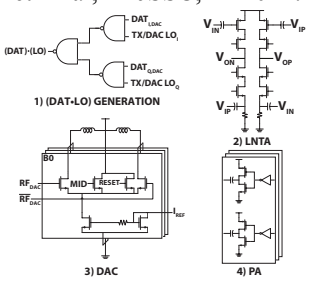

Fig. 3 Block schematics

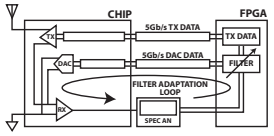

Fig. 4 Test setup

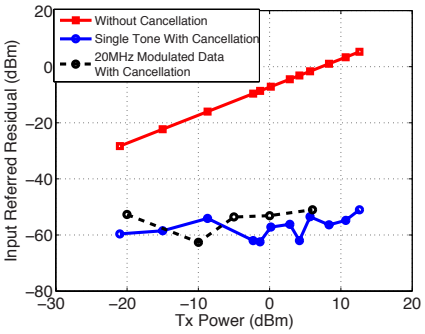

Fig. 5 TX signal at RX input

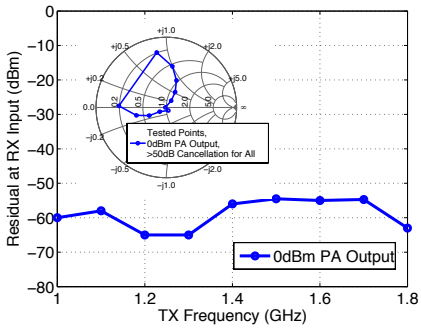

Fig 6. Residual vs. frequency and load

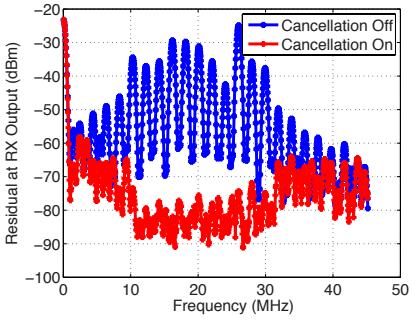

Fig. 7 RX output in TX band, 20MHz TX

Gain (dB)	6-18
Baseband BW (MHz)	15-140
RF 3dB BW (MHz)	800
(OOB) IIP3 (dBm)	10.2
NF, No Matching Network	4.7dB
Matching Network Loss	2.9dB

Fig. 8 RX performance summary

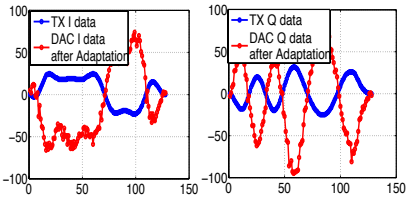

Fig. 9 TX and DAC after adaptation

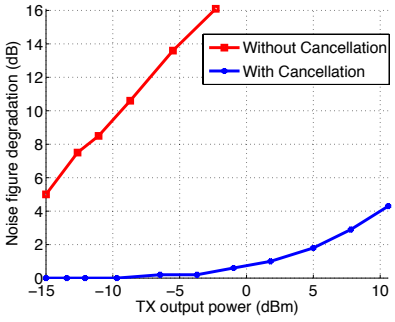

Fig. 10 NF degradation vs. TX power

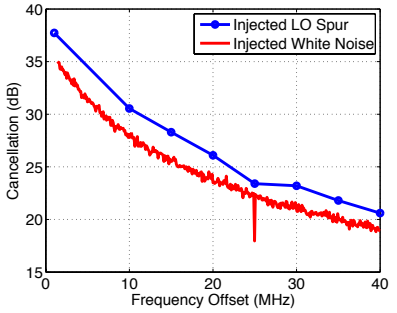

Fig. 11 Phase noise cancellation

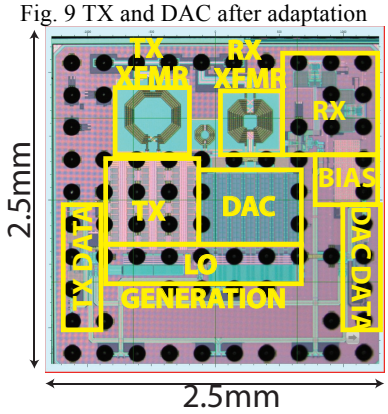

Fig. 12 Die photo

	This Work	[1]	[2]	[3]
Technology	**65nm**	65nm	65nm	65nm
Frequency (GHz)	**1.0-1.8**	.3-1.7	.8-1.4	.15-3.5
Max TX Power Leakage (dBm)	**+12.6**	+2	-4	+1.5
Cancellation at Max TX Power (dB)	**>50**	>30	33	>27
Cancellation 20MHz Modulated Data (dB)	**>50**	-	20	27
Receive Noise Figure (dB)	**7.6**	4.2	7.5[1]	6.3
NF Degradation, +2dBm TX, 40MHz Offset (dB)	**1.1**	.8[2]	.9[3]	4[4]
RX Power (mW)	**40**	74.6-83.0	63-69	23-56
Single Antenna, No External Isolation	**Yes**	No	No	No
Fully-Integrated TX+RX	**Yes**	No	No	Yes[5]
Canceller Power (mW)	**60**	13-72	44-182	Unreported
Active Area (mm^2)	**3.9**	1.2	4.8	2

1)Includes 2.7dB LC duplexer loss 2)TX power unreported(<+2dBm), 100MHz offset 3)TX power unreported(<-4dBm) 4)Full duplex 5)Unknown if measured with on-chip TX

Fig. 13 Comparison table