

# A Fast, Flexible, Positive and Negative Adaptive Body-Bias Generator in 28nm FDSOI

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## Abstract

This work demonstrates a fully-integrated, compact body-bias generator (BBG) with a fine voltage step and sub-100ns response time for use in process and voltage compensation as well as dynamic energy optimization. The generator is implemented in 28nm UTBB FDSOI, using only 1.0V core and 1.8V IO voltage inputs. A modular design enables easy integration into target mobile SoCs, scalable to power domains of any size. The fine resolution (5mV  $V_{th}$ ), 100ns full-scale and 5ns incremental step response, low power (<10 $\mu$ W), and 1.2% area overhead enable fine-grained adaptive body-biasing (ABB). The ability to dynamically track a target frequency within 1% for 200mV of  $V_{CORE}$  change is demonstrated experimentally.

## Introduction

The ultra-thin body and box (UTBB) FDSOI technology features a high sensitivity (>70mV/V) of transistor threshold voltages to body bias. In contrast to adaptive voltage scaling (AVS), enabling adaptive body-bias (ABB) require only two additional power grid lines without substantial consideration of IR drop. The load for body biasing is almost purely capacitive (see Figure 1), with low static current – under 5 $\mu$ A/mm<sup>2</sup> worst case. Optimal body bias can be used for run-time compensation of process, aging, temperature and supply-voltage variations, or to improve energy efficiency [1], but a compact, low power, fast BBG is required. This work implements a fully-integrated switched-capacitor solution that can be integrated on any SoC with low overhead to enable fast, fine-granularity threshold control.

## IP Implementation

Figure 2 shows the two main building blocks of the BBG. The driver unit receives four 1-bit digital commands from the control unit to toggle on or off the charging and discharging of the transistor wells (see Figure 3). The nwell drivers are pMOS and nMOS power switches that provide 0V-1.8V range and high slew rates. Figure 4 shows the pwell negative voltage generation, which is based on a switched-capacitor (SC) charge-pump in contrast to current-source-based solutions in bulk CMOS [2]. The driver implements a 1:-1 SC charge pump with the negative bootstrap circuit for the negative gate drive signal  $G_{bot}$  [3]. The flying capacitor consists of a MOS/MOM stack and occupies the lowest five metal layers to achieve 8fF/ $\mu$ m<sup>2</sup> density at 1.8V. The driver unit design enables simple distribution across large body bias domains for a fast and uniform charging profile.

The control unit integrates a body-bias sensor and decision logic, as well as a digital interface for communication with a power management unit and debug-and-trace registers (see Figure 5). It operates between two main modes: transition or *ON-mode*, and keep-the-value or *STEADY-mode*. In the *ON-mode* body bias sensor is a direct voltage sample-and-compare circuit clocked at 1or 2GHz, thus enabling sub-ns closed loop control over the driver units. A pwell sampler employs a -1:0.8 switched capacitor structure with 20% gain-error to compensate for the lower pMOS body factor. The outputs of the analog upper- and lower-bound rail-to-rail comparators are used to generate exclusive charge or discharge commands. Once the voltages settle inside the bounds, the control unit switches to low-power

*STEADY-mode* and a 0.5MHz clock. The analog reference voltages are generated with a 5-bit two-path resistive DAC implemented using poly resistance only in the slow path and a combination of MOS and poly resistance in the fast path (see Figure 6). This enables 2ns settling of the new upper-bound/lower-bound values and only 400nA of DAC static consumption in *STEADY-mode*. The size of upper-bound/lower-bound window is programmable with a default value of 58mV. When new digital target values are received, or when voltages leak out of the window, the fast clock unit is engaged within a cycle and the control unit switches into *ON-mode* to set new body-bias voltages.

## System Integration and Measurement Results

Both the driver and the control unit occupy the lower five metal layers and are generated as hard macro IP instances with a programmable digital interface for system integration. The body bias generator was embedded in a RISC-V processor SoC, implemented in a 28nm UTBB FDSOI process with LVT transistors. Figure 7 depicts the placement of two drivers and the control unit to supply the total body-bias area of 1mm<sup>2</sup>. Figure 8 shows measurement results of the static levels of pwell and nwell voltage reachable with the BBG IP. The nwell has 58mV resolution which, according to simulation, translates to roughly a 5mV  $V_{th-n}$  step. Similarly,  $V_{th-p}$  achieves 5mV minimal step with a 72mV pwell resolution. Figures 9 and 10 display the dynamics of charging and discharging of the wells. The nwell reaches high slew rates of -80mV/ns and +65mV/ns during discharging and charging, respectively. The pwell voltage ramps down from 0V to -1.3V in 160ns with one driver unit, and in 90ns with two units, switching at 1GHz in both cases. The pwell discharges from -1.4V to 0V in 70ns with only one unit operating. During the *ON-mode* the BBG drives currents in the range of 40-200mA, while in *STEADY-mode* it sources only 3.3 $\mu$ A and 1 $\mu$ A from the 1.8V and 1V supplies respectively. High *ON-mode* currents are averaged over long periods of *STEADY-mode* and contribute less than 2 $\mu$ A in total average current. Figure 11 illustrates the maintenance of target nwell and pwell voltages with short recharge phases when the well voltages drift due to leakage. In this case, under 5ns *ON-mode* recharge of 5ns duration occurs every 1ms and 0.2ms for the nwell and pwell respectively. Figure 12 demonstrates the variation-compensation and energy-efficiency optimization capability of the BBG. On-chip critical path replicas (CPRs) and frequency counters are used to extract the switching frequency which is used to tune the next BB value. The design is able to maintain the target frequency of the CPR within 1% while dynamically changing  $V_{CORE}$  in the range of 760mV-970mV. Note that pwell and nwell may have asymmetric well voltages to achieve robust compensation. Table I compares our solution with other relevant BBG designs and summarizes the performance.

## References

- [1] J. Tschanz, *et al*, *JSSC*, vol. 37, no. 11, pp. 1396–1402, Nov 2002.
- [2] T. Kuroda, *et al*, *JSSC*, vol. 31, no. 11, pp. 1770–1779, Nov 1996.
- [3] Y. Tsukikawa, *et al*, in *VLSI Circuits*, pp.85–86, Jun 1993.
- [4] N. Kamae, *et al*, in *A-SSCC*, pp. 53-56, Nov 2014.
- [5] M. Meijer, *et al*, *Trans. VLSI*, vol. 20, no. 1, pp. 42–51, Jan 2012.
- [6] D. Levacq, *et al*, *JSSC*, vol. 43, no. 11, pp. 2390–2395, Nov 2008.

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TABLE I: Comparison and summary of BBG performances

Metric	This work	Kamae[4]	Meijer[5]	Levacq[6]
Technology	28 FDSOI	65nm bulk	90nm bulk	90nm bulk
BBG Area	0.012mm <sup>2</sup>	0.0052mm <sup>2</sup>	0.03mm <sup>2</sup>	0.006mm <sup>2</sup>
Bias Area	1mm <sup>2</sup>	0.22mm <sup>2</sup>	1mm <sup>2</sup>	0.15mm <sup>2</sup>
Area overhead	<b>1.2%</b>	2.3%	3%	2%
Response time	<b>30/70ns</b>	1.6/2μs	4/5μs	-/70ns
V <sub>th</sub> Resolution	5mV	4mV	2mV	>20mV
BBG Supply	1.0V, 1.8V	0.5V-1.2V	1.2V	2.5V, -1V, 1V
BBG Power	<b>10μW</b>	600μW	177μW	1500μW
V-range: nwell, pwell	[0, 1.8] V, [0, -1.4] V	VDD±0.25V, GND±0.25V	[0.7, 1.2] V / [0, 0.5] V	/ [-0.85, 0.4] V

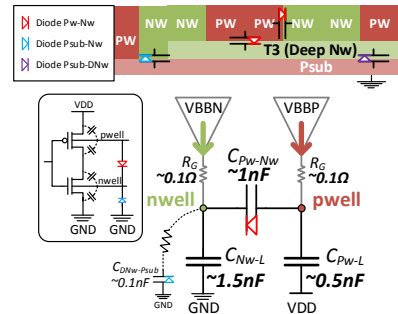


Figure 1. Load model.

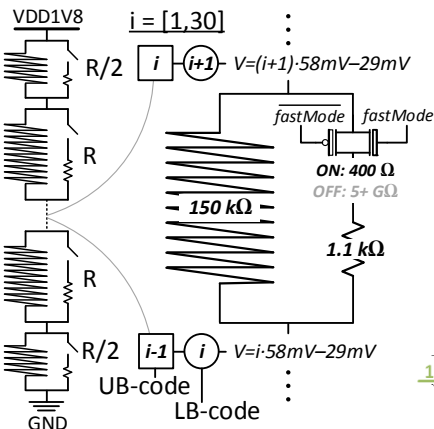


Figure 6. A 5b fast- and slow-path DAC.

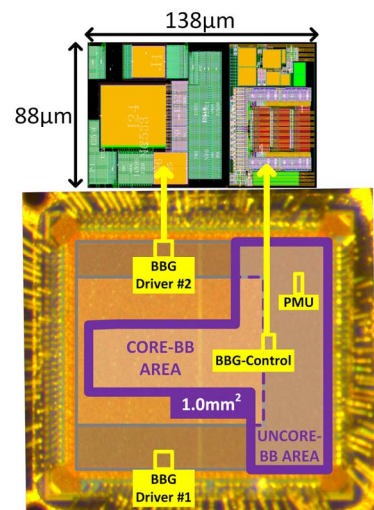


Figure 7. Die-photo and BBG layout

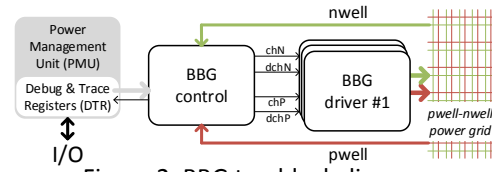


Figure 2. BBG top block diagram.

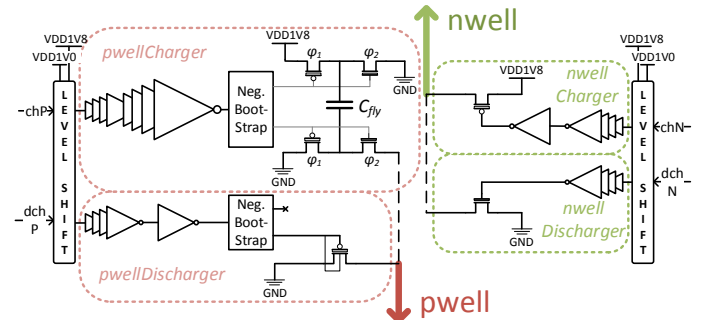


Figure 3. Driver unit - block diagram.

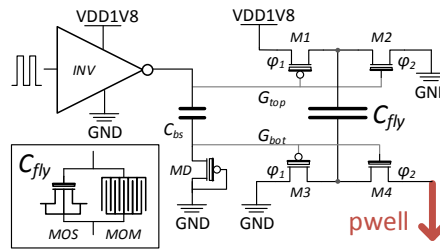


Figure 4. Negative voltage generation - "1:-1" switch-capacitor charge pump.

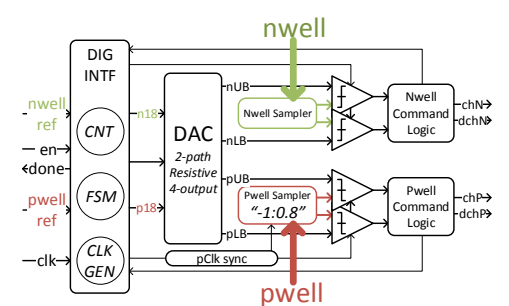


Figure 5. Control unit - block diagram.

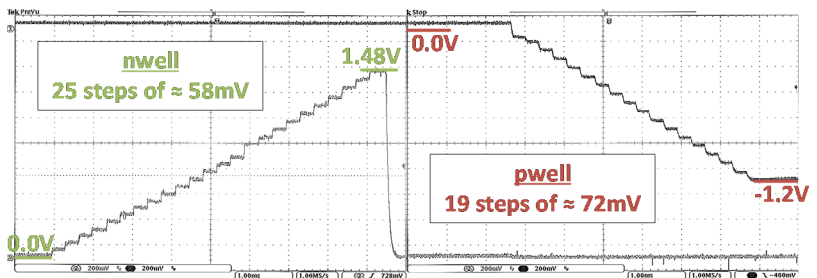


Figure 8. Nwell and pwell voltage sweeps.

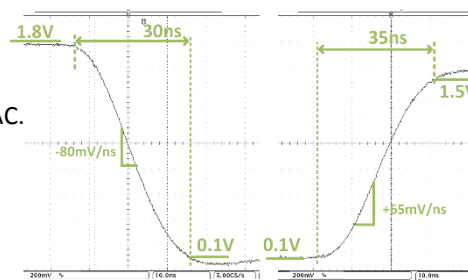


Figure 9. Nwell discharging and charging.

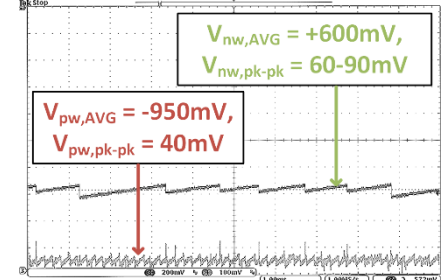


Figure 11. Maintaining the BB values.

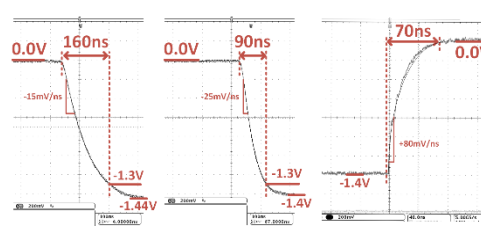


Figure 10. Pwell charging and discharging.

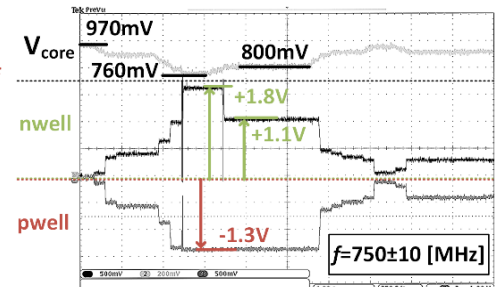


Figure 12. Adaptive BB for CPR frequency tracking on variable V<sub>CORE</sub>.