On-Chip Supply Power Measurement and Waveform Reconstruction in a 28nm FD-SOI Processor SoC

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***Abstract*—A compact system for on-chip supply current waveform reconstruction and power estimation is presented. The system, comprising a programmable current load, a sampling comparator and processing logic, is implemented in a 28nm FD-SOI system-on-chip (SoC) to monitor the supply of a digital processor generated by a switched-capacitor DC-DC converter. The monitoring system is able to reconstruct the rippling supply waveform and extract core power consumption with a low area overhead (0.3% of the die area). Two different techniques yield either 2.5% accuracy with a 28 ms sample time or 5% accuracy with a 1 µs sample time, providing valuable information for on-chip power management strategies.**

I. Introduction

Portable devices are energy-limited, and their instantaneous power consumption can significantly exceed their thermal design constraints. Fine-grained dynamic voltage and frequency scaling (DVFS) has emerged as a technique to carefully manage the energy consumption of such systems. Efficient implementation of such methods is enabled by integrating voltage regulators on die and adapting their output voltage based on instantaneous measurements of power consumption.

Traditional power monitoring based on series resistors is implemented either off-chip [1], partially integrated on-chip [2] or by using an on-chip sleep transistor [3]. More recent methods are based on indirect measurements from which power consumption can be reconstructed based on the functionality of the integrated DC-DC converter. Sinangil et al. measured the discharge time of the off-chip capacitor of a buck converter [4]. Although accurate, this technique causes a droop in the supply voltage. Dutta et al. proposed to measure the switching frequency of an off-chip boost converter [5]. All of those approaches rely on intrusive measurements or off-chip components.

In this paper we propose two fully integrated measurement techniques suitable for simultaneous-switching switched-capacitor DC-DC converters (SC-DCDC) [6]. SC-DCDC regulators can be completely integrated on chip and achieve conversion efficiencies of up to 86% when combined with adaptive clocking. Such high efficiencies are achieved by allowing a large ripple in the supplied voltage.

Accurate estimation of power consumption can thus be achieved by reconstructing the supply waveform on-chip. This information can then be used to optimize the SC-DCDC efficiency across the range of operating conditions. Methods for on-chip waveform capture have been proposed recently [7], [8] with the primary goal of monitoring supply droops. The method implemented in this work is simpler: it leverages the fact that the SC-DCDC ripples are synchronous to a known toggle signal, which is used as a trigger for statistical reconstruction.

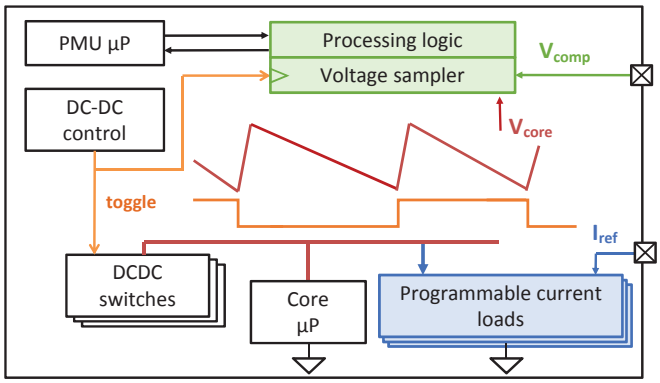

Fig. 1. System overview.

As a trade-off between accuracy and sampling speed, this paper proposes a second technique for power estimation based on the measurement of the SC-DCDC toggle frequency. Compared to [5], we propose this method for a fully integrated converter, which requires a finer modeling of loss effects to achieve a satisfying accuracy. Both approaches operate non-intrusively and fully in the background.

II. Power Supply Monitor

A. System Architecture

Figure 1 shows a block diagram of the SoC. The supply V_{core} of the RISC-V processor core is generated by the SC-DCDC unit cells [6]. The monitoring system includes the SC-DCDC control logic, a programmable current load, and sampling and processing logic to capture V_{core} variations. The main processor is directly supplied by V_{core}. A $0.053\,\text{mm}^2$ power management unit (PMU) processor controls the waveform reconstruction block and acquires the results of the measurements [9].

The power supply monitor is integrated with a simultaneous-switching SC-DCDC converter [6]. The circuit employs a lower-bound controller that toggles the flying capacitor when the drooping core voltage reaches the threshold of a comparator. Measurements showed that efficiency is optimal for a ripple voltage of around 100 mV. The converter is reconfigurable in three operating modes down-converting from a 1.8 V supply (1:2 1.8 V) and a 1.1 V supply (2:3 1.1 V and 1:2 1.1 V).

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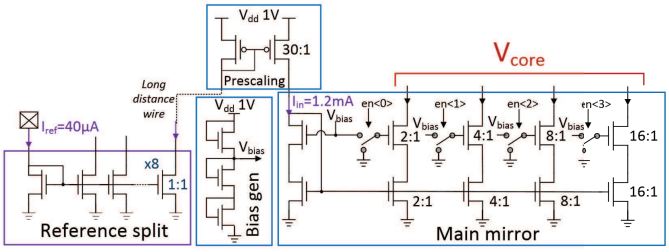


Fig. 2. Programmable load current mirror schematics.

B. On-Chip Tunable Load

To calibrate the power monitoring system and measure the efficiency of the SC-DCDC converter, the output load must be set precisely. Recalibration must be possible at runtime to account for time-varying load behavior such as temperature changes, so the load must also be programmable in the background during operation. Zimmer et al. use the processor itself as a load after characterizing it with the SC-DCDC converters bypassed [6]. This approach is disruptive at runtime and sensitive to PVT conditions. The alternative of using an off-chip current sink would require a dedicated IO pad and a tunable off-chip component. This approach may not sink a constant current because of the high-frequency components of the SC-DCDC output voltage.

Figure 2 shows the proposed solution, an on-chip tunable load relying on a low-swing cascode current mirror that multiplies a fixed off-chip reference. This design is chosen to guarantee a fixed current across the full SC-DCDC output voltage range. To limit local IR drop, eight different mirror units are distributed across the chip, and a 1:1 reference splitter replicates the 40 µA off-chip reference to each mirror. Each mirror has a 4-bit weighted programming code, resulting in a load tunable from 0 to 288 mA in 120 steps of 2.4 mA. When the mirrors are fully turned off, their simulated current leakage in the worst-case corner is 32 µA, which is negligible compared to the power consumption of the SoC. Run-time calibration can be achieved by momentarily clock-gating the core so it provides a constant leakage, and varying the tuning code of the mirrors.

C. Tunable Delay Comparator

The acquisition of the V_{core} amplitude is triggered by the SC-DCDC edges through the use of the SC-DCDC controller toggle signal generated by the lower-bound comparator. A track-and-hold circuit followed by an analog-to-digital converter would be unnecessarily complex and may not have enough resolution to capture the ripple voltage extremes immediately before and after the SC-DCDC toggle.

Figure 3 presents the statistical method used in this work. An off-chip voltage V_{comp} is provided as a tunable reference. When the SC-DCDC toggles, an additional comparator fires after a tunable delay to estimate if V_{core} is greater than V_{comp}. By sweeping V_{comp} and the delay, and repeating the measurement across many ripple events, the waveform can be statistically reproduced.

The range of the tunable delay circuit is designed be at least one SC-DCDC ripple period (>125 ns at minimum load current) to allow for full waveform reconstruction. The time resolution must also be finer than the transient of the rising voltage, which is on the order of 1ns. To achieve such a

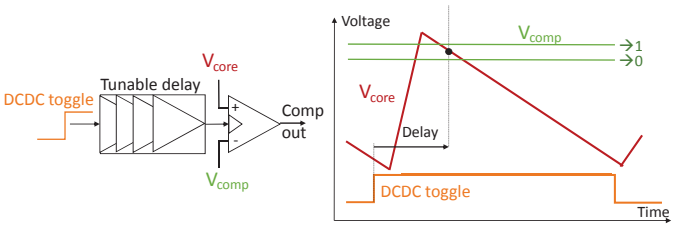


Fig. 3. Principle of the proposed statistical waveform reconstruction.

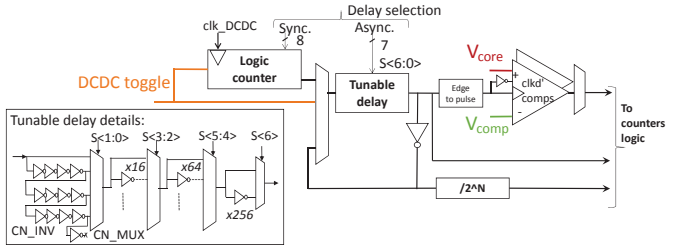


Fig. 4. Details of the synchronous and asynchronous delay elements and subsequent comparators.

wide dynamic range, a coupled synchronous and asynchronous delay method is employed as shown in Figure 4. The first stage consists of a programmable counter, synchronous with the control logic that generates the SC-DCDC toggle rising edge. After overflowing, the comparator generates a positive edge which is delayed through a 200 ps-to-4 ns tunable-length inverter chain with 32 ps steps. After exiting the delay chain, the edge is converted to a pulse and sent to a StrongARM comparator [6]. An nMOS or pMOS comparator can be selected depending on the value of V_{comp}.

The delayed edge and the result of the comparison are sent to a custom logic block. This block synchronizes the signals to a 1 ps reference clock and counts the number of times the comparator has triggered ($V_{core} > V_{comp}$) to provide the fraction of the comparison events which are positive. It also measures the SC-DCDC toggle frequency.

III. Silicon Implementation

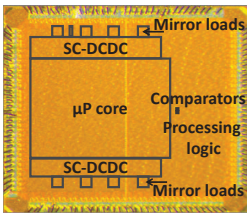
A. Test Chip Implementation

To validate the measurement principle, the waveform capture instrumentation has been implemented in a testchip using 28 nm ultra-thin body and BOX fully-depleted silicon-on-insulator (UTBB FD-SOI) technology [10]. The current mirror and the strongARM comparators are designed as custom analog macros. The gates in the asynchronous delay chain are selected manually but automatically placed and routed. The synchronous delay block and the aggregating logic are implemented at RTL level and automatically synthesized, placed and routed. These blocks are powered by a fixed 1V supply.

Figure 5 presents the system blocks annotated on the full chip micrograph. The current mirrors are spread over 8 blocks, and each occupies a 90 µm × 90 µm square. The reference splitting mirror is 78 µm × 12 µm and the comparators and synthesized processing logic occupy 9305 µm^2. The total instrumentation overhead represents 2.5% of the die area.

B. Mirror Load Performance

The current load has been characterized over core voltage changes to validate its behavior. A fixed voltage is applied



Function	Mirror load	Delay element	Processing Logic	Area [µm²] (% of chip)
Calibration	X			65,736 (2.16%)
Waveform Reconstruction		X	X	9,305 (0.31%)
Frequency Measurement			X	8,166 (0.27%)

Fig. 5. Annotated test-chip micrograph and summary of blocks contributing to the proposed on-chip functions.

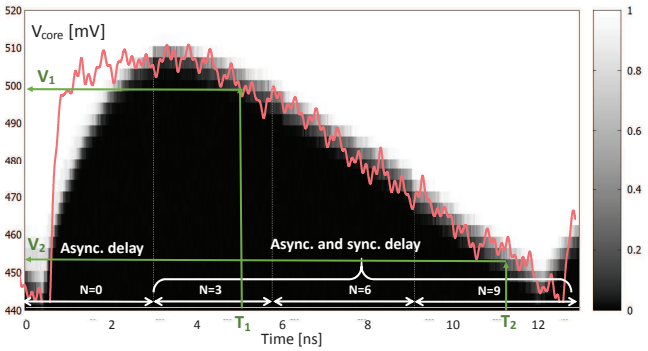


Fig. 6. Statistical waveform reconstruction of a SC-DCDC ripple in 1:2 1.1V mode (in gray) compared with direct oscilloscope measurement (in red).

to V_{core} and the current drawn is measured as the mirrored current is incrementally increased. Measurements show good linearity across calibration codes. The measured current across the full 1 V to 0.5 V operating range is limited to $\pm 1\%$ error or ± 2 mA at maximum load. This result demonstrates that the load acts as a nearly ideal current source under the rippling supply voltage.

C. Delay and Voltage Calibrations

To produce run-time SC-DCDC waveform cross-sections, the asynchronous delay linearity must be validated. For each of the delay settings, the delay line is looped to form an oscillator and the period is measured by the processing logic. The unit delay is measured to be 31.6 ps over a 1 V supply, covering a delay range from 280 ps to 4299 ps. The synchronous delay ranges from 0 to 256 ns with 1 ns steps. Finally, the comparator is calibrated by applying a fixed, known core voltage. Its offset is measured and subtracted from all subsequent measurements.

IV. Monitoring Applications

A. Full SC-DCDC Output Ripple Reconstruction

Figure 6 illustrates a full statistical reconstruction of the core supply waveform obtained by sweeping V_{comp} and the sampling delay of the comparator. The plot reconstructs a full ripple in 1:2 1.1V mode by stitching together four different acquisitions, one where only the asynchronous delay was swept and three with both asynchronous delay sweep and a synchronous delay of 3, 6 and 9 cycles. A total of 13.8 million samples were used to create the waveform histogram. Apart from the fast transient rise, the system reconstructs the ripple properly up to the next toggling event. The inaccuracy in capturing the fast transient stems from process corner and comparator transient offset artifacts. This in-situ detection of the minimum voltage supplied to the core can be used as a safeguard to detect core voltage droops.

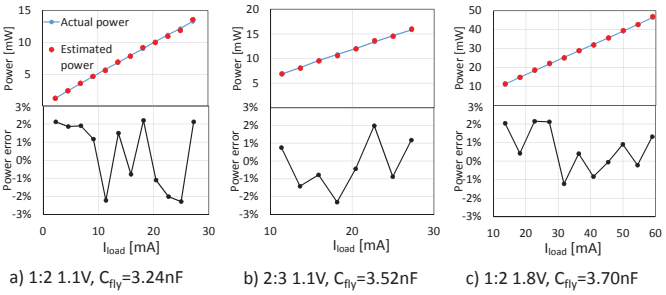


Fig. 7. Power estimate by ripple slope computation in each of the three SC-DCDC modes.

B. Power Estimate by Waveform Slope Capture

The main application of the proposed SC-DCDC converter instrumentation is to provide rapid and non-invasive information about the core power consumption. The output of the custom logic can be programmed and processed by the on-chip PMU to extract power estimates. The first proposed approach is based on computing the slope of the reconstructed waveform. Two delays T_1 and T_2 are chosen to encompass the linear part of the waveform (illustrated in green on Figure 6) and the corresponding voltages V_1 and V_2 are reconstructed. The total power consumption is then estimated by the energy discharge of the SC-DCDC flying capacitor C_{fly} between T_1 and T_2 [4], [6]:

$$P = C_{fly} \cdot (V_1^2 - V_2^2)/(T_2 - T_1) \quad (1)$$

Figure 7 shows the power estimated by Eq. 1 compared with the known power drawn by the current mirror load. In each SC-DCDC mode the error is within $\pm 2.5\%$. As the flying capacitor is implemented as an on-chip MOM+MOS, the exact C_{fly} value is PVT sensitive; it is estimated in each of the three modes as a fitting parameter. Each measurement of V_1 and V_2 requires 7 acquisitions of 10,000 samples, and the setting of the off-chip V_{comp}. Assuming a 100 ns ripple period and a 1 ms latency of the reference voltage generator, a calibrated sample can be generated every 28 ms.

C. Power Estimate Via Ripple Frequency Capture

To provide a finer time resolution of the power estimate, a second method based on the measurement of the SC-DCDC toggle rate can be used. For this technique, it is important to differentiate between *core power*, which is used to determine core energy efficiency, and *wall-plug power*, useful for battery life estimation and total dissipated power (TDP) limits.

Figure 8 presents the measured and estimated power for the 2:3 1.1V mode. The SC-DCDC toggle frequency F and wall-plug power are measured for each of the current load settings. The core power is computed from the current load and the measured average voltage. The purpose of the model is to provide a calibrated estimate of the wall-plug and core power consumption computed by the PMU at run-time by measuring F only. The simplest estimate relies on assuming power to be proportional to F [5]. This method significantly overestimates both core and wall-plug power, because at high loads the ripple amplitude decreases in the fast switching limit of the regulator [11]. This results in a smaller amount of energy transfer per SC-DCDC switching event.

In SC-DCDC converters, losses are dominated by switching and bottom-plate losses [6], which are proportional to the

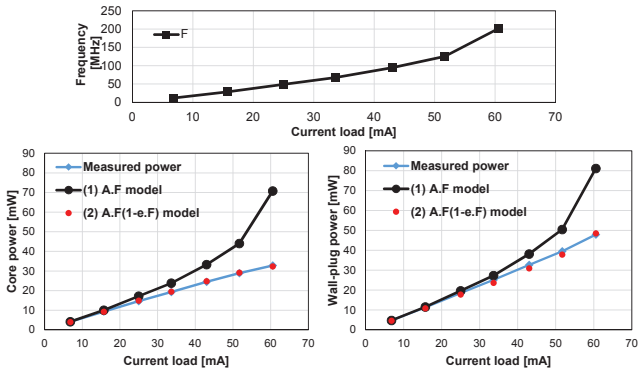


Fig. 8. Measured SC-DCDC toggle frequency F (top plot) and measured and model estimated core power (bottom left) and wall-plug power (bottom right) in 1.1V 2:3 SC-DCDC mode.

frequency. A refined power model accounts for this fact by adding a fitting parameter e as a loss term:

$$P = A \cdot F(1 - e \cdot F) \tag{2}$$

This model yields an excellent fit with a -3.2%/+1.2% error for core power and -6.1%/+3.2% for wall-plug power in the full range of operation of the DC-DC converter in 2:3 1.1V mode. A similar accuracy of -0.6%/+2.7% (core) and -4.5%/+5.8% (wall plug) and -5.3%/+4.9% (core) and -1.4%/+4.9% (wall plug) is obtained in 1:2 1.8V and 1:2 1.1V modes, respectively. The fitting parameters A and e have separate values for each of the three SC-DCDC modes and for core and wall-plug power; the parameters can be obtained via a two-point calibration for each mode.

Table I shows the benefits of the two proposed power monitoring strategies. The waveform reconstruction approach offers the best reported accuracy of 2.5%, while the frequency counter model offers a possibility for a power readout in every SC-DCDC switching event without requiring any off-chip components or communication. This method of power monitoring is not specific to simultaneous-switching SC-DCDC converters. For more conventional interleaved SC-DCDC converters [11], the power can also be extracted from the switching frequency. The fitting parameters in Equation 2 would simply need to be adjusted to account for charge-sharing losses, which are proportional to F.

V. Conclusion

A simultaneous-switching SC-DCDC converter is instrumented with an on-chip power measurement system. The power estimation circuit is implemented in a RISC-V SoC to provide on-chip monitoring of the supply voltage and power delivered to the processing core. Two power estimation methods are implemented and the supply voltage waveform is reconstructed accurately, matching off-chip measurements. The waveform-based approach to power estimation is accurate within 2.5% while the frequency-based approach provides both on-chip (within 5%) and wall-plug (within 6%) estimates. The measurement system requires minimal area overhead (2.2% for the calibration load and 0.3% for instrumentation), resulting in an attractive building block for low-power adaptive SoCs.

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TABLE I. Comparison with other power monitors

	This Work		[2]	[3]	[4]	[1]	[5]
Strategy	Waveform Reconstruction	Frequency counter	Series resistor	Sleep transistor	Capacitor discharge	Series resistor	Frequency counter
Technology	28nm FD-SOI	28nm FD-SOI	90nm CMOS	180nm CMOS	180nm CMOS	Multiple ICs board	Multiple ICs board
Off-chip components	Voltage source	-	R	-	L,C (shared)		
Area [mm^2]	0.066+0.009	0.066+0.008	0.0128	0.01	0.036	871	NA
Invasive	No	No	Yes	Yes	Yes	Yes	No
Test load	On chip with off-chip Iref	On chip with off-chip Iref	On chip with off-chip Rx	On-chip	Not needed	Off-board	Off-board
Accuracy	2.5%	5%	5%	8.5%	10%	3%	15%
Sampling time	28ms	$1\mu s$	$8\mu s$	$0.08\mu s$	NA	$1\mu s$	$15\mu s$