

A Passive-Mixer-First Receiver with LO Leakage Suppression, 2.6dB NF, >15dBm Wide-Band IIP3, 66dB IRR Supporting Non-contiguous Carrier Aggregation

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Abstract—A passive-mixer-first receiver design in 28 nm CMOS is presented where the front-end 5-bit mixer DAC provides a wide-band tuneable impedance match to suppress the LO leakage as well as to improve image rejection performance. Baseband LNA together with the AC-boosting compensation amplifier provides a 50MHz baseband bandwidth, which allows support for non-contiguous carrier aggregation for LTE. The proposed design can suppress multiple LO harmonics down below -62dBm. The system achieves < 3dB NF, >15dBm IIP3 and an IRR > 66dB with 60mW power

Index Terms—LTE, passive mixer, receivers, carrier aggregation, image rejection.

I. INTRODUCTION

LTE Advanced, a new standard from the 3GPP committee, introduces carrier aggregation (CA) to address the demand for further data rate increases. Among many different scenarios, intra-band non-contiguous CA presents serious challenges to receivers' noise figure and linearity performance due to the in-band and out-of-band interference. A mixer-first design [1] offers superb linearity without a large power penalty. However, the design suffers from LO leakage re-radiation. Without backward isolation from the LNA, the strong LO signals can potentially leak to the antenna. Also, conventional mixer-first receivers have rather limited image rejection (IR) performance, making them unsuitable for CA.

This work proposes a highly linear mixer-first receiver to support LTE non-contiguous CA. A 5-bit mixer DAC (MxDAC) is integrated into every mixer to provide calibration for LO leakage and image rejection. The receiver achieves a 2.6dB Noise Figure (NF) and > 15dBm IIP3 while consuming only 60 mW of power, which also includes the five on-chip LDOs.

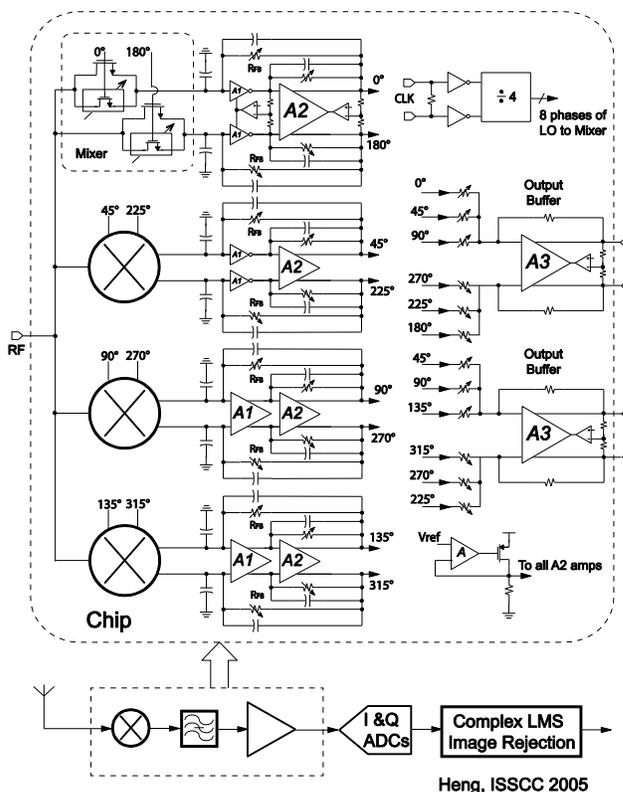


Fig. 1. Architectural overview of the passive mixer-first LTE radio receiver system.

II. SYSTEM OVERVIEW

Fig. 1 shows an overview of the entire system. The single-ended RF signal is down-converted by eight different paths, each of which is driven by a non-overlapping 12.5% duty-cycle clock. When combined with appropriate weightings, eight-phase down-conversion not only rejects the 3rd and 5th harmonics, but also reduces the effect of noise folding, and hence improves the overall NF [1]. Each of the mixer units consists of a mixer core

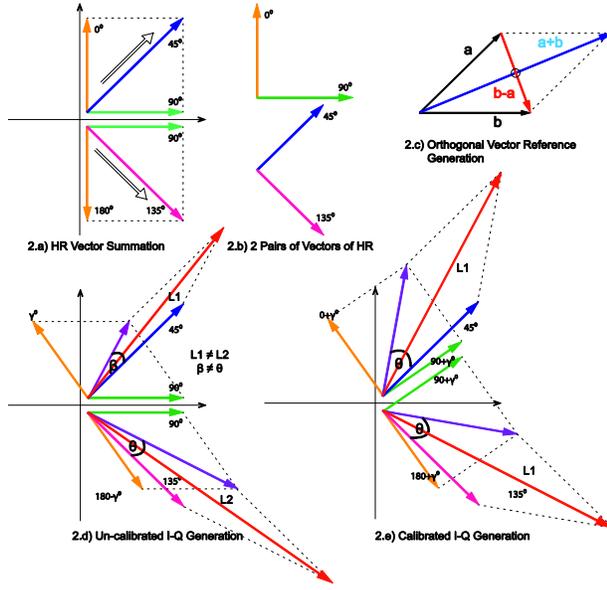


Fig. 2. Principle of IQ correlated orthogonal calibration (IQ-COC)

and an additional 5-bit MxDAC for fine tuning. The baseband circuit is implemented as two amplifiers (A_1 and A_2) in cascade to achieve a wide baseband bandwidth (50MHz) and high slew rate while simultaneously maintaining low power consumption. A_1 serves as a transconductor, while A_2 works as a trans-impedance amplifier. The dominant pole of the baseband circuit is set by the capacitors to the ground at the input of A_1 , and the feedback capacitors set the secondary pole. Five separate LDOs are implemented on chip for better supply isolation. An on-chip LO divider generates all of the required clock phases from an external LO running at 4X the carrier frequency. After off-chip digitization, a digital LMS image rejection filter similar to what is reported in [2] helps to further enhance the IR performance.

Two major issues with this architecture are LO leakage and limited IR performance. LO leakage is a result of mismatches among the mixers and the LO buffers. In this design, the embedded MxDAC can fine-tune the mixer devices' sizes, and alleviate this issue. Moreover, since the MxDAC improves the matching of the mixers, the IIP2 performance is also enhanced. IR performance, on the other hand, is limited by the phase and the gain mismatches among different paths [2]. Compared to the gain mismatch, the phase mismatch is harder to calibrate.

III. IQ CORRELATED CALIBRATION

Fig. 2 shows the principle of the IQ vector formation. In a harmonic rejection (HR) system, as demonstrated in 2.b), there are two pairs of orthogonal vectors (0° and 90° , 45° and 135°). As shown in Fig. 2.c), a pair of perfectly

orthogonal references can be generated by vector summation and subtraction of a pair of vectors. However, this idea cannot be simply applied to a HR system, as illustrated in Fig. 2.d), for reasons explained in [2].

To alleviate this issue, the concept of correlated orthogonal calibration (IQ-COC) is proposed in this work. As shown in Fig. 2.e), the pair of 0° and 90° signals can be first used to create the orthogonal references to calibrate the pair of 45° and 135° . Afterwards, the calibrated 45° and 135° pair can in turn help correct the phase mismatch of the 0° and 90° pair. As illustrated in Fig. 2.d), in a HR system, phase mismatch alone can result in both phase and gain mismatches for the final IQ channels. Although the phase values of different paths might rotate after IQ-COC, the IR or EVM performance is not degraded, because the entire resulting signal constellation rotates. This can easily be re-adjusted in the digital domain. The calibration procedure starts with first iteratively sweeping through all of the codes of the MxDAC to achieve a balanced suppression of leakages from multiple LO harmonics. The gain of the baseband amplifiers is then fine tuned to reduce the gain mismatches between different paths. Afterwards, IQ-COC is applied to the system one orthogonal pair of channels at a time to fine-tune the code word of each MxDAC. Finally, the digital LMS image rejection filter is enabled to further enhance the IRR.

IV. OPTIMIZING FOR THE NOISE FIGURE

The noise figure of such a system can be described as,

$$F \approx 1 + \frac{R_{sw}}{R_a} + \frac{R_a + R_{sw}}{19R_a} + 8 \frac{(R_a + R_{sw})^2}{R_a R_{FB}} + \frac{1}{8} \left(\frac{\overline{v_{n,A}^2}}{4kTR_a} \right) \left(\frac{8(R_a + R_{sw})}{R_{FB}} + 1 \right)$$

where the R_a is the antenna impedance. The noise figure is set by the mixer switch on-impedance R_{sw} , the feedback resistor R_{FB} and the noise from the amplifier $\overline{v_{n,A}^2}$.

In this work, the switch resistance R_{sw} is substantially reduced utilizing the 28nm technology. The 28nm technology provides superior switches with much lower on-impedance as well as lower switching power. Also, baseband architecture is optimally refined, such as the shunt feedback is wrapped around two stages of gain. This allows the feedback resistor R_{FB} to be large and hence contribute very little noise. Finally, large amount of design effort has been invested to minimize $\overline{v_{n,A}^2}$ from the first stage amplifier, such as careful device sizing to minimize flicker noise contribution and optimization for its G_m and bias condition for the best trade off between power and noise performance.

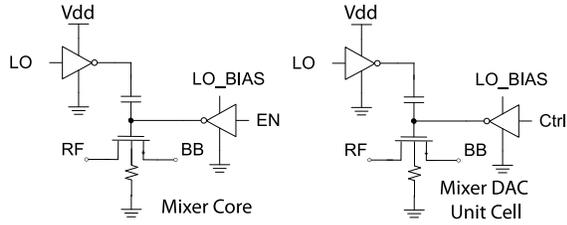


Fig. 3. Circuit implementation of the mixer system.

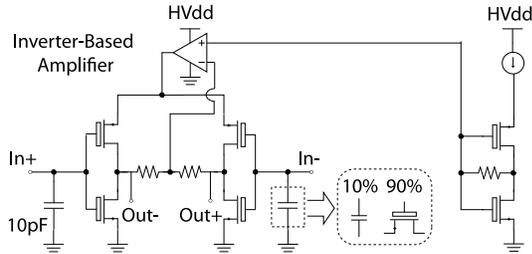


Fig. 4. Details of the inverter-based amplifier A1.

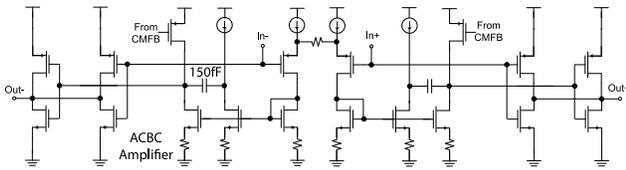


Fig. 5. Circuit details of the baseband ACBC amplifier A2.

V. CIRCUIT IMPLEMENTATION

Fig. 3 shows the details of the mixer design. The unit cell of the MxDAC occupies approximately 1% of the mixer core, and the mixers are DC-biased to 0.65V.

The amplifier A_1 in Fig. 1 is an inverter-based thick oxide design for ensuring large-signal linearity and better noise performance. The detail of it is shown in Fig. 4. To improve the power supply rejection (PSR) performance, the common-mode control amplifier is designed as a low-dropout (LDO) amplifier. The LDO reference comes from a local replica bias. All LDOs operate with 1.5V.

The second amplifier A_2 in Fig. 1 must have a high gain and wide bandwidth, which is quite challenging with a 1V supply. A two-stage amplifier design can meet the gain requirement but the bandwidth and slew rate suffer. An AC-boosting compensation (ACBC) scheme [3] provides a better alternative for the trade-off. As shown in Fig. 5, a PMOS input pair is adopted for better flicker noise performance. Also, the input signal is fed forward to the output stage to create a feed-forward zero, which allows for smaller compensation capacitors and hence faster slew rate. Moreover, the output stage has a class-AB structure for even better slew rate and linearity performance.

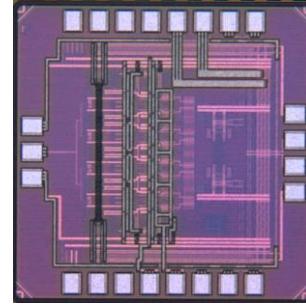


Fig. 6 Chip microphotograph

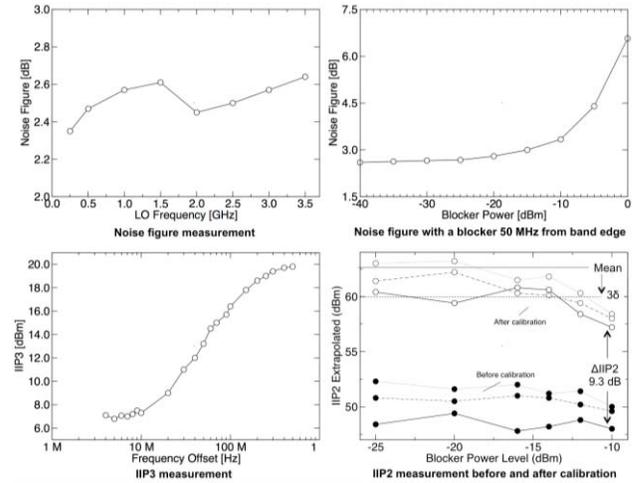


Fig. 7. Measurement results for noise figure and linearity.

VI. DESIGN PROTOTYPE AND MEASUREMENT

The design is implemented in a general-purpose 28nm technology with a 1V supply and an active area of 460 μm by 500 μm as shown in Fig. 6.

Fig. 7 shows the noise and linearity measurement results. To measure the noise figure, the conversion gain is first measured, which is $\sim 35\text{dB}$. Then the output noise is integrated with the losses before the RF input are accurately embedded. Finally, the noise figure is extracted from dividing the output noise by the conversion gain. The measured double-sideband noise figure varies from 2.4 to 2.6dB. In the presence of a 0dBm close-in blocker that is 50MHz away from the band edge, the NF degrades to 6.5dB. The receiver frontend achieves a $>15\text{dBm}$ IIP3 for tone spacing larger than 50MHz. The LO leakage calibration also improves the IIP2 performance. As shown in Fig. 7, the improvement in IIP2 across the three silicon samples is at least 9.3dB. The IIP2 results after calibration are in good agreement with the simulation (mean value and its distribution), which are overlaid on top of the measurement results.

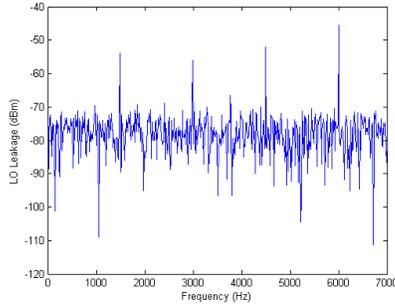


Fig. 8. LO leakage prior to calibration.

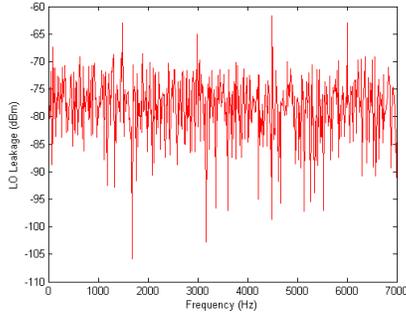


Fig. 9. LO leakage after calibration.

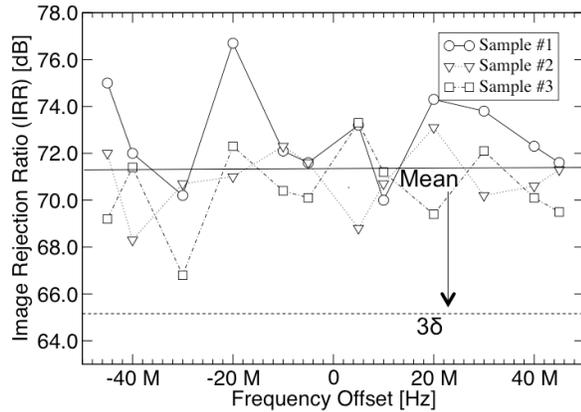


Fig. 10. Image rejection ratio measured at 2 GHz frequency.

LO leakage measurement results at 1.5GHz operating frequency are detailed in Fig. 8 and Fig. 9. The calibration effectively suppresses LO harmonics leakage from -48 dBm (4th harmonic) down to -62dBm (3rd harmonic). Moreover, Fig. 10 shows that at 2GHz operating frequency, the measured IRR of the three samples exceeds 66dB across the 100MHz complex baseband bandwidth. It also fits well with the simulation results, and the simulated mean value and its distribution are shown on top of the IRR measurement data. Finally, the comparison table summarizes the performance and compares it with the other latest state-of-the-art designs.

TABLE I
PERFORMANCE COMPARISON TABLE

	[4]	[5]	[6]	This Work
Technology	28nm	180nm	45nm	28nm
RF Freq. [GHz]	0.6-3	0.1-1.8	0.7-2.7	0.4-3.5
Bandwidth [MHz]	N/A	N/A	50	15-50
NF [dB]	1.8 (3)	3.5	3.8	2.4-2.6
P1dB [dBm]	-6	N/A	N/A	+4.6
NF w/ 0dBm [dB]	13 (9)	N/A	5.1	6.5
OOB-IIP3 [dBm]	10	22	2.75	20.5
IIP2 [dBm]	49	70	40	64
HR (3rd/5th)	52/54	N/A	N/A	47/51
IRR [dB]	N/A	N/A	70	66
LO Leakage [dBm]	N/A	N/A	N/A	-62
Power [mW]	39-70	43-67	15	38-75*
Supply [V]	1	1.8	1	1/1.5
Area [mm ²]	5	0.8	0.16	0.23

*Power number includes all the on-chip LDOs

VII. CONCLUSION

This work demonstrates a mixer-first receiver designed in 28 nm CMOS. The 5-bit MxDAC provides a wide-band tuneable match to suppress the LO leakage. Baseband LNA together with the ACBC amplifier provides a 50MHz baseband bandwidth. It provides support for non-contiguous carrier aggregation for LTE in power efficient manners. The circuit achieves <3dB NF, >15dBm IIP3 and 35dB gain with 60mW power.

ACKNOWLEDGMENT

The authors thank Y. Wang, R. Sathwani, S. Ramon, P. Schwendt and O. Korobeynikov from Intel.

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