Dynamic Single-P-Well SRAM bitcell characterization with Back-Bias Adjustment for Optimized Wide-Voltage-Range SRAM Operation in 28nm UTBB FD-SOI

O. Thomas[1,2], B. Zimmer[1], S. O. Toh[1], L. Ciampolini[3], N. Planes[3], R. Ranica[3] P. Flatresse[3] and B. Nikolić[1]

[1] Berkeley Wireless Research Center, Berkeley, CA, United States, email : olivier.thomas@cea.fr – [2] CEA-LETI Minatec Campus, 38054 Grenoble Cedex 9, France, Crolles – [3] ST Microelectronics, 38926 Crolles, France

Abstract

This paper demonstrates the 28nm ultra-thin body and buried oxide (UTBB) FD-SOI high-density (0.120µm²) single p-well (SPW) bitcell architecture for the design of low-power wide voltage range systems enabled by back-bias adjustment. The results from a 140kb programmable dynamic SRAM characterization test module provide both information about location and cause of failures as well as power and performance by mimicking system operating conditions over a wide supply voltage range. A 410mV minimum operating voltage and less than 310mV data retention voltage with a leakage current close to 100fA/bitcell are measured. Improved bitcell read access time and write-ability through back-bias are demonstrated with less than 5% of stand-by power overhead.

Introduction

Voltage reduction and increased variability associated with technology scaling compromise margins necessary for robust SRAM operation. Ultra-thin body and buried oxide (UTBB) FD-SOI eliminates channel doping to lower intrinsic transistor variability [1], and offers multiple threshold voltages through selection of the well under the buried oxide [2-3] with an ability to lower SRAM operating voltage. Traditionally, SRAM functionality is evaluated through static voltage margins during the development phase and is monitored with built-in self-test (BIST) in production [4]. Dynamic metrics [5] more accurately characterize SRAM read and write margins than static ones. In scaled technologies dense SRAM may only be functional with dynamic stimuli [6]. This work demonstrates the dynamic performance of the high-density (0.120µm²) single-P-well (SPW) 6T bitcell architecture [7-8] for wide voltage range modern wireless systems, using a complete SRAM dynamic defect and performance characterization module designed in an early production 28nm UTBB FD-SOI dual V_T CMOS process.

UTBB devices and Single-P-Well SRAM features

UTBB-FDSOI devices (Fig.1) are fabricated with a gate-first high-k metal-gate 28nm technology implementing an ultra-thin silicon layer (7nm) on top of a 25nm buried-oxide (BOX) [9]. The thin BOX isolation enables to apply efficient extended body biasing (V_B) without source-drain junction leakage and to adjust transistor V_T with well doping types providing low-V_T (LVT) and regular-V_T (RVT) devices (Fig.2) [2-3]. In the SPW design (Fig.3) [7], both PMOS and NMOS devices are placed over a common p-well, leading to LVT PMOS pull-up (PU) devices and RVT pull-down (PD) and pass-gate (PG) NMOS devices (Fig.4). The common PW is isolated from the grounded p-substrate by using a deep n-well (DNW) biased at the SRAM array supply voltage or higher. By changing V_{PW} (Fig.5), back-bias is applied to all SRAM transistors trading-off access time, power consumption and stability. Derived from high-density (0.120µm²) regular SRAM bitcell architecture, SPW design does not require process and footprint modifications (Fig.6) [8] and reduces scaling limitations caused by well-proximity and diffusion issues.

Test chip features

The test chip (Fig.7) provides a dynamic characterization module designed to evaluate SRAM bitcell retention-stability (RET), read-stability (RS), write-ability (WA), and read-access timing faults (RA) (Fig.8). The module (Fig.9) consists of a 140kb SPW SRAM macro clocked by an on-chip pulse

generator (PG) and controlled by a programmable BIST. The SPW SRAM macro includes 4 arrays of 280 columns by 128 word-lines (WL). The BIST is a finite state machine with 3 paths (Fig.10). BIST setup data are loaded through a scan chain and can be scanned out for verification through the first path. The memory initialization is checked through the second path, while the third path is dedicated for the memory tests. Input and output data are scanned at low frequency (CLK_L) and the tests can be performed at up to 800MHz using an external clock reference (CLK_H). A synchronizer circuit avoids hazardous glitches for signal traversing from low (high) to high (low) clock frequency. The BIST supply voltage (V_{DDB}) is separated from the SRAM. The SRAM output data (Do<69:0>) are level-shifted (LV) to the BIST to extract errors (E<69:0>). While the BIST runs at a nominal voltage, the SRAM macro can be run at a lower voltage. The SRAM periphery (V_{DDP}) and array (V_{DDA}) supply voltages are also electrically independent for bitcell power consumption measurement. SRAM bit error rate (BER) evaluation consists of 3 main steps (Fig.11). It begins with a safe initialization (INIT) of the SRAM, continues with the selected test (RD, WR…) and ends with a safe check (CHECK). Before each step, the SRAM supply voltage and the clock frequency are set to fulfill the initialization, test and check conditions. The initialization, test and check are performed column-by-column to avoid half-selected bitcell failures in BER evaluation.

Experimental results and discussion

The characterization test module determines both the location and cause of failures for every bitcell in the array (Fig.12) by measuring independently the BER of each mode (RET, RA, RS, and WA) (Fig.13). By mimicking the SRAM operating conditions, it enables optimization of conflicting design requirements (i.e. WA vs. RS) and performance trade-offs (i.e. column height vs. RA) (Fig.14). The minimum SPW bitcell operating voltage (V_{MIN}) is RA limited for WL pulse widths lower than 10ns and WA limited for longer pulse widths, reaching static test results (Fig.15). To demonstrate the use of p-well back-bias voltage in a wide tuning range to improve SRAM performances and reduce standby-power, Fig.16-20 show how the RA and WA BER as well as the minimum data retention voltage (DRV) and the bitcell static power are affected. Increasing V_{PW} reinforces NMOS and weakens PMOS (cf. Fig.5), and in turn, improves RA but harms DRV and WA. Thus for fast access time a positive back-biasing (V_{PW}>0V) can be used to improve RA (Fig.16), whereas for ultra-low operating voltage a V_{PW} close to 0 enables a V_{MIN} as low as 410mV. In sleep mode, V_{PW} is adjusted to minimize DRV and stand-by power. In negative back-bias (V_{PW}<0) the strength of the bitcell inverter devices is more balanced. A DRV lower than 310mV is achieved (Fig.17) allowing an ultra-low leakage current in average close to 100fA/bitcell (Fig.18). The bitcell static power depends on both PMOS and NMOS leakage currents. While positive (negative) back-biasing increases (reduces) the NMOS leakages it reduces (increases) the PMOS leakages. The minimum static current is obtained for V_{PW} in between -0.5V and 0V (Fig.19). However, it is worth to note that back-biasing adjustment has a low impact on the SPW bitcell static power due to the NMOS PMOS leakage compensation. Thus, it enables wide back-bias range adjustment to improve access time and bitcell robustness with a very low stand-by power overhead. The test module also helps to track bitcell mechanisms of failures. WA V_{MIN} is limited by the completion of the transition of the high logic level node driven by PMOS PU transistors and the discharge of the high logic level node driven by PG/PU current ratio (Fig.20) [7]. Completion and discharge failures are traded-off versus the PU strength. In negative back-biasing range WA failures are caused by the weak PG/PU ratio, while in positive back-bias range it originates from a weak PU completion explaining the optimum WA achieved at V_{PW} 0V.

Conclusion

The SPW bitcell architecture combined with a wide back bias range in UTBB FDSOI enables both low operating voltage and fast access time. The low sensitivity of the bitcell I_{OFF} current to changes in body bias enables access time improvement through V_B adjustment. In sleep mode, V_B is set to minimize the bitcell standby leakage current and the data retention voltage. A V_{MIN} of 410mV and a DRV lower than 310mV with a leakage current close to 100fA/bitcell are demonstrated. Key causes of dynamic bitcell failures are analyzed, providing early feedback for both design decisions and process improvement, scalable to finer process geometries.

References:

[1] K. Cheng et al., p. 49, IEDM'09.
[2] O. Weber, et al., p. 58, IEDM'10.
[3] J-P. Noel, et al., Vol. 58, No. 8 p. 2473, TED'11.
[4] Y.-H. Chen, et al., Vol. 47, p. 969, JSSCC'12.
[5] S.O. Toh, et al., p. 35, VLSI'10.
[6] Y. Morita, et al., p. 37, VLSI'10.
[7] O. Thomas, et al., p. 1, SOI-Conference'12.
[8] R. Ranica, et al., p. 210, VLSI'13.
[9] N. Planes, et al., p. 133, VLSI'12.

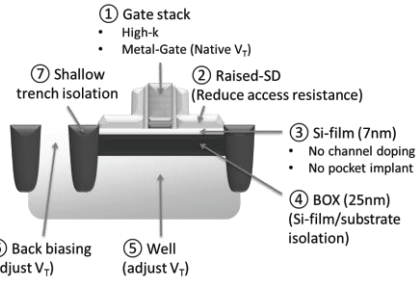

Fig.1: UTBB FD-SOI cross section view. Device V_T is set by the gate stack and adjusted by well doping type [2-3]. Wide V_T tuning is feasible by back-biasing changing the well bias.

V_T	NMOS		PMOS	
	Well type	V_{BS} (V)	Well type	$\|V_{BS}\|$ (V)
RVT	P	0	N	0
LVT	N	0	P	V_{DD}

RVT: Regular-V_T
LVT: Low-V_T

Fig.2: UTBB FD-SOI V_T definition.

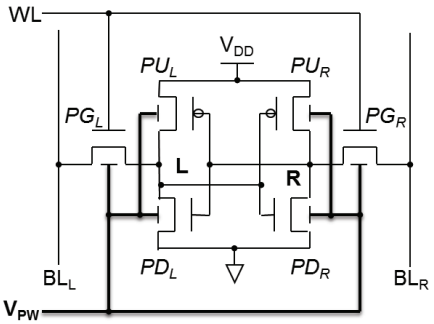

Fig.3: SPW bitcell schematic. Back gate of NMOS (PG, PD) and PMOS (PU) devices are electrically connected by the common P-well.

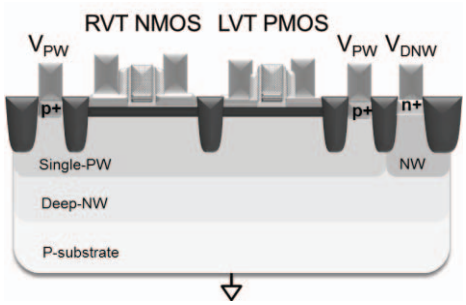

Fig.4: SPW bitcell device cross section view. DNW isolates the PW from the p-substrate enabling wide voltage range PW back biasing.

Back bias (BB)	PD, PG	PU
V_{PW} = 0V (default)	No BB	No BB
V_{PW} > 0V	FBB	RBB
V_{PW} < 0V	RBB	FBB

FBB: Forward-BB → $|V_T|$ reduces
RBB: Reverse-BB → $|V_T|$ increases

Fig.5: SPW bitcell device V_T shift and back bias mode versus V_{PW} considering V_T definition in Fig.2.

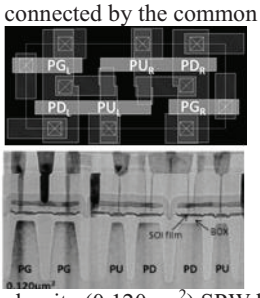

Fig.6: High density (0.120µm^2) SPW bitcell layout and TEM cross section [8]. 28nm High-k metal-gate technology implementing 7nm Si-film relying on 25nm BOX thickness [9].

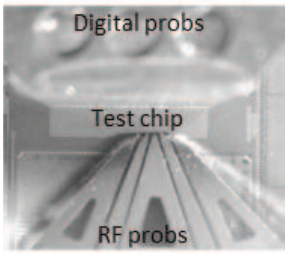

Fig.7: Test chip photograph. Implemented to be testable on wafer during the process development. 25 digital and 2 RF probes are used to bring in and output low and fast signals.

Metric	Definition
RET	Bitcell ability to retain data in retention
RS	Bitcell ability to retain data versus read access time
RA	Bitcell ability to discharge bitline versus read access time
WA	Bitcell ability to flip data versus write acess time

Fig.8: SRAM bitcell metric definitions testable with the test chip.

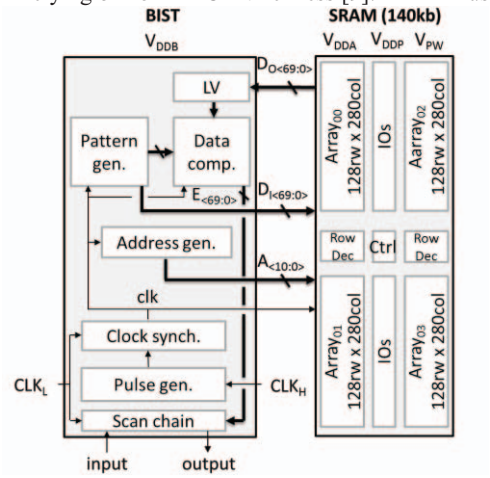

Fig.9: Dynamic characterization module architecture, including a 140kb SPW SRAM macro clocked by an on-chip pulse generator and controlled by a programmable BIST. Input and output are scanned in and out at low clock frequency (CLK_L) while tests can be performed at higher frequency (CLK_H).

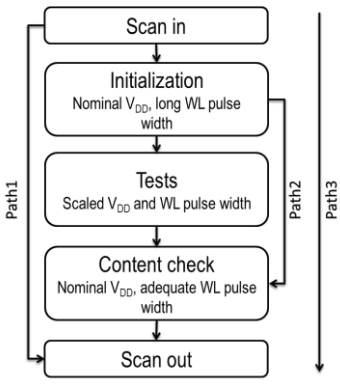

Fig.10: BIST finite state machine:
Path1 – Scan chain test
Path2 – SRAM initialization test
Path3 – SRAM tests

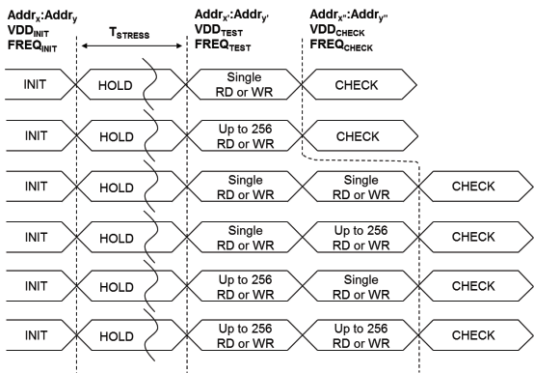

Fig.11: SRAM access patterns for evaluating retention, read, write and timing SRAM failure rate, while considering multiple cycle and electrical stress.

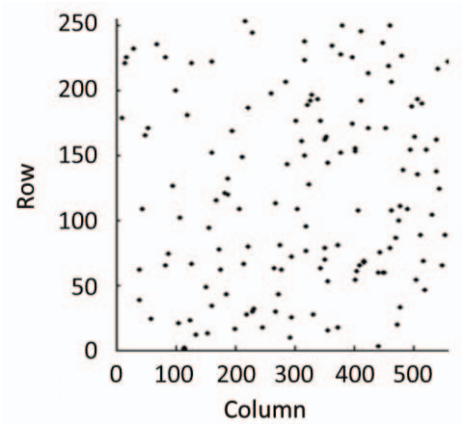

Fig.12: Memory map of RS errors measured at V_{DD}=300mV and 5000ns word-line pulse width. The random distribution of errors confirms that errors measured are caused by the bitcells and not the periphery.

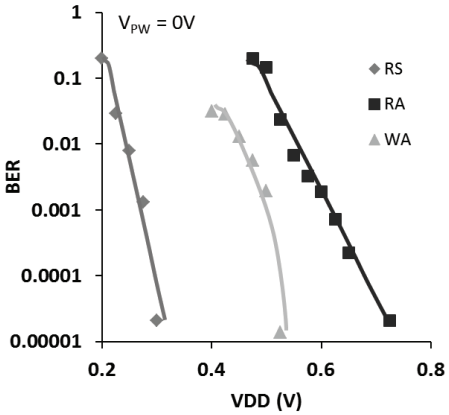

Fig.13: RS, RA and WA BER versus V_{DD} considering a word-line pulse width of 2.5ns. Each metric is measured independently column by column to avoid false error measurements caused by column interleaving.

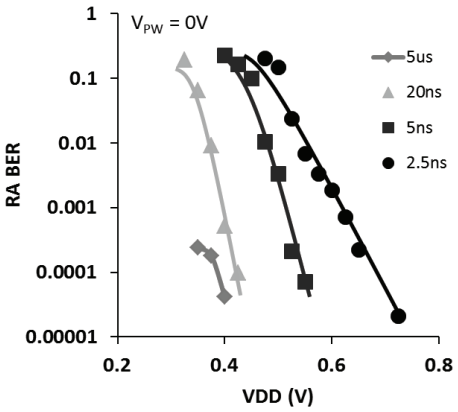

Fig.14: RA BER versus V_{DD} for various word-line pulse widths.

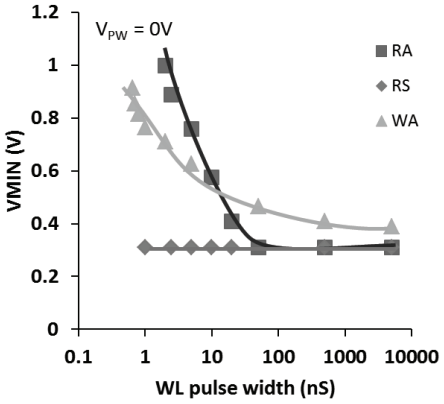

Fig.15: RS, WA, RA V_{MIN} versus WL pulse width. For WL pulse width longer than 10ns V_{MIN} is limited by WA, while for shorter pulse width V_{MIN} becomes limited by RA. RS is not the primary V_{MIN} limiting condition.

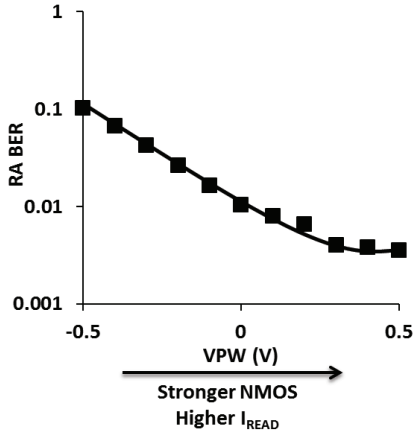

Fig.16: RA BER versus V_{PW} (V_{DD}=500mV, WL pulse width=5ns). V_{PW} increase forward biases the PD PG NMOS devices leading to an over one decade decrease of RA BER due to the increase of bitcell read current enabling faster access time.

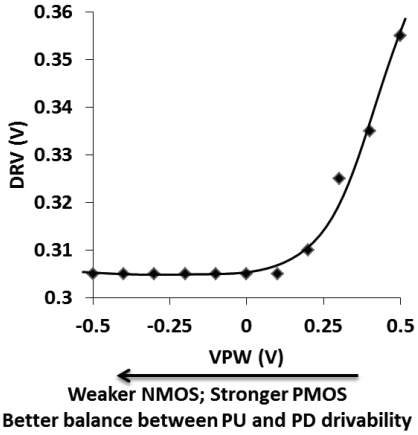

Fig.17: DRV versus V_{PW}. Decreasing V_{PW} balances NMOS and PMOS device strength improving bitcell retention voltage margin. Positive back-bias weakens PU degrading the retention of high logic state, increasing DRV.

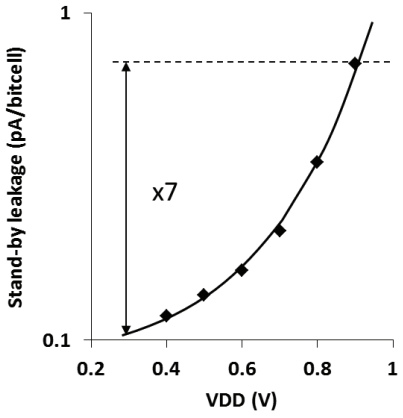

Fig.18: Bitcell stand-by current versus V_{DD} measured at ambient temperature.

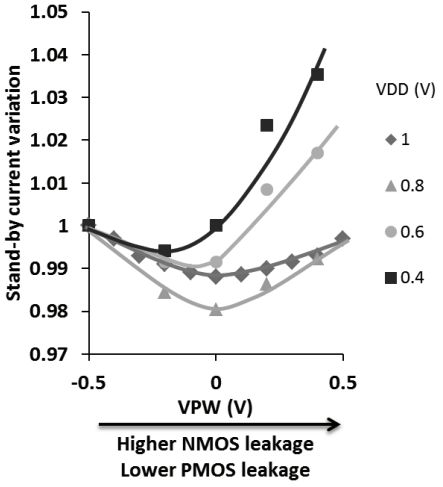

Fig.19: Bitcell stand-by current variation versus V_{PW}. Low impact of V_{PW} on stand-by current due to the leakage current compensation between PMOS and NMOS. Lowest stand-by current is reached when -250mV<V_{PW}<0V.

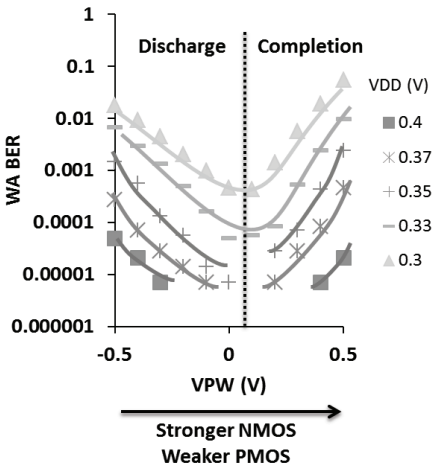

Fig.20: WA BER versus V_{PW} (WL pulse width =5000ns). When V_{PW} < 0, the weak PG/PU ratio causes discharge failures, while for V_{PW} > 0 PU completion fails. Measurements agree with simulation results in [7].