

# A Highly Reconfigurable 400-1700MHz Receiver Using a Down-Converting Sigma-Delta A/D with 59-dB SNR and 57-dB SFDR over 4-MHz Bandwidth

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## Abstract

A highly reconfigurable radio-frequency-to-digital signal converter is presented. Center frequency is precisely defined by a local-oscillator signal, while baseband bandwidth is defined in the digital domain. An SNR of greater than 59 dB across a 4-MHz bandwidth is measured across center frequencies ranging from 400MHz to 1.7GHz. An IIP3 of greater than +19dBm is measured, with an out-of-band 3-dB desensitization level of greater than +1dBm.

## Introduction

Proliferation of various wireless standards as well as the interest in software-defined and cognitive radios have resulted in the need for highly reconfigurable radio-frequency (RF) receivers. This reconfigurable receiver should have flexibility for choosing both a center frequency as well as an appropriate baseband bandwidth.

In this work, we present an RF receiver based on a down-converting sigma-delta (SD) A/D. An input RF signal is down-converted to baseband using a passive mixer within a second-order SD A/D. The SD A/D is built using a passive switched-capacitor filter circuit and is run at a clock rate equal to the center frequency of the RF signal ( $f_{LO}$ ). The system is able to capture a wide bandwidth while simultaneously protected from the folding of signals due to aliasing, except for signals at odd-multiples of  $f_{LO}$  [1]. A feedback SD topology is chosen due to its superior tolerance toward large out-of-band blockers [3].

Final baseband signal selection is performed in the digital domain; therefore change of baseband bandwidth can be easily accommodated by changing digital filter coefficients.

## Circuit Design

Within each of I and Q channels, the input signal is further divided into two paths (Fig. 1). A transconductor (GM) converts an input RF voltage into an output current. The high output impedance of the GM forces the output current to flow through two pairs of MOS switches, both of which are switched at  $f_{LO}$ . During the period when LO signal is high, output current from GM is directed to a set of capacitors in the top path. When LO signal is low, these capacitors are isolated from the input, and the signal is held constant. This two-path scheme indirectly implements a sample-and-hold function for the succeeding switched-capacitor circuits. This scheme also limits the timing jitter sensitivity to only that of the LO signals.

The sampled-and-held signal is then processed by a second-order SD A/D. For each path, two feedback digital-to-analog converters (D/As) are needed. The first D/A, FB1, is time-shared between the two paths and is embedded within the transconductor structure. Both feedback D/As are implemented as return-to-zero D/As in order to avoid inter-symbol-interference. A variable gain range of 12-dB is established by making reference currents for both feedback D/As digitally programmable.

Figure 2 shows the schematic of the combined GM and FB1 circuit. The GM circuit is a two-stage amplifier with a common-source first-stage followed by a folded-cascode second-stage amplifier. A second-stage amplifier is needed in order to boost the output impedance of the amplifier and to provide reverse isolation to the input RF port. The FB1 circuit is current-shared with the cascode amplifier, which is accomplished by replacing the bottom current source of the cascode amplifier with a current-switching D/A. The digital input to

the FB1 circuit is also padded-out to support future work on in-band interference cancellation.

The feedback signal provided by the SD modulator tracks and cancels in-band signals at the output of GM+FB1 circuit. Therefore, this feedback scheme enables the mixer circuit to have a large conversion gain without creating a large distortion due to output compression. Out-of-band signals as well as the SD quantization noise are filtered out by the frequency characteristics of the load impedance. Both of these features help limit the voltage swing at the output of the GM+FB1 circuit, which improves overall system linearity.

The comparator design is particularly challenging due to a small regeneration time as well as the need for a very small input-referred noise due to the lack of front-end gain in the system. The core comparator is adapted from [4]. A gated-diode amplifier [5] with a gain of 8-dB precedes the comparator to improve the input-referred offset and noise of the overall comparator.

Both I and Q channel are implemented in the test chip. An on-chip clock generator circuit takes in an input frequency of  $2xf_{LO}$  and generates I and Q LO signals and all the necessary clock phases.

## Measurement Results

The chip is implemented in a general-purpose 90nm technology with a 1.2V supply voltage. Reported signal bandwidths are for the separate I and Q channels. The measured power consumption includes both channels as well as an input clock buffer. Further power reduction is possible by scaling down the clock generation and distribution circuits.

Figure 6 shows signal-to-noise ratio (SNR) for a constant 4-MHz bandwidth for a center frequency that varies from 200MHz to 1.7GHz. At higher over-sampling ratio (OSR), white noise from the active circuits dominates; while at lower OSR, quantization noise from the modulator dominates. At the lowest-noise gain setting, the activation of the gated-diode amplifier results in a 0.4dB improvement in SNR. Spurious-free dynamic range (SFDR) is limited by the third-order distortion (HD3) of the GM circuit.

Since there is no explicit filtering in the receiver, maintaining linearity as well as resiliency towards large blocking signals are important. An IIP3 of greater than +19 dBm is measured. Desensitization due to out-of-band blockers (Fig. 8) occurs in this system because of modulator over-range (close-in blockers) and saturation of the cascode stage in the GM circuit (far-out blockers). Desensitization due to spurious tone (distortion) is caused by second-order intermodulation product (IM2).

## Acknowledgements

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## References

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- [5] W.K. Luk, R.H. Dennard, *IEEE Trans. Circuits & Systems*, May 2005
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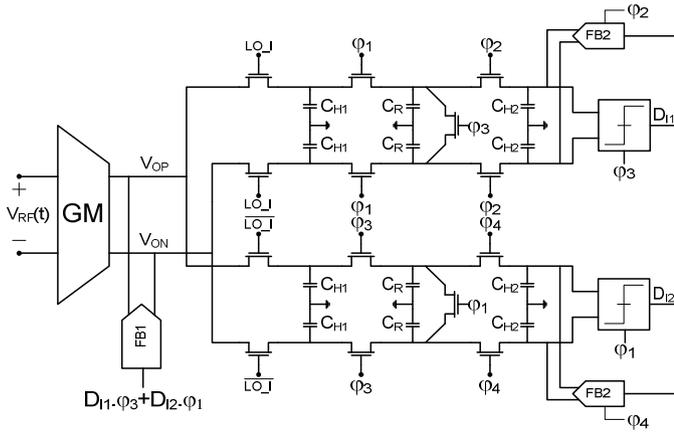


Fig. 1: Simplified schematic for I channel.

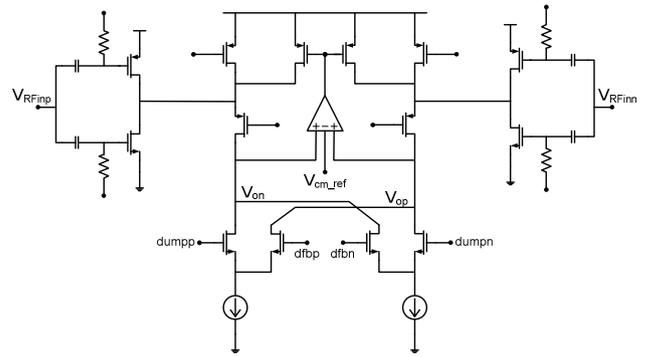


Fig. 2: Transconductor (GM) and 1<sup>st</sup> feedback D/A (FB1).

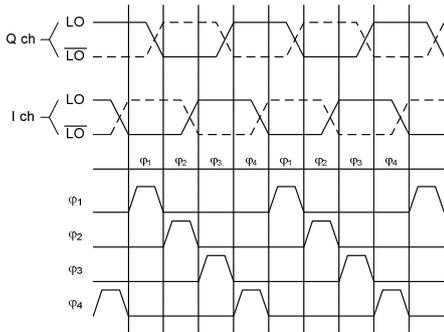


Fig. 3: Timing Diagram.

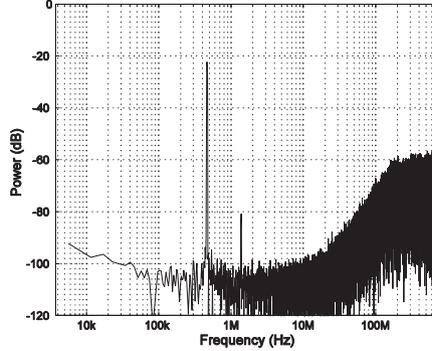


Fig. 4: Spectrum plot, 1.5-GHz center frequency Input signal at 1.5 GHz + 457 kHz.

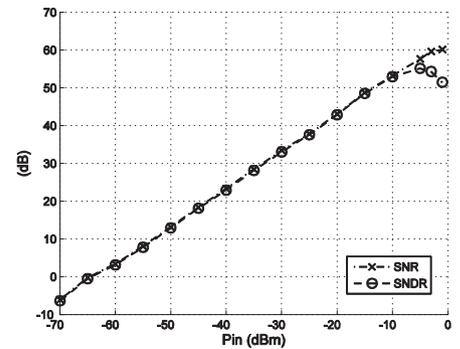


Fig. 5: SNR sweep at 1.5-GHz center freq., 4-MHz bandwidth.

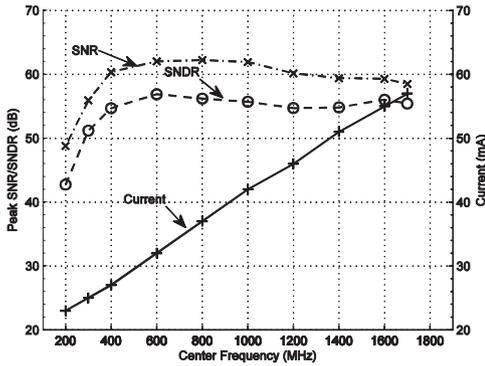


Fig. 6: Center frequency sweep, 4-MHz bandwidth.

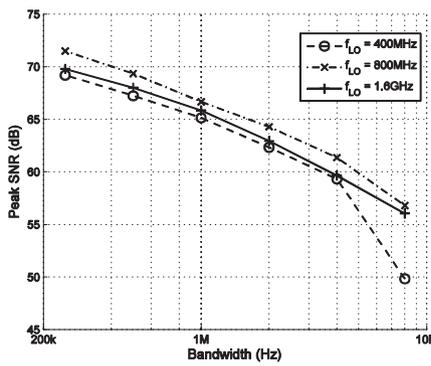


Fig. 7: SNR for variable bandwidths.

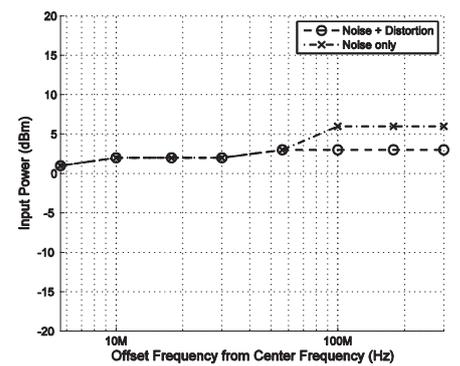


Fig. 8: Out-of-band 3-dB desensitization levels, 4-MHz bandwidth.

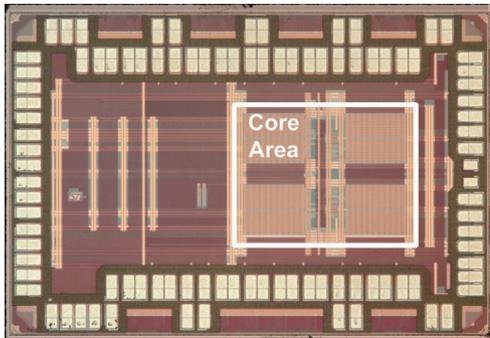


Fig. 9: Die photo.  
Core Area: 1 x 0.8mm  
Chip Area: 2.4 x 1.6mm

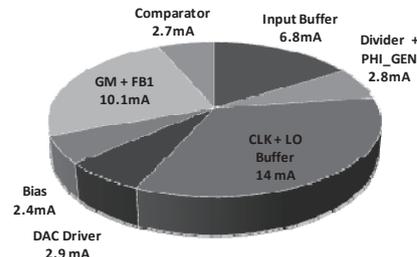


Fig. 10: Power consumption breakdown at 1-GHz center frequency.

TABLE 1: PERFORMANCE SUMMARY

Center Freq.	0.4-1.7GHz
SNR (4-MHz BW)	>59 dB
SNDR (4-MHz BW)	>55 dB
SFDR	57 dB
IIP3	+19 dBm
IIP2	+60 dBm
LO→RF Leakage	-76 dBm
Rejection to signals @ even multiples of $f_{LO}$	> 61dB
Input-referred noise (highest gain setting)	45 nV/rtHz
Technology	GP 90 nm, 7M1P
Supply Voltage	1.2 V
Current Consumption at $f_{LO} = 1\text{GHz}$	42 mA