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A2L-D ESSCIRC - Power Converters

Time: **Tuesday, September 16, 2008, 09:50 - 10:50**
Place **Tinto**
Chair **Erik Bruun,** ***Technical University of Denmark***

A2L-E Temperature and Gas Sensors

Time: **Tuesday, September 16, 2008, 09:50 - 10:50**
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Chair **Andreas Demosthenous,** ***University College London***

A2L-F Delay Locked Loops

Time: **Tuesday, September 16, 2008, 09:50 - 10:50**
Place **Kilsyth**
Chair **Doris Schmitt-Landsiedel,** ***Technical University of Munich***

A3L-D RF Building Block

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A3L-E Unconventional Image Sensors and Circuits

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Chair **Jed Hurwitz, *Gigle Semiconductor***

A3L-F On-chip digital monitors and regulators

Time: **Tuesday, September 16, 2008, 11:20 - 12:50**
Place **Kilsyth**
Chair **Per Larsson-Edefors, *Chalmers University of Technology***

A 15 MHz □600 MHz, 20 mW, 0.38 mm^2, Fast Coarse Locking Digital DLL in 0.13μm CMOS

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Abstract - **A digital delay-locked-loop (DLL) suitable for generation of multiphase clocks in applications such as time-interleaved and pipelined ADCs locks in a very wide (40X) frequency range. The DLL provides 12 uniformly delayed phases that are free of false harmonic locking. The digital control loop has two stages: a fast-locking coarse acquisition is achieved in four cycles using binary search; a fine linear loop achieves low jitter (8.9 ps rms @ 600 MHz) and tracks PVT variations. The DLL consumes 20 mW and occupies a 470 □m X 800 m area in 0.13μm CMOS.**

I. INTRODUCTION

Time-interleaved and pipeline ADC's require generation of multiple clock phases in a very wide operating frequency range with challenging jitter requirements in the upper frequency range. DLLs are often used in these applications, but they face design tradeoffs between the requirements for low jitter, fast locking, wide frequency-range and low power. Low voltage headroom, associated with supply voltages in scaled technologies presents a challenge for analog control loops in a DLL to achieve a very wide locking range. This limitation is solved by using digital control loops that ideally can use longer wordlengths to extend the dynamic locking range [1-11]. Jitter in digital DLL's is determined by the size of the DAC LSB that controls the delay line. However, the interaction of the wide dynamic range control with the delay line dramatically impacts other performance metrics such as the locking time, jitter, power consumption and silicon area.

In this DLL, a novel architecture allows the design to achieve 40X locking range together with fast locking, and low jitter at high frequencies in steady state. This locking range enables a wide set of operating modes as well as the testability of the ADC system that uses it. A 10-bit digital control is used to control the jitter, and the locking range. It is used to adjust the delay of the current-starved inverter based delay line, where the 4 most significant bits (MSB's) coarsely select the frequency range (15MHz – 600MHz using a fast binary search, and a binary-weighted DAC replicated at each delay cell. The 6 least significant bits (LSB's) linearly control the delay elements for a low jitte in steady state. The unit-element LSB DAC is share among all delay cells. This split-control architecture enable the delay adjustment of delay elements with low suppl voltage in the desired operating range. This design als allows for low power consumption and a moderate silicon area for a DLL with 12 clock phases.

II. ARCHITECTURE

Figure 1 shows the basic block diagram of the proposed DLL. The binary search brings the total delay D of the delay line within the locking range, $3T/4 < D < 5T/4$. If $3T/4 < D$ the UNDER signal is activated by the false-locking detection logic, Table 1.

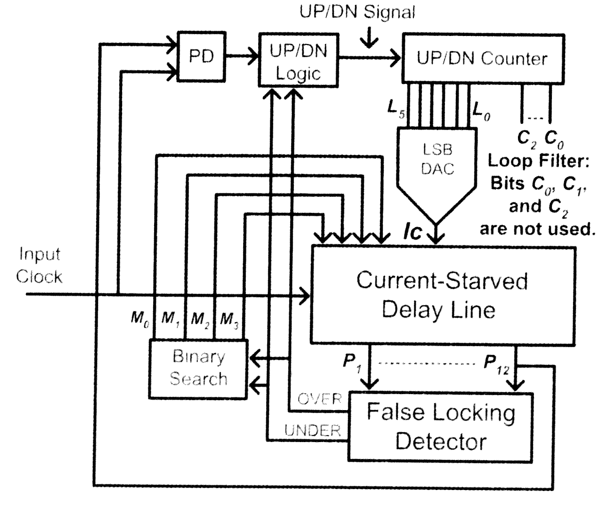

Fig. 1: Block diagram of the DLL.

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Similarly, if $D > 5T/4$, the OVER signal is activated. The UNDER and OVER signals are correctly detected for duty cycles of the input clock from 25% to 75% making this DLL immune to duty-cycle variations.

The binary search machine gets triggered by either an external reset signal or by a sudden change in either the UNDER or OVER signals. This feature makes this DLL to track frequency changes in its entire range of operation which makes it suitable for broadband applications. When the binary search completes, the 6-bit LSB linear loop, whose counter is initialized at mid-range, makes the final fine adjustments to bring the total delay D within one LSB of the desired input clock period T. Only the top 6 bits of the 9-bit counter are used to drive the unit element DAC; the 3 LSBs provide low-pass filtering by slowing down the loop. Discarding the 3 LSBs also lowers jitter in steady state because it averages random up and down signals due to noise. The linear search stays on during the operation to provide compensation for voltage, temperature variations and aging.

The delay line is a chain of 24 current-starved inverters (Fig. 2). Each inverter receives the 4 MSBs from the binary search state machine and adds them to the mirrored current from the unit element DAC driven by the 6 LSB's.

Since a delay cell is the cascade of two of these inverters, the rising and falling times at the delay cell's output will be equal, preserving the duty cycle even if there are mismatches between the p-type and n-type devices of the current starvation sources.

The false locking detector is fully digital [7]. It determines the UNDER and OVER signals based on the delay line phases P1 to P12. Table 1 shows the logic levels of the delay line phases at the rising edge of the input clock.

TABLE 1: FALSE LOCKING DETECTION USING P1-P12 DELAY LINE PHASES

Delay	0.6T	0.76 T	0.8T	T	1.22T	1.29 T	1.33 T	1.67T
P1	0	0	0	0	0	0	0	0
P3	0	0	0	0	0	0	0	0
P5	0	0	0	0	0	1	1	1
P7	0	0	0	0	1	1	1	0
P9	0	0	0	1	0	0	0	0
P10	0	0	1	1	0	0	0	1
P11	0	1	1	1	0	0	0	1
P12	1	1	1	0	0	0	0	1
UNDER		IN LOCKING RANGE					OVER	

The UNDER signal is high if all the phases from P1 to P10 are low. The OVER signal is high if a '...10...' pattern is found in any two consecutive phases from P1 to P8. As it can be inferred from Table 1, the UNDER and OVER signals are safely detected for duty cycles of the input clock from 25% to 75%. In the event that either the UNDER or OVER signals remain active after the binary search finishes, the UP/DN logic disables the phase detector (PD) output, to avoid false locking. Instead, it uses the UNDER or OVER signals to bring the linear loop into a locking range.

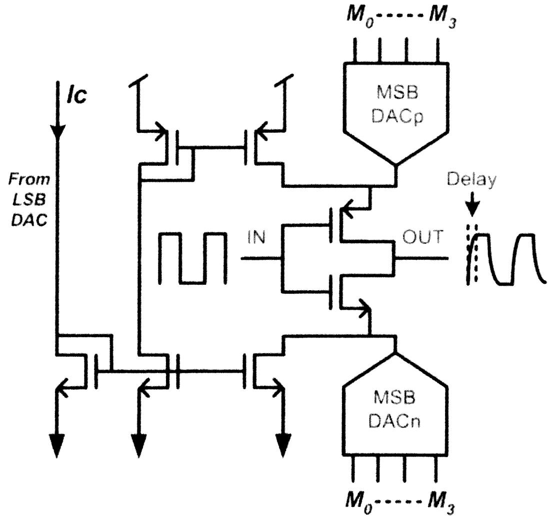


Fig. 2: Current-starved inverter.

The jitter of this DLL topology is inversely proportional to the squared value of the frequency of operation. This result can be derived as follows: for a frequency of operation F_1 that requires a nominal current I_1, where $F_1 = kI_1$, k being a constant that depends on the capacitance of the current starved delay cell and the number of cells that formed the delay line. Assuming linear low-to-high and high-to-low propagation delays, the proportionality constant is given by (1):

$$k \approx \frac{M * Vdd}{C} \text{[V/F]}, \tag{1}$$

where Vdd is the power supply, M is the number of current-starved inverters and C in the total capacitance that loads each inverter. The delay of the delay line is given by

$$T_1 = \frac{1}{kI_1}, \tag{2}$$

and the peak-to-peak jitter will be,

$$\Delta t_1 = \frac{1}{k(I_1 - \Delta I)} - \frac{1}{k(I_1 + \Delta I)}, \tag{3}$$

where ΔI is the current LSB value. Similarly for a frequency that is larger by a factor N, i.e., $F_2 = NF_1 = kI_2 = kNI_1$, the associated jitter is, $\Delta t_2 = \frac{1}{k(I_2 - \Delta I)} - \frac{1}{k(I_2 + \Delta I)}$. Thus, the jitter drop-off when the frequency rises from F_1 to F_2 is given by,

$$\frac{\Delta t_2}{\Delta t_1} = \frac{(I_1 - \Delta I)(I_1 + \Delta I)}{(I_2 - \Delta I)(I_2 + \Delta I)} \approx \left(\frac{I_1}{I_2}\right)^2 = \frac{1}{N^2}. \tag{4}$$

In the prototype chip, the MSB and LSB currents are programmable, which gives flexibility for testing purposes. This also allows adjusting the LSB current to minimize the jitter at lower frequencies.

Replicating the MSB DAC across all the current starved inverters minimized DC current consumption, as only the dynamic current is drawn from these DACs. On the other hand, the LSB DAC current was mirrored to all current cells, since it is much smaller. The DC current in the LSB's corresponds to only the lower 6 LSBs of the total 10 bits in the dual digital control loop; furthermore, current scaling by a factor of 20 lowers the mirrored DC current. This current is scaled up to its nominal value locally at each delay cell where only the dynamic power is consumed.

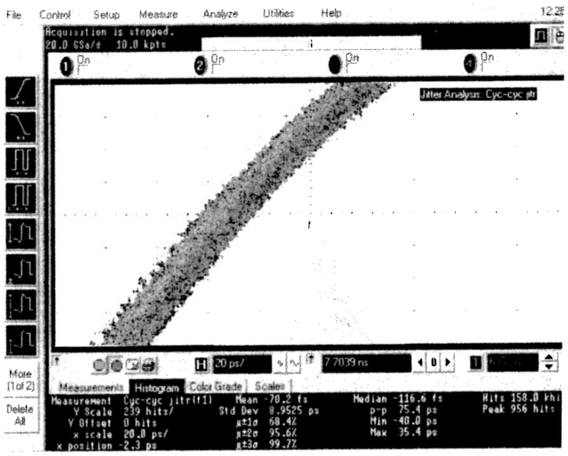
III. IMPLEMENTATION AND TESTING

The DLL has been implemented in a general-purpose, 0.13µm 6M1P CMOS technology. The DLL occupies 470µm × 800µm area. Measured jitter performance is summarized in Table 2 and jitter measurement plot at 600 MHz and 380 MHz are shown in Fig. 3 and Fig. 4, respectively. Five chips were tested with almost the same measurement results. The DLL clock is driven off-chip using LVDS pads, which worsens the jitter by up to 7 ps rms. The actual on-chip DLL jitter variance is expected to be up to $(7\ \text{ps})^2$ better that the squared of the rms values in Table 2. This expected on-chip jitter is also reported in Table 2. The linear control loop can be left running to absorb PVT variations in the locked state. The steady-state jitter produced by the LSB toggling is reduced with increased clock frequency as indicated in Eqn. (4). For frequencies larger than 300 MHz, the jitter produced by the LSB toggling is lower than the intrinsic jitter induced by the electronic noise. At low frequencies, however, the effect of the LSB toggling is higher, as the output will toggle between two phases as shown in Fig. 5. In the worst case, if the edge of the delayed clock gets very close to the input clock, the intrinsic jitter will make the linear loop to toggle between 3 LSBs producing a 3 edge clock eye diagram. As a result, the peak-to-peak jitter can be as big as 2 LSBs. This case is illustrated in the measured eye diagram of Fig. 6.

TABLE 2: RMS JITTER ACROSS THE OPERATING RANGE.

Freq. (MHz)	600	500	400	300	200	150	50	15
Measured rms off-chip jitter [ps]	8.9	8.9	9	9.5	10.2	20.5	100	116[1]
Expected on-chip jitter [ps]	4.1	4.5	5	5.7	7.4	19.2	100	116

[1] An LSB current that is lower than in the other measurements was used here to improve the jitter.



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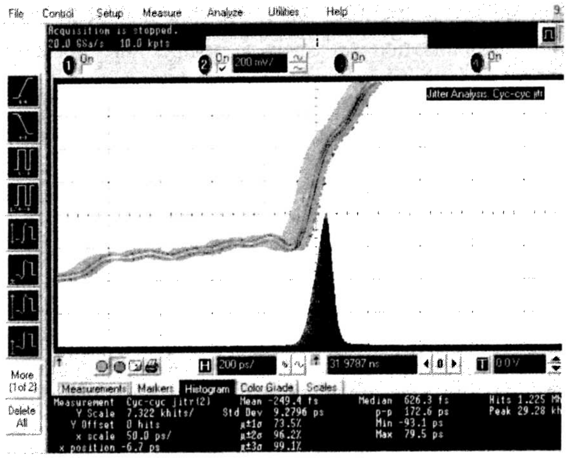
Measurement  Cyc-cyc jitr(f1)    Mean -70.2 fs       Median -116.6 fs      Hits 158.0 kh
    Y Scale  239 hits/        Std Dev  8.9525 ps        p-p  75.4 ps       Peak 956 hits
   Y Offset  0 hits              μ±1σ  68.4%            Min -40.0 ps
    x scale  20.0 ps/            μ±2σ  95.6%            Max  35.4 ps
 x position -2.3 ps              μ±3σ  99.7%
```

Fig. 3: Jitter measurement at 600 MHz.



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Measurement  Cyc-cyc jitr(2)     Mean -249.4 fs      Median  626.3 fs      Hits 1.225 M
    Y Scale  7.322 khits/     Std Dev  9.2796 ps        p-p  172.6 ps      Peak 29.28 k
   Y Offset  0 hits              μ±1σ  73.5%            Min -93.1 ps
    x scale  50.0 ps/            μ±2σ  96.2%            Max  79.5 ps
 x position -6.7 ps              μ±3σ  99.1%
```
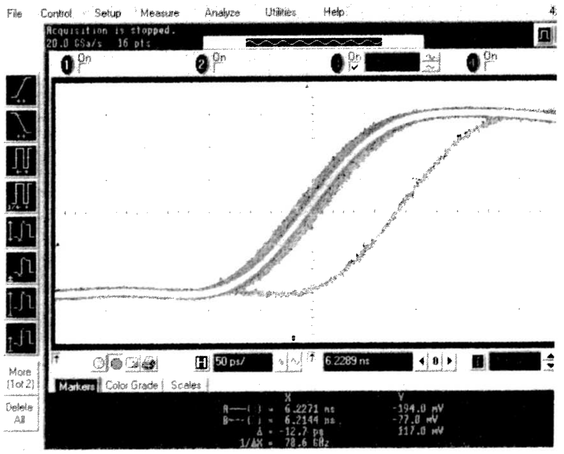

Fig. 4: Jitter measurement at 380 MHz.



```
                 X                  Y
A——( ) =   6.2271 ns          -194.0 mV
B---( ) =   6.2144 ns          -77.0 mV
      Δ =  -12.7 ps            117.0 mV
   1/ΔX =   78.6 GHz
```

Fig. 5: Toggling of the LSB current for low freq operation. The locking frequency is 15 MHz.

TABLE 3: COMPARISON BETWEEN THIS WORK AND RECENTLY REPORTED DLL S

	Tokun.[1]	Song[2]	Kim[3]	Kim[5]	Wang [6]	Bhor.[8]	Wang [9]	Yang[10]	Chang[11]	**This work**
Freq. (MHz)	20-300 (15X)	30-200 (6X)	40-800 (20X)	120MHz-1.8 GHz (15X)	400-600(1.5X)	200-1.2G (6X)	150-550 (3.7X)	40-500 (13.75X)	2-700 (350X)	15-600 (40X)
VDD	2 – 4 V	2.5 V	1.2 V	3.3 V	2.4-3.3 V	1.2 V	1 V	1.8 V	1.4-2.5 V	1.2 V
Power	9 mW	30 mW	43 mW	86.6 mW	9.9 mW	6.1mW	0.37 mW	12.6 mW	23 mW	20 mW
Type	Analog	Digital	Digital	Digital	Digital	Digital	Digital	Digital	Digital	Digital
Area	0.03 mm²	0.66 mm²	0.22 mm²	0.07 mm²	0.7 mm²	0.24 mm²	0.0119 mm²	0.2 mm²	0.88 mm²	0.38 mm²
Jitter (rms)	6.9ps@ 200 MHz	7.1 ps 200 MHz	1.6 ps @ 700 MHz	1.8 ps @ 700 MHz	24.4 ps peak-to-peak	4.6 ps	5.5 peak-to-peak	1.5 ps	17.6 ps peak-to-peak	8.9ps @ 600 MHz
Locking time	1.8 μs	-	-	1 cycles	10 cycles	-	4 cycles	134-14 cycles	32 cycles	4 cycles coarse lock
CMOS	0.30 μm	0.25 μm	0.13 um	0.35 μm	0.35 μm	0.13 μm	65 nm	0.18 μm	0.18 μm	0.13 μm

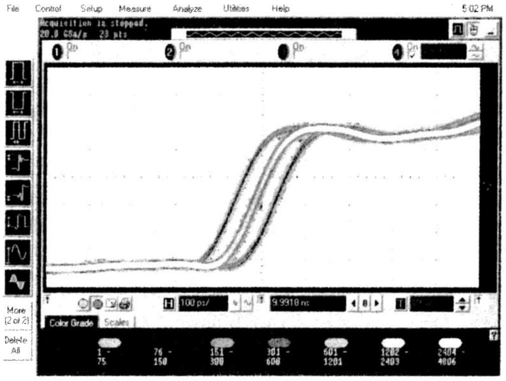


Fig. 6: Measured data showing the case of 3 LSBs flipping in the LSB DAC for low frequency operation. The locking frequency is 15 MHz.

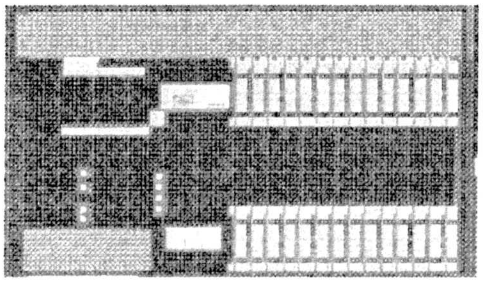


Fig. 7: Chip micrograph. DLL size is 470 m X 800 m.

IV. CONCLUSIONS

This paper presents an all digital implementation of a DLL with a 40X frequency locking range. A dual loop design, consisting in a coarse fast binary search combined with a linear search is proposed. This design achieves a large locking range with fast coarse locking while keeping the jitter and power consumption low. The chip occupies a 470μm X 800μm area and draws 20 mW @ 600 MHz in 0.13μm general-purpose CMOS. The 12 uniform phases of this DLL makes it suitable for providing the phases in applications such as time-interleaved and pipelined ADCs and broadband communications.

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REFERENCES

[1] Y. Tokunaga, et. al., "A 0.03mm/sup 2/ 9mW Wide-Range Duty-Cycle Correcting False-Lock-Free DLL with Fully Balanced Charge-Pump for DDR Interface," IEEE ISSCC 2006, Feb. 6-9, 2006 Page(s):1286 – 1295.

[2] E. Song, et. al., "A Reset-Free Anti-Harmonic Delay-Locked Loop Using a Cycle Period Detector," IEEE JSSC, vol. 39, no. 11, pp. 2055-2061, Nov. 2004

[3] Y-S. Kim, et. al., "A 40-to-800MHz Locking Multi-Phase DLL" IEEE ISSCC 2007, Feb. 11-15, 2007 Page(s):306 – 307.

[4] J-S. Wang, et. al., "An Ultra-Low-Power Fast Lock-in Small-Jitter All-Digital DLL," IEEE ISSCC 2005, Feb. 6-10, 2005 Page(s):422 – 423.

[5] J-H. Kim, et. al., "A CMOS DLL-Based 120MHz to 1.8 GHz Clock Generator for Dynamic Frequency Scaling," IEEE ISSCC 2005, Feb. 6-10, 2005 Page(s):516 – 517.

[6] Y-J. Wang, et. al., "All-Digital Delay-Locked Loop/Pulsewidth-Control Loop With Adjustable Duty Cycles," IEEE JSSC, vol. 41, no. 6, pp. 1262-1274, Jun. 2006.

[7] Y. Aibara, et. al., "A Novel False Lock Detection Technique for a Wide Frequency Range Delay-Locked Loop," IEICE 2006 E89-A(2):385-390

[8] P. Bhoraskar, Y. Chiu, "A 6.1-mW dual-loop digital DLL with 4.6-ps RMS jitter using window-based phase detector," ASSCC '07, 12-14 Nov. 2007 Page(s):79 – 82

[9] J-S Wang, C-Y Cheng, Y-C Liu, Y-M Wang, "A 0.67μW/MHz, 5ps jitter, 4 locking cycles, 65nm ADDLL, ASSCC '07, 12-14 Nov. 2007 Page(s):300 – 303

[10] R.-J. Yang, S.-I Liu, A 40–550 MHz Harmonic-Free All-Digital Delay-Locked Loop Using a Variable SAR Algorithm," ," IEEE JSSC 2007, vol. 42, no. 2, Page(s): 361-373

[11] H-H Chang, S-I Liu, A wide-range and fast-locking all-digital cycle-controlled delay-locked loop," IEEE JSSC 2005 vol. 40, no. 3, Page(s): 661-670