A 1.2V, 10.8mW, 500kHz Sigma-Delta Modulator with 84dB SNDR and 96dB SFDR

Cheongyuen W. Tsang[1], Yun Chiu[2], Borivoje Nikolic[1]
[1]University of California, Berkeley, USA
[2]University of Illinois, Urbana-Champaign, USA

Abstract

A 1.2V switched-capacitor sigma-delta modulator achieves 96dB peak SFDR and 84dB peak SNDR at 1MS/s in a 0.13µm 6M1P general-purpose CMOS process. The high linearity is achieved by using high-gain op-amps and boot-strapped sampling switches. The power dissipation is 10.8mW at 64MHz clock frequency, excluding the voltage references.

Introduction

The demand for wide bandwidth (BW), high dynamic-range (DR) communication systems drives the development of ADCs with higher sampling rates and higher resolutions, while maintaining the requirement for low power consumption. Designing ADCs in deeply scaled-CMOS process enables their integration with digital baseband circuits to provide a low-cost SoC solution. Although offering higher switching speeds, scaled-CMOS processes present serious challenges to precision analog designs. For instance, scaled transistors have lower intrinsic voltage gain, making it difficult to design low power high-gain amplifiers; the reduced supply voltages also limit the amplifier output swing, which in turn, affects the DR of the ADC. This work demonstrates a switched-capacitor sigma-delta modulator that achieves 84dB SNDR, 84dB DR, 96dB SFDR, and a 500kHz BW, with a low power consumption of 10.8mW in a 1.2V 0.13µm digital CMOS, using single-bit, 2-1 MASH topology. Gain-boosted amplifiers and bootstrapped sampling switches are employed to improve the linearity of the modulator.

Modulator Architecture

With low signal levels, limited by the 1.2V supply, the capacitors need to be sized up substantially to maintain a high DR, in kT/C noise limited designs: every 6dB increase in SNR quadruples the power consumption. Therefore, it is critical to strike a balance between the architecture and circuit topologies to meet design specifications at low supply voltages. Sigma-delta ADCs can employ either single-bit [1] or multi-bit quantizers [2]. To lower distortion, multi-bit quantizers typically require dynamic element matching or calibration for the DACs, which increases the design complexity and requires additional power and area. To avoid this added complexity, a single-bit topology was chosen. A 2-1 MASH sigma-delta architecture, formed by cascading a second- and a first-order modulators is inherently stable and achieves a third-order noise shaping. With an OSR of 64, this architecture can achieve a signal-to-quantization noise ratio (SQNR) of over 100dB.

Circuit Design

In sigma-delta ADC design, the input-referred noise for the first integrator is not noise-shaped, and directly subtracts from the noise budget; thus the noise requirement for the first integrator is the most stringent. The noise requirements of the later stages are much relaxed, which indicates that an optimal low-power design should have the sizes of the stages tapered. The input-referred noise of the modulator in Fig. 1 is given by [3]:

$$S_{N,electronic} = \frac{S_{N1}}{M} + \frac{\pi^2}{3a_1^2 M^3} S_{N2} + \frac{\pi^4}{5a_1^2 a_2^2 M^5} S_{N3} \quad (1)$$

where S_{Nj} is the input-referred noise of the j-th integrator ($j = 1, 2, 3$) and M is the oversampling ratio. Limited by the 1.2V supply, the gain coefficients (a_1, a_2, f_1, f_2, etc.) of the integrators (Fig. 1) are optimized to prevent overloading [3]. By using Eq. (1), approximately 90%, 9% and 1% of the noise budget is allocated to the first, second, and third integrators, respectively. Sampling capacitors of the first integrator (shown in Fig. 2) are 1pF, while those of the other two integrators are scaled down to reduce the power consumption.

Finite OTA dc gain causes noise leakage in the modulator, resulting in SNR degradation. Although calculations and behavioral level simulations show that a linear dc gain of 700 is adequate, higher dc gain is desirable to suppress harmonic distortion. Thus, amplifiers with gain higher than 80dB are used in this design (Fig. 3). The gain-boosting technique [4] allows the OTA to achieve the same high dc gain as that of a 2-stage amplifier, while maintaining the wide BW as that of a single-stage folded-cascode amplifier. The folded-cascode OTA with gain-boosting is more power-efficient than a 2-stage architecture because it does not require frequency compensation. Simulated gain of the first OTA is about 90dB at maximum $1.4V_{pp}$ output swing over all process corners and the unity-gain BW is 300MHz. A switched-capacitor common-mode feedback circuit centers the output common-mode voltage at mid-rail (0.6V) to allow a balanced output voltage swing. The bias currents of the later OTAs are scaled down with the capacitor sizes. To achieve high linearity, the clock bootstrapping technique [5] is adopted to keep the on-resistance of the input switches signal independent. This technique avoids the added loading of the PMOS devices in the complementary switches, providing a high input BW.

Prototype Results

The prototype core area is $1.51mm^2$ (Fig. 4) and the die including the pads occupies $2.52mm^2$. The full-scale input voltage of this modulator is $1V_{pp}$, and the references are 1.2V and 0V. Fig. 5 plots the measured FFT spectrum of a 200kHz input signal with 64MHz sampling frequency. Fig. 6 plots the measured SNDR vs. the input level at 200kHz. The peak SNDR is 84dB with a full-scale input. The DR is also 84dB. The peak SFDR is 96dB. For 300kHz and 400kHz input frequencies, the peak SNDR is still 84dB. Table I summarizes the performance of the experimental chip. The FOM ($FOM = P/2/BW/2^{ENOB}$) of 0.83pJ/conversion-step of this work compares favorably to previously published high BW, high DR switched-capacitor sigma-delta modulators (Fig. 7).

Acknowledgements

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References

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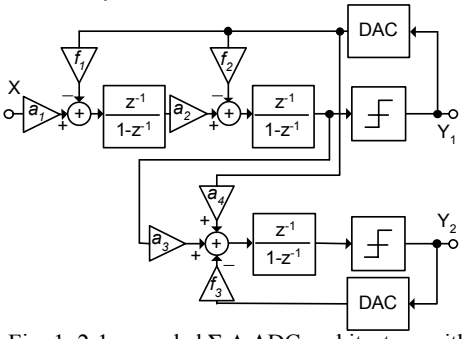

Coeff.	Value
a1	0.25
f1	0.25
a2	0.4
f2	0.25
a3	1
a4	0.1
f3	0.2

Fig. 1: 2-1 cascaded Σ-Δ ADC architecture with scaled coefficients.

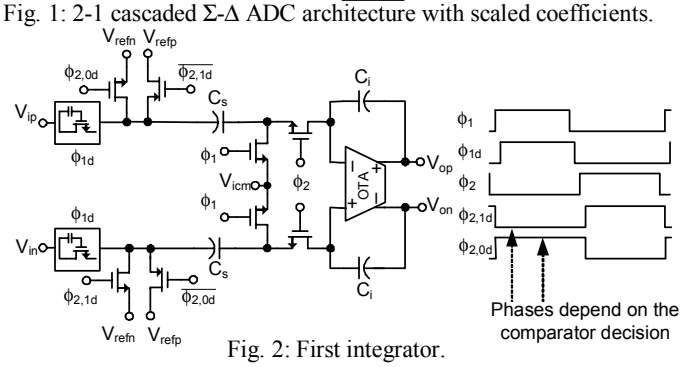

Fig. 2: First integrator.

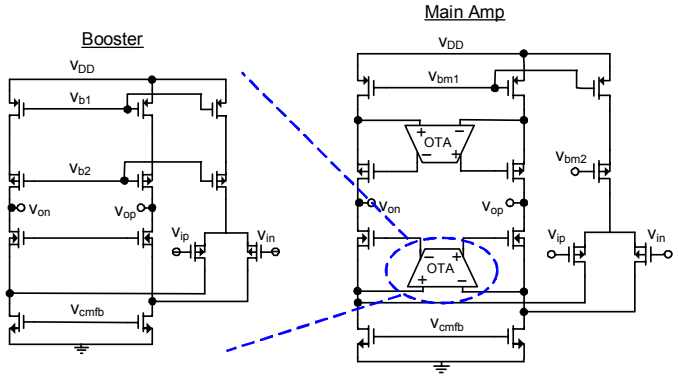

Fig. 3: Gain-boosted operational transconductance amplifier.

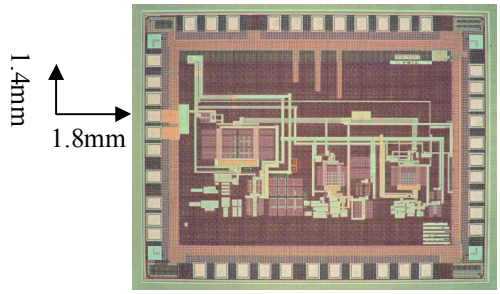

Fig. 4: Chip micrograph.

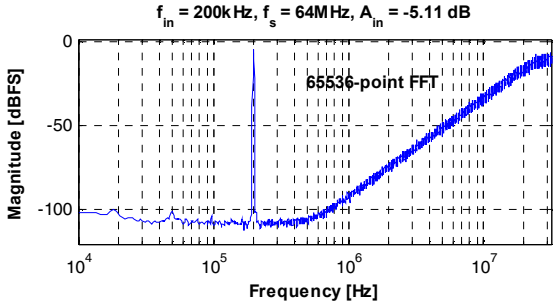

Fig. 5: Measured FFT plot of a -5.11dBFS signal.

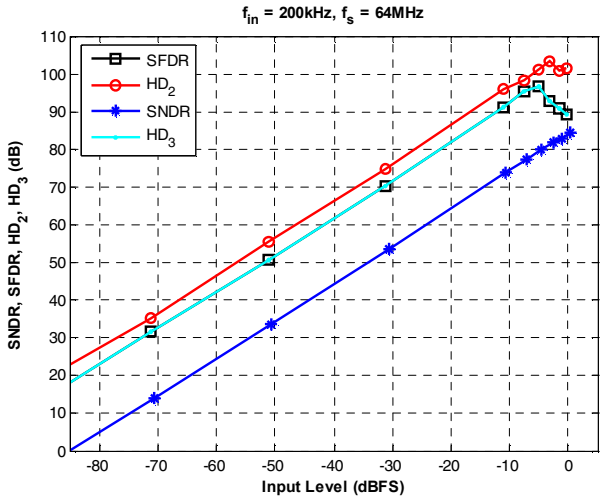

Fig. 6: SNDR, SFDR and harmonic distortion (HD) vs. input level.

TABLE I. PERFORMANCE SUMMARY

Sampling Frequency	64MHz
Oversample Ratio(OSR)	64
Signal Bandwidth (BW)	500kHz
References	1.2V/0V
Maximum Input	$1V_{pp}$
Dynamic Range	84dB
Peak SNR/SNDR	84dB/84dB
Peak SFDR	96dB
Supply Voltage	1.2V
Process Technology	0.13µm 6-metal CMOS
Power(excluding reference)	10.8mW

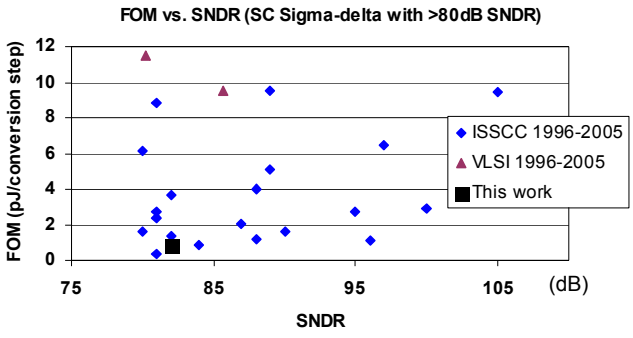

Fig.7: A comparison of ΣΔ modulators published at ISSCC and VLSI Symp. in 1996-2005 with $FOM = Power/2^{ENOB}/2/BW$.