2006 IEEE International SOI Conference Proceedings

FinFET SRAM with Enhanced Read / Write Margins

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Introduction

Increased transistor leakage and performance variation present challenges for scaling of conventional six-transistor (6-T) SRAM cells. It has been recently shown that advanced transistor structures such as FinFETs [1] are more scalable and that FinFET-based 6-T SRAM cell designs offer improved static noise margin (SNM) with reduced variability, as compared with planar bulk-Si SRAM cells [2]. Further, by leveraging the capability of the FinFET to be operated in back-gate (BG) mode (in which the gate electrodes on either side of the fin are separated and independently operated), dramatic improvement in cell read margin can be achieved with no layout area penalty by using dynamic feedback on the pass-gate (PG) transistors (Fig. 1) [2]. In this work, the impact of this pass-gate feedback (PGFB) technique on cell write-ability is examined, and gate workfunction (Φ_m) tuning for optimization of the trade-off with read margin is discussed. To further improve cell write-ability, the p-channel pull-up devices can also be operated in BG mode, with their back gates driven by a separate write word line. This pull-up write gating (PUWG) technique is effective for maintaining larger than 6 standard deviations yield down to 0.4V V_{DD} without area penalty, making FinFET-based 6-T SRAM compelling for high-density memory applications.

Methodology

A pseudo-analytical model for FinFET *I-V* characteristics was fit in all regions of operation for DG and BG operating modes to 2-D device simulations [3] and used to investigate SRAM operation. Nominal dimensions are given in Fig. 1. Figs. 2 and 3 verify that this model fits well mixed-mode simulations for SNM and the write-ability current I_W (defined in [4]). For the yield analyses, independent, Gaussian variations in L_g and T_{Si} were considered, with σ_{Lg}= σ_{Tsi}=1.54nm. The yield of a cell is estimated in the number of standard deviations (cell sigma) to the most probable point of failure (SNM=0 or I_W=0) using an iterative, sensitivities-based approach.

Results and Discussion

Fig. 2 illustrates nominal SNM over a range of V_{DD} for a conventional 6-T FinFET SRAM cell and a cell with pass-gate feedback (PGFB), as illustrated in Fig. 1. With feedback, the pass-gate transistor on the node storing a '0' is weakened, reducing its ability to pull up the storage node during a read operation. As a result, the pass-gate cannot linearize the lower shoulders of the butterfly curves, as in a conventional design (inset), and higher SNM is achieved. Although a higher workfunction can be used to improve SNM, it is less effective than PGFB at high V_{DD}.

Additionally, a larger Φ_m will degrade write-ability by increasing the V_T of the pass-gate transistors and lowering that of the pull-ups (Fig. 3). This effect is most significant at low V_{DD}, where a larger Φ_m can keep the pass-gate device in subthreshold operation. The PGFB technique allows for lower Φ_m and therefore higher I_W at low V_{DD}; however, I_W is limited at high V_{DD} by the reducing gate drive on the pass-gate as the cell switches (Fig. 4).

A further benefit of the low Φ_m is that the V_{CL} bias at the I_W point is larger (Fig. 3, inset). At low V_{DD}, this bias approximately scales with V_{DD}. The larger V_{CL} results in smaller gate drive and the equivalent of a degraded subthreshold swing for the PU5 transistor. This is illustrated in Fig. 4, where the crossing of the PG and PU I-V curves roughly corresponds to the minimum V_{DD} at which the cell is write-able ($I_W > 0$). Since the effects of a small T_{Si} variation in PG3 or PU5 will shift the respective I-V curve horizontally, the amount by which the crossing moves gives a rough approximation of the slope of the I_W yield vs. V_{DD} curve. The flatter PU5 curve of the PGFB design suggests a flatter yield vs. V_{DD} curve at low V_{DD}. The complete yield projection considering possible L_g and T_{Si} variations for all six transistors confirms this result (Fig. 5).

Just as feedback can be used to weaken the pass-gate transistor during a read operation, it is possible to weaken the pull-up transistors during a write operation using a write wordline (WWL) as one of the gates on each pull-up. As illustrated in Fig. 6, the shared WWL contact can be added without increasing cell area, but the routing may require an extra layer of metallization. During a write operation, V_{WWL}=V_{DD} weakens the pull-up transistor. At all other times, $V_{WWL} < V_{DD}$ will pull out the upper shoulders of the butterfly curves (Fig. 7), complementing the effect of PGFB. Fig. 8 illustrates enhanced I_W for the pull-up write-gating (PUWG) case, when Φ_m is chosen for 180mV SNM at V_{DD}=0.7V. The PGFB and PUWG techniques can be combined to improve I_W further through lower Φ_m.

The bias to which WWL steps down after a write operation determines the range of Φ_m that meets a given SNM target (Fig. 9). With PGFB, the range is much larger, enabling low Φ_m at moderate biases. A large ΔV_{WWL} turns both PMOS transistors on, degrading SNM. To maintain high yield at low V_{DD}, ΔV_{WWL} should be chosen away from its maximum. Fig. 10 illustrates high nominal SNM for PGFB+PUWG at V_{WWL}=0.4. At very low V_{DD} the nominal and yield for SNM is highest due to the complementary effects on the butterfly curves (Figs. 10 & 11). The I_W yield is highest for this combination as well, allowing for six sigma yield at 0.4V (Fig. 12).

Conclusions

FinFET-based SRAM designs with dynamic feedback and write word line gating are shown to have improved read and write performance and higher projected yield, without area penalty. PGFB enables greater write-ability at low V_{DD} by allowing for low Φ_m. PUWG allows for further write-ability improvement by weakening the PMOS transistors during a write operation. Combined, these techniques enable continued 6-T SRAM scaling.

References

[1] N. Lindert *et al.*, *DRC*, 2001, pp.26-27.
[2] Z. Guo *et al.*, *ISLPED,* 2005, pp.2-7.
[3] Taurus Device v.2005.10 (Synopsys, Inc.)
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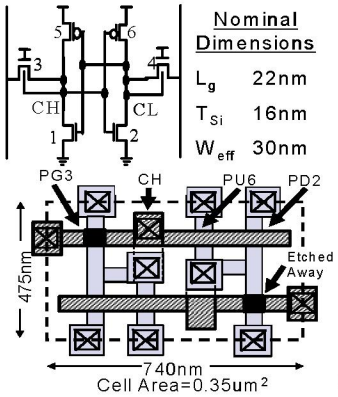

Fig. 1. A 6-T FinFET SRAM in the pass-gate feedback (PGFB) configuration [1]. The back gate of each PG device is connected to its respective storage node.

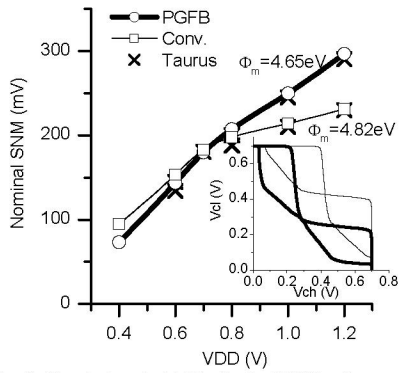

Fig. 2. Nominal read stability for the PGFB and conventional FinFET SRAM cells with Φ_m values chosen to give 180mV at V_{DD}=0.7V. The improved read stability of the PGFB at higher V_{DD} comes from the weakened pass-gate, which pulls out the lower shoulders of the butterfly curves (inset).

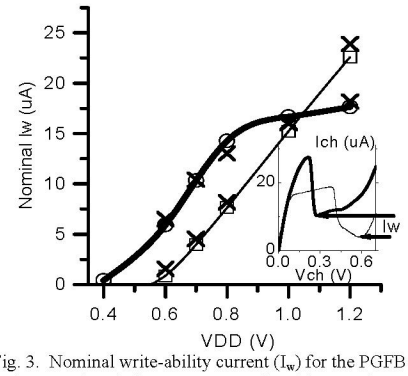

Fig. 3. Nominal write-ability current (I_w) for the PGFB and conventional FinFET SRAM cells with Φ_m values as in Fig. 2. I_w is defined as the minimum of the N-curve (inset) after the peak. The improvement in PGFB I_w at low V_{DD} is largely attributable to the lower Φ_m; however, at higher V_{DD}, the feedback limits the PG current and degrades write-ability.

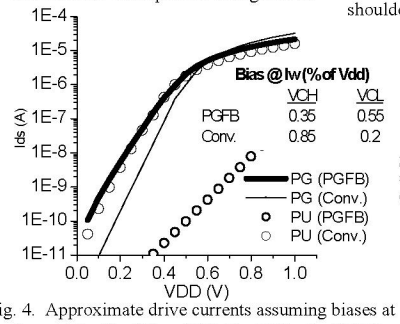

Fig. 4. Approximate drive currents assuming biases at the I_w point for the PG and PU. The PU in the PGFB case appears to have a degraded subthreshold swing because of the higher V_{CL}/V_{DD} ratio. The ratio of the PG and PU slopes can be used to approximate the slope of the yield vs. V_{DD} curve (Fig. 5).

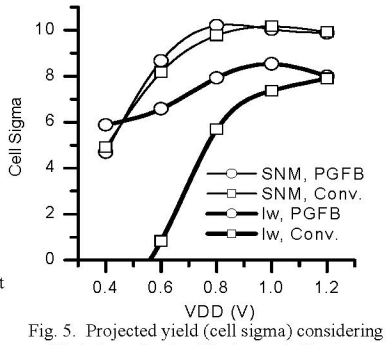

Fig. 5. Projected yield (cell sigma) considering SNM and I_w independently. The large yield enhancement of PGFB I_w at low VDD enables 6-sigma yield at 0.5V. Parameter variation $\sigma_{Lg} = \sigma_{TSi}$ = 1.54nm.

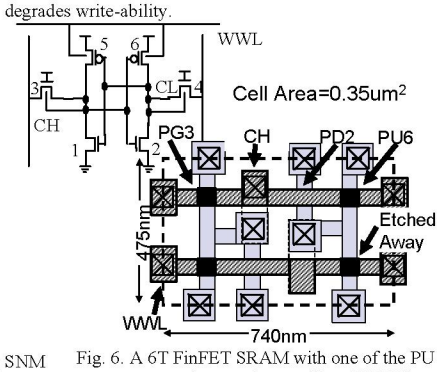

Fig. 6. A 6T FinFET SRAM with one of the PU gates connected to a write wordline (PUWG). This modification can be combined with the PGFB design, without area penalty.

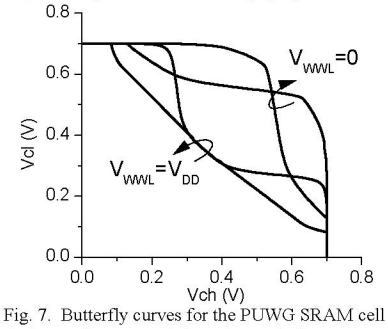

Fig. 7. Butterfly curves for the PUWG SRAM cell design. When WWL is low, the PU leaks current and the top shoulders of the curves are pulled out. This effect can complement that of PGFB on the lower shoulders.

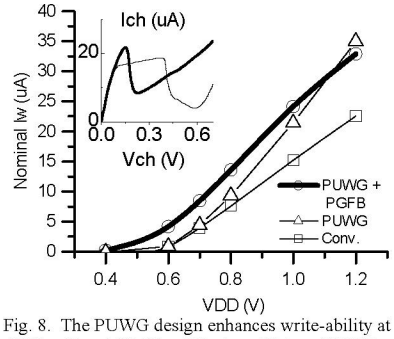

Fig. 8. The PUWG design enhances write-ability at all V_{DD} (Φ_m=4.87eV), while the addition of PGFB enables a lower Φ_m (4.67eV) for further improvement at very low V_{DD}.

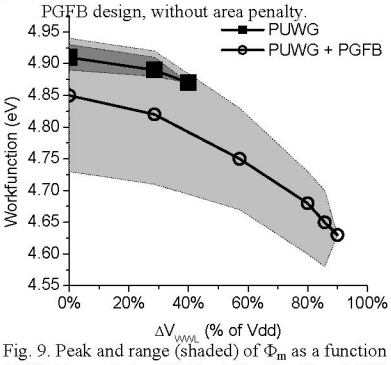

Fig. 9. Peak and range (shaded) of Φ_m as a function of WWL bias such that SNM > 180mV at V_{DD}=0.7 V. With PGFB, a much lower Φ_m is achievable, which improves write-ability. Above 85% V_{DD}, the WWL gate controls the PU current, sharply degrading SNM.

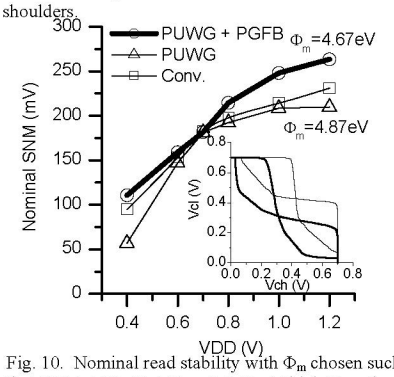

Fig. 10. Nominal read stability with Φ_m chosen such that SNM=180mV at V_{DD}=0.7 V. At high V_{DD}, the effect of PGFB on the butterfly curves complements that of PUWG (inset), resulting in greater SNM.

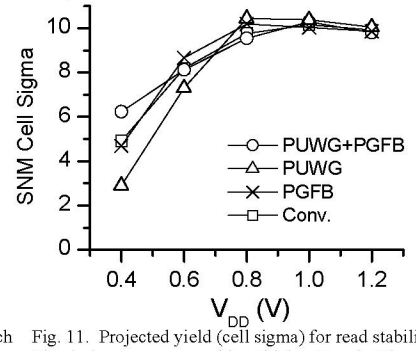

Fig. 11. Projected yield (cell sigma) for read stability. The designs are comparable at higher V_{DD}, but the combination of PUWG and PGFB provides for higher yield at lower V_{DD}.

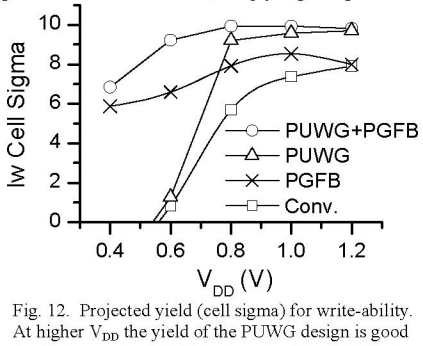

Fig. 12. Projected yield (cell sigma) for write-ability. At higher V_{DD} the yield of the PUWG design is good due to the weakened PU device. For V_{DD} < 0.4V, the combination PUWG+PGFB design achieves greater than 6 sigma yield due to its lower Φ_m.