Measurements and Analysis of Process Variability in 90nm CMOS

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Abstract

Process variability in deeply scaled CMOS has both random and systematic components, with a varying degree of spatial correlation. A test chip has been built to study the effects of circuit layout on variability of delay and power dissipation in 90nm CMOS. The delay is characterized through the spread of ring oscillator frequencies and the transistor leakage is measured by using an on-chip ADC.

1. Introduction

Increased process parameter variability has been perceived as one of the major roadblocks to further technology scaling [1]. Presently, the variability is captured in the design by using simulation corners, which correspond to the values of certain process parameters that deviate by 3 standard deviations from their typical value. The variations are generally characterized as within-die (WID), die-to-die (D2D) and wafer-to-wafer (W2W) [2]. Variation of process parameters can be systematic or random, spatially or temporally correlated. Sources in the variability are in the transistors, interconnect, and in the operating environment (supply and temperature) [3]. Device parameters vary systematically because of deviations in nominal widths and lengths due to exposure and etching, variation in film thicknesses (oxide thickness, gate stack), and variation in dose of implants. Random device parameter fluctuations stem from line-edge roughness [4], Si/SiO_2 and poly-Si interface roughness [5] and doping fluctuations [6].
The corner-based design approach treats all variations as being WID, with all devices on a chip being correlated. The spread of corners is increasing with technology scaling, which makes it challenging to simultaneously satisfy performance, power and parametric yield requirements. In order to better account for the variability in the design process, it is necessary to distinguish systematic shifts in parameter values from truly random ones. Simultaneously, it is important to determine the spatial correlation distance of each of these parameters [7]. While some of these relationships are generally known at the process level, they are hardly visible to the designer.
The goal of this paper is to quantify systematic and random components of variability in scaled CMOS by analyzing the measured data.

2. Lithography-Induced Variations

Present lithography systems employ step-and-scan method, where the stepping is used to move the wafer between major exposure fields. Within an exposure field, the mask pattern is projected through a slit of light onto a wafer [8].
In sub-wavelength lithography, the effective length of a printed gate depends on its neighborhood [9-11]. Polysilicon (polySi) lines with varying pitch will have different effective channel lengths. Isolated lines expose the resist with higher light intensity, resulting in shorter channel lengths, as illustrated in Figure 1. Dense lines also have higher depth of focus, and are more immune to defocusing of the optical system [12]. Optical proximity correction techniques in the mask processing add sublithographic assist features to control the printed critical dimensions; however, their effect is limited due to shallow depth of focus.
Lens imperfections are often described through aberrations, Figure 2. Aberrations create optical path differences for each pair of rays through the imaging system. Effects such as astigmatism and spherical aberrations cause differences in exposed patterns at the level of a reticle.
Coma effect [13] is a lens aberration due to lens imperfection, which may cause two identical gates surrounded with non-symmetrical features to print differently from each other [14].
Flare presents the effect of scattering and reflections of light through the projection system that cause variations in the effective CDs, Figure 3. In general, the amount of flare is dependent on the local pattern density in the mask [14].

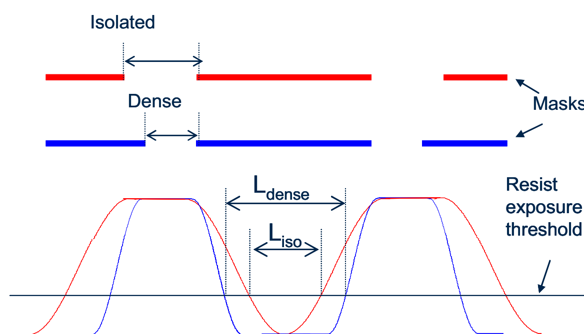

Figure 1: Isolated and dense lines.

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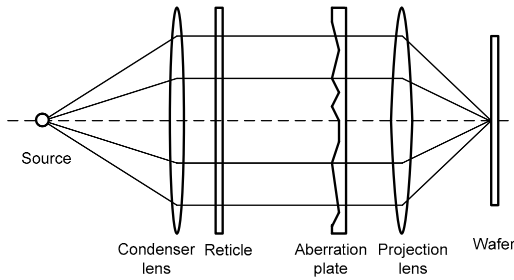

Figure 2: Lens imperfections.

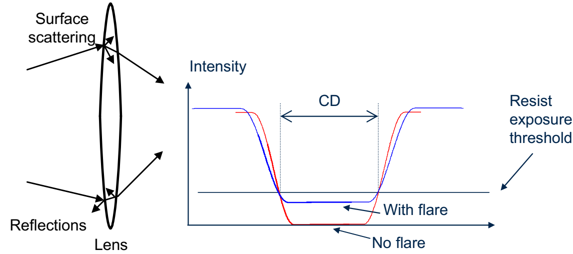

Figure 3: Effect of flare.

Proximity effects, aberrations, and flare are usually not captured in the design process, and induce layout-dependent systematic variations in the design.

3. Test chip

To evaluate the characteristics of lithography-induced variations, a test-chip in a general-purpose 90nm CMOS technology has been built, which measures ring-oscillator (RO) frequencies and transistor standby leakage currents (I_{LEAK}) of an array of test-structures [15].
The chip contains an array of 10×16 tiles [16-18], occupying $1\text{mm} \times 1\text{mm}$ area. Each tile has twelve 13-stage ring oscillators (ROs) and 12 transistors in the off-state, each with a different layout (Fig.4). The transistors consist of single poly finger, as well as a stack of three fingers. PolySi pitch is varied in the test structures to capture the effect of channel length variations. PolySi orientation, together with the properties of the two-dimensional tile array, are used to determine the effects of correlation. Non symmetrical features target measurements of the coma effect. Metal coverage is also varied in the layout to investigate the effects of anneal [19].

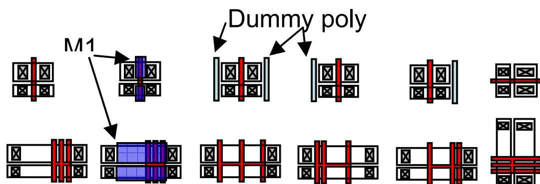

Figure 4. Layout variations in the test chip.

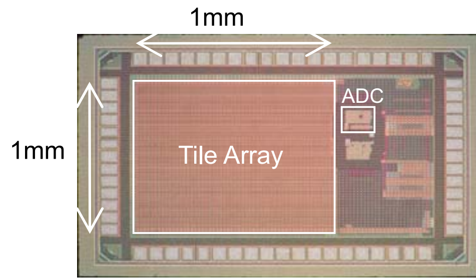

Figure 5. Test chip die photo.

The test chip shown in Figure 5 includes frequency dividers and an on-chip single-slope analog-to-digital converter for leakage current measurements.

4. Measurement results

Measured data shows several important trends. The largest impact of layout on performance variability has the gate polySi density, which causes a systematic shift in frequency of up to 10%. D2D variation is significant resulting in a 3× std. deviation/median ($3\sigma/\mu$) of 15% over half a wafer. Finally, WID variation for identical structures is relatively small ($3\sigma/\mu \sim 4\%$). WID spatial correlation of RO frequency shows a dependency on direction of spacing and the orientation of the gates.

4.1 Effects of layout on frequency and leakage

Variations in polySi pitch spacing cause over 10% shift in frequency and a 20x shift in I_{LEAK} (Figures 6 and 7). This is much larger than the 1.1% frequency shift predicted by Spice simulations of the extracted layout, which capture only changes in the parasitic capacitances associated with varying layouts. D2D and WID variations are reduced with increased polySi density. Similarly, the effect of layout on stacked gates is smaller (Fig. 8).

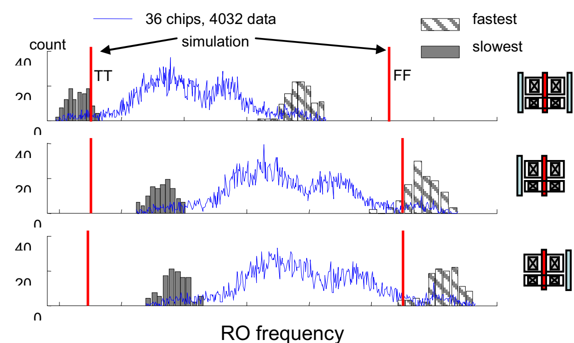

Figure 6. Frequency distribution for single-finger configurations. Vertical lines correspond to typical and fast corner simulation results. Bar plots correspond to the WID distribution of the fastest and slowest chip.

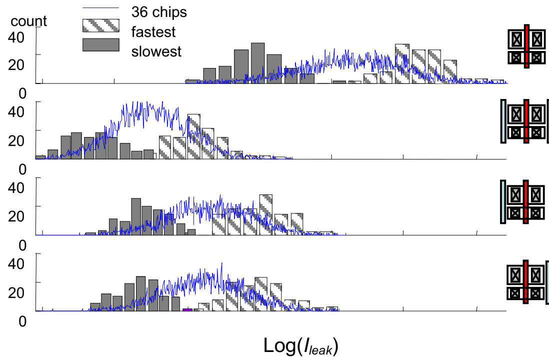

Figure 7. Log(I_{LEAK}) distribution for a single-finger configuration.

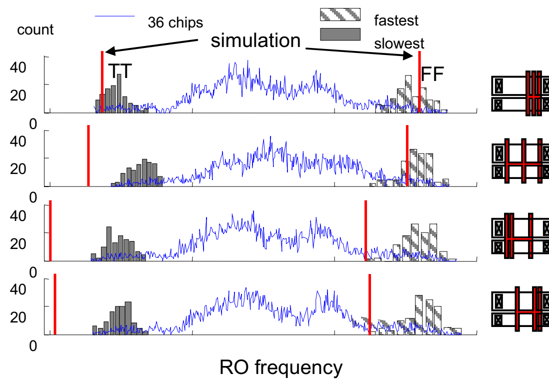

Figure 8. Frequency distribution for stacked gates.

Coma effect is present but small, around 1-2% shift in the mean RO frequency of single gates as shown in the second and third plots of Fig 6. Variation ($3\sigma/\mu$) is smaller by 0.4% for rotated gates across all chips. The effect of M1 on gates is small and due mainly to differences in parasitic capacitances. Both D2D and WID variations are weakly affected by layout.

4.2 D2D variations

The wafer maps of mean frequency and leakage in Fig. 9 show a radial pattern that can be attributed to non-uniform resist development [20-21]. As a result, the performance of chips is spread between the typical and fast corners.

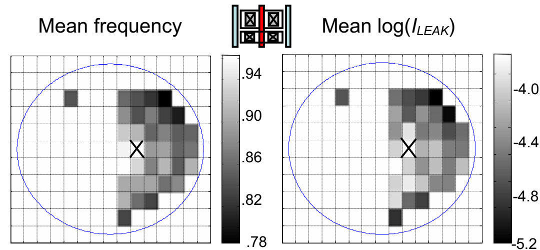

Figure 9. Wafer maps of mean RO frequency and mean Log(I_{LEAK}).

4.3 WID variations

WID variation is small and weakly dependent on the layout. A spatial correlation is observed in the frequency measurements, stronger in the horizontal than in the vertical direction (Fig.10). We observe that correlation depends only on the direction of spacing and orientation of the gates.

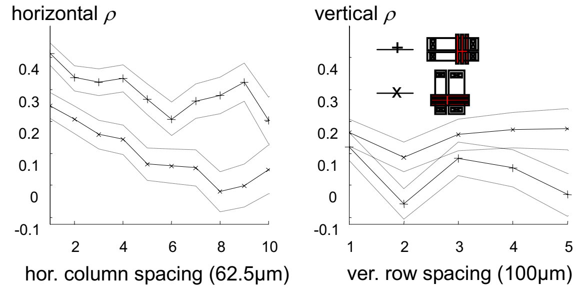

Figure 10. Spatial correlation coefficient.

In the horizontal direction, correlation is higher for vertically oriented gates while in the vertical direction, correlation is higher for horizontally oriented gates. In the RO, inverters with vertical gates are placed next to each other horizontally and inverters with horizontal gates are placed next to each other vertically. Hence we find that gates placed parallel to each other have higher correlation (Table 1). This observation accounts for the smaller WID variation observed in RO with rotated gates. The random gate delays, being less correlated in the rotated RO, has more averaging in the vertical direction.
The horizontal direction is along the slit of light in the stepper and is subject to lens aberrations and curvature resulting in more correlated features. The vertical direction is along the scan direction, which is subject to variation in scan speeds and light dosage, resulting in less correlated features. Other manufacturing effects such as e-beam mask stitching discontinuity could also account for the observed dependence on direction.
Leakage current, which is less sensitive to gate-length (L) but more sensitive to threshold voltage than RO frequency, has negligible spatial correlation.

Table 1. Spatial correlation coefficient of neighboring ROs for different gate orientation and spacing direction.

Slit direction = horizontal Scan direction = vertical		Horizontal spacing	Vertical spacing
RO Freq.	Vertical Gates	.4	.1
	Horizontal Gates	.25	.2
I_{LEAK}		0	0

5. Conclusion

Layout has significant impact on lithography-induced variability in 90nm technology. Correlation between the variations in ring-oscillator frequency measurements and transistor leakage currents indicates that the variations are caused by variations in effective channel lengths. The polySi pitch has the strongest effect, resulting in up to 10% variation in RO frequency for inverters laid out with isolated poly lines. To compensate for this effect, transistors with different channel lengths can be extracted from the layout [14], or the layout can be made uniformly dense [22].

The use of step-and-scan lithography induces stronger correlation between the gates laid out perpendicular to the direction of slit of light than those perpendicular to the direction of scan. This effect can be exploited in the layout of regular datapaths and memory to obtain a tighter performance spread [1, 23].

Systematic D2D variations dominate the WID variations for small chips, indicating that the use of per-die adjustable supply voltages and substrate biasing can be used for improving the parametric yield [2].

Acknowledgments

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