Energy-Delay Optimization of Thin-Body MOSFETs for the Sub-15 nm Regime

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Abstract

This paper presents the design of enhancement-mode and accumulation-mode thin-body MOSFETs optimized in terms of energy vs. delay (E-D), and assesses the effectiveness of back-gate biasing to adjust the leakage current. It is shown that back-gated FETs (BG-FETs) can provide power savings over double-gate FETs. Because BG-FETs span a wide range in E-D space, they can provide a single-device solution for high-performance and low-power applications through adaptive supply-voltage and threshold-voltage biasing.

Introduction

Power becomes a primary design constraint for CMOS technologies beyond the 90nm node, requiring circuit designs to be optimized with respect to both energy and delay. To achieve optimal energy *vs.* delay (E-D) performance, multiple transistor designs tailored to various applications are presently used. Alternatively, adaptive threshold-voltage (V_{th}) control can be used in conjunction with dynamic supply-voltage (V_{DD}) scaling to minimize power dissipation in circuits using a single transistor design.

Thin-body MOSFETs are more scalable than the classical bulk-Si MOSFET structure, and hence may be adopted for sub-45nm (gate length $L_G < 20$nm)
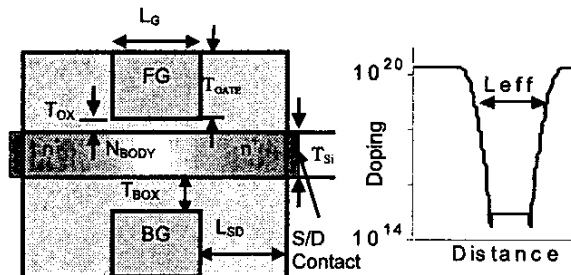

Fig 1: Cross-sectional schematic of BG FETs studied. The effective channel length L_{EFF} is defined as the separation between the points where the S/D doping falls off to 2×10^{19} cm^{-3}. (See inset).

CMOS technologies. Adaptive V_{th} control can be achieved in a thin-body FET by biasing the front and back gates of a double-gate FET independently, using the front gate to switch the transistor on/off and the back gate to adjust V_{th}. Back-gate tunneling sets the upper limit for $|V_{BG}|$. In this paper, we compare the E-D performance benefits of such back-gated (BG) FETs over the double-gate FET (DG-FET) in which the two gates are biased together.

Transistor Design Optimization

2-D device simulations were performed using Taurus with drift-diffusion transport and the 1-D Schrödinger equation [3]. Two BG-FET designs were considered: enhancement-mode (ENH) and accumulation-mode (ACC). Two versions of the DG-FET were also considered: high-performance (HP) device and low-power (LP). (See Fig. 1 and Table 1).

The DG-FETs and BG-FETs were each optimized to achieve maximum drive current I_{on} for a fixed active-state leakage current and DIBL of 100 mV/V. This was achieved by co-optimizing T_{Si}, T_{BOX}, and the S-D separation (L_{EFF}) for a constant T_{OX} using the design-of-experiments (DOE) methodology, and considering the scale length [4]. $L_{EFF} > L_G$ is optimal in the sub-20nm L_G regime [5].

BG-FETs, which have only one switching gate, need to have a thinner body than the DG-FET to adequately control short-channel effects (Table 1). A thin T_{BOX} provides higher V_{th} sensitivity to V_{BG}, but results in poorer subthreshold swing S and degraded I_{on}. Thus, BG-FETs have I_{on} values intermediate to those of the HP and LP DG-FETs (Fig. 2).

Device Simulation parameters	Lg = 13nm			Lsd = 13nm	
	T_{OX}	V_{DD}	T_{GATE}	S-D doping	
	11.5 Å	0.6 V	19.5 nm	10^{20} cm^{-3}	
	BG ENH	BG ACC		DG-FET	
	HP[a]	HP	LP	HP	LP
T_{BOX} (Å)	63	69	20.1	11.5	11.5
T_{Si} (nm)	5	4.3	4.3	8.2	8.2
N_{BODY} (cm^{-3})	2×10^{16}	-1×10^{19}		2×10^{16}	
Φ_G (eV)	4.4	4.57	4.5	4.45	4.6
S-D $\sigma_{Gaussian}$ (nm)	2.0	0	0	2.0	2.0
ρ_C, Ω-cm^2	5×10^{-9}	5×10^{-9}		5×10^{-9}	
L_{EFF} (nm)	20.2	21.4[c]	17.6	15.6	15.6
$I_{OFF, ACTIVE}$ (µA/µm)	1	1	1	1	0.01
I_{ON} (µA/um)	575	473	629	665	398
I_{SLEEP} (nA/µm)[d]	10	10	0.4	1000	10

Table 1: Summary of the device design parameters used. [a] HP refers to high performance and LP refers to low power. [c] L_{EFF} for the BG ACC device is defined as the distance between points where the S/D doping falls to the channel doping value. [d] Sleep state current is evaluated at $V_{BG} = -V_{DD}$.

Comparison of BG-FETs and DG-FETs

BG-FETs and DG-FETs are compared here in terms of short channel behavior, ON-state performance and immunity to process-induced variations.

(a) BG ENH (b) BG ACC (c) HP DG-FET

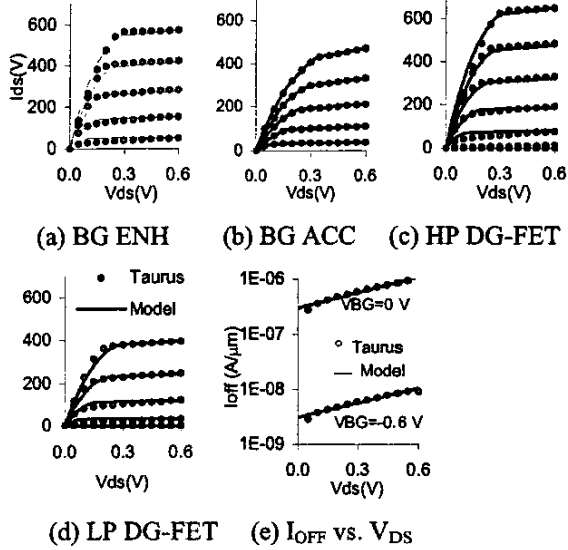(d) LP DG-FET (e) I_{OFF} vs. V_{DS}

Fig. 2: Drain characteristics of the devices used in this study. (a-d) Simulated curves from Taurus [3] (symbols) were fitted to an empirical model (solid lines). (e) Leakage of the BG devices matches that of the HP DG-FET at V_{BG}=0V, and are lower than the leakage of the LP DG-FET at V_{BG} = -V_{DD}.

The BG-FETs were optimized in order to achieve a sleep state current of 10^{-8} µA/µm at V_{BG}= -V_{DD}. Increasing the back-gate effect to reduce the sleep state current comes at the expense of I_{on}. Simulations of optimized BG-ACC and BG-ENH FETs with L_g=9nm (Fig. 3a) show that back-gate control on V_{th} is effective for sub-10nm gate lengths. The ACC design provides the largest back-gate effect, and therefore can be put into deep sleep mode, making it attractive for low power applications.
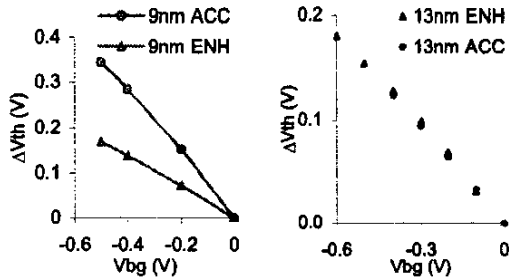

Fig. 3: (a) ACC devices can show better sensitivity to V_{BG} and hence lower leakage (b) 13nm ACC and ENH devices with same back-gate effect for equal I_{OFF} reduction.
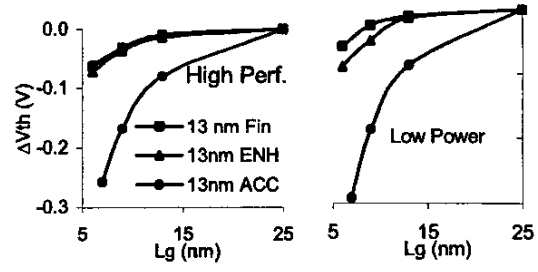

Fig 4: The ENH devices show better V_{th}-rolloff than the ACC devices. Low-power and high-performance devices show similar V_{th}-roll off characteristics.
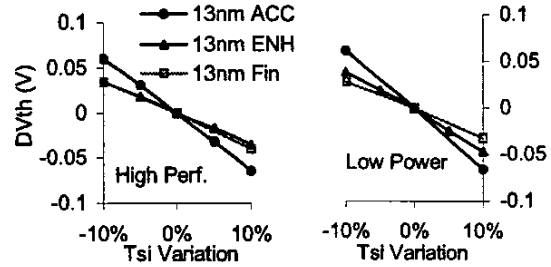

Fig 5: The ENH devices show lower sensitivity to variation in T_{Si} than the ACC devices. DG-FETs show the least sensitivity to T_{Si} fluctuations.
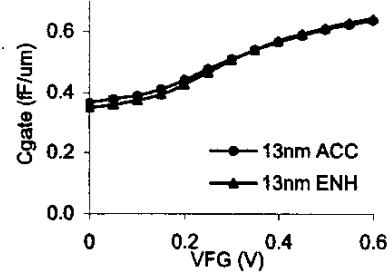

Fig 6: The gate capacitance is similar for ACC and ENH devices; thus the intrinsic delay scales with I_{on}.

In comparing short-channel effects, V_{th} rolls off more rapidly with decreasing L_G (Fig. 4) and is more sensitive to T_{Si} variations (Fig. 5) for the BG-ACC device. The DG-FET shows the least T_{Si} sensitivity, owing to its thickest body.

The BG-ENH device has lower intrinsic delay than the BG-ACC device, because of its larger I_{on} (Fig.2) and marginally smaller C_{GATE} (Fig.6). The performance gap between the two devices decreases with scaling into the sub-10nm regime, while the BG-ACC device retains much lower sleep leakage (Table 1).

Circuit-Level Benefits of BG-FETs

The simulated I-V data were fit to a simple velocity saturation model (Fig. 2), which was subsequently used for circuit simulations to evaluate E-D tradeoffs. Adaptive V_{DD} and V_{th} scaling can be used to minimize energy dissipation as the delay requirements of a circuit change. Deeply scaled bulk-MOSFETs have limited V_{th} tuning range due to lowered body effects and reduced V_{DD}/V_{th} ratios [1-2], and the V_{th} of DG-FETs cannot be dynamically changed. The V_{th} tunability of BG-FETs makes them attractive for minimizing energy over a wide range of target frequencies. Fig. 7 demonstrates an example system, where adaptive V_{DD}/V_{th} control of BG-FETs achieves wider energy scalability spanning the range of both HP/LP DG-FETs. While the highest performance achievable by the BG-ENH FET is lower than that of the HP DG-FET, the minimum energy approaches that of the LP DG-FET when the throughput is reduced significantly. Clearly, BG-ACC devices are not suitable for highest performance applications due to low I_{on}.
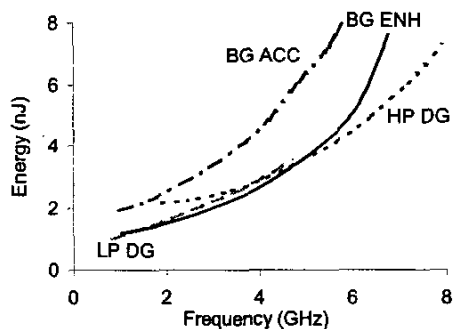

Fig 7: Dynamic voltage scaling of DG-FETs and BG FETs at L_g = 13nm. With V_{BG} adjusted as V_{DD} is scaled, the BG-FETs are able to achieve higher performance than the low-power DG-FET and lower energy than the HP DG-FET.

Table 2: Example System @ L_G = 13nm	
Logic depth	375 CV/I
Gate area	2.4 mm^2
Activity	10%
% Core sleep	30%

Active leakage control [1] implemented with BG devices allows a circuit to benefit from the low sleep-state leakage while still having performance determined by the on-state I_{on} in active blocks. The energy penalty for placing a BG device in the sleep state is the switched capacitance of the back gate, and it can be done in a single cycle. In a bulk-Si

MOSFET technology, switching a large well capacitance incurs a significant energy and delay penalty. Since the benefits of the BG FETs going into a deeper sleep is retained with scaling into the sub-10nm regime (Fig. 3), they are well suited for leakage control in future systems. In our simulations, V_{BG} was limited to -V_{DD}; practical systems implementations set the limit on V_{BG}.
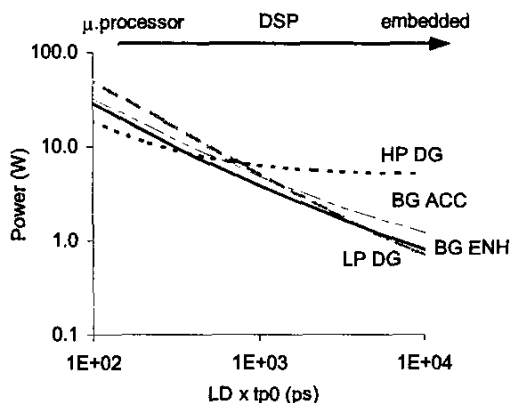

Fig 8: Minimum power envelope with changing logic depth in the example system (Table 2). The envelope represents the minimum power achievable through voltage scaling and back-gate biasing.

Fig. 8 illustrates the E-D trade-offs with varying logic depth. Both BG-ENH and BG-ACC implementations make use of adaptive threshold control for active leakage control in addition to V_{DD} adjustment to achieve a wider range of optimality. The minimum power envelope for the BG-FETs lies in-between that of the HP and LP FinFETs. Both Fig. 8 and Fig. 9 illustrate the capability of the BG-FETs to achieve delays similar to a HP DG-FET, and attain the low power of LP DG-FETs at low operating frequencies.

Conclusion

Back-gated thin-body FETs provide the ability to put a circuit into sleep mode to reduce power dissipation. Thus, BG-FETs are advantageous for retaining the benefits of dynamic supply-voltage and threshold scaling in the sub-10 nm era, and provide single technology solutions that can span both high-performance and low-power application spaces.

References

[1] J.W. Tschanz et al., IEEE JSSCC, p.1838, 2003
[2] A. Khakifirooz et al., IEEE SOI Conf., p.58, 2002
[3] Taurus 2002.4 User's Manual, Synopsys Inc., 2002
[4] D. Frank et al., IEEE EDL, Vol.19, p.385, 1998
[5] S. Balasubramanian et al., SiNano.Workshop, 2002