25.4 A 1.8V 14b 10MS/s Pipelined ADC in 0.18μm CMOS with 99dB SFDR

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Pipelined ADCs are widely used in Nyquist sampling applications that require a combination of high resolution and high throughput. While scaling of CMOS technology offers the potential for improvement of sampling rate, the accompanying reduction in supply voltage creates both fundamental and practical limitations on achievable resolution and speed, particularly when low power consumption is required. Much of the recent work in pipelined ADCs has been aimed at alleviating or overcoming these challenges.

This work describes the prototype design of a 14bit pipelined ADC in 0.18μm CMOS technology that achieves a 73.6dB SNDR while consuming only 112mW of power. The measured SFDR of 99dB up to and beyond the Nyquist frequency demonstrates the superior linearity and bandwidth of the analog circuitry operating under a low supply voltage of 1.8V. The techniques that have enabled this performance include a power-efficient, ratio-independent conversion scheme, an optimum pipeline stage scaling algorithm, a nested CMOS gain-boosting technique, a Δ/Σ common-mode (CM) voltage regulation circuit, and an op amp sharing technique.

Figure 25.4.1 shows the block diagram of the 6-stage, 14bit pipelined A/D converter. At the architectural level, a loaded amplifier model is used to optimize the stage resolution and capacitor tapering factor simultaneously, taking into account noise from both the amplifier and switches. A speed factor is introduced to make the analysis dependent on sampling rate. Without a dedicated S/H amplifier, a 1.5b/stage topology is used in this work to avoid the phase misalignment between the sample acquisition time and the comparator banks decision time in the first stage. The optimum capacitor tapering factor is determined to be 0.5 with this choice.

In a fully optimized pipeline implementation, the most important source of nonlinearity error is capacitor mismatch. In this work, a passive capacitor error-averaging (PCEA) technique is used. Calculations and Monte Carlo simulations demonstrate that 14bit INL can be achieved with 7bit capacitor matching accuracy [1]. Figure 25.4.2 shows the PCEA circuit diagram. In each cycle T, two residue voltages containing complementary errors are produced by interchanging roles of sampling capacitors C_1 and C_2. Two capacitors from the next stage directly sample the residue voltage pair sequentially. Compared to the active CEA approach [2], an explicit averaging amplifier is eliminated; averaging takes place when two sampling capacitors merge charge in the subsequent phase. The elimination of residue resampling reduces the total conversion power by a factor of four with fixed SNR; uncorrelated circuit noise in two separately acquired residues further increases SNR by 3dB. The limitation of PCEA is that it takes four phases to complete the sampling-comparison-amplification process as opposed to two in a conventional implementation. In this work, the extra phases are also utilized to allow a long comparator resolving time of T/4.

Delivering sufficient DC gain while maintaining low power dissipation at high sampling rate is a difficult challenge for op amp designs under low supply voltage. In this work, a nested CMOS gain-boosting technique (Fig. 25.4.3) is used. A two-level boosting with 0.2μm devices results in a minimum of 130dB open-loop gain in simulation. To maintain high current efficiency and high output swing simultaneously, the main amplifier utilizes a pseudo-differential (PD) architecture as shown in Fig. 25.4.3. With four transistors in stack, the output swing of the op amp exceeds $2V_{pp}$. Boosting amplifiers are all folded cascodes with p- or n-type input to allow flexible input CM ranges. The nested boosters assume identical structures and are scaled down relative to the main boosters.

Provision for CM control is crucial in PD amplifiers. Figure 25.4.4 shows an analog Δ/Σ loop that facilitates this regulation. Output CM is sensed and compared to the desired reference; the error is then accumulated with a discrete-time integrator and fed-back to be the bottom-plate bias for the S/H circuit. A look-ahead capacitor is used to cancel high-frequency gains such that the closed-loop gain is almost zero at all frequencies.

To further reduce power, only six op amps are used for the 14bit converter with each shared between adjacent SC blocks. The challenge of this technique is to maintain charge fidelity at the summing node. A modified clock scheme and dummy switches are used to minimize residual charge errors.

Signal-dependent charge injection and on-resistance variation of switches pose fundamental limits on achievable distortion levels of switched-capacitor circuits. Increased f_T through technology scaling improves switch performance. In this work, the use of 0.18μm devices combined with the clock bootstrapping [3] and inline switch [4] techniques resulted in an outstanding dynamic performance for Nyquist converters.

The prototype ADC was fabricated in a 1.8V, 0.18μm, 6M1P digital CMOS process. Capacitors are implemented using metal-insulator-metal (MIM) structures with no special attention paid in layout to match them. The die size of the chip measures 4.3 x 3.5mm^2 (Fig. 25.4.7). The conversion is free of trimming or calibration. With reference voltages of 1.4V and 0.4V, measured DNL and INL are +0.31/-0.31LSBs and +0.53/-0.58LSBs respectively (Fig. 25.4.5). Peak SNDR reaches 73.6dB with 1MHz input, equivalent to 11.9 ENOB. Measured SFDR is 98dB (THD = 91dB) at 1MHz input and 99dB (THD = 95dB) at 5.1MHz input. The elevated low-frequency distortion is attributed to the transformer used in testing. At 40MHz input, the chip still produces 84dB of THD, but SNDR drops to 64dB (Fig. 25.4.6). All measurements are done at a 10MS/s sampling rate, 1.8V supply, and 25°C. Total power consumption of the chip is 112mW excluding the LVDS digital output drivers.

Acknowledgements:
The authors thank ST Microelectronics for providing the chip fabrication and the Data Conversion Systems Group of National Semiconductor for help with testing.

References:
[1] Y. Chiu, "Inherently Linear Capacitor Error-Averaging Techniques for Pipelined A/D Conversion," *IEEE Trans. CAS II*, vol. 47, pp. 229-232, Mar. 2000.
[2] B.-S. Song et al., "A 12bit 1MSample/s Capacitor Error-Averaging Pipelined A/D Converter," IEEE *J. Solid-State Circuits*, vol. 23, no. 12, pp. 1324-1333, Dec. 1988.
[3] A. M. Abo et al., "A 1.5V, 10bit, 14.3MS/s CMOS Pipeline A/D Converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, May 1999.
[4] H. Pan, et al., "A 3.3V 12b 50MS/s A/D Converter in 0.6μm CMOS with Over 80dB SFDR," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1769-1780, Dec. 2000.

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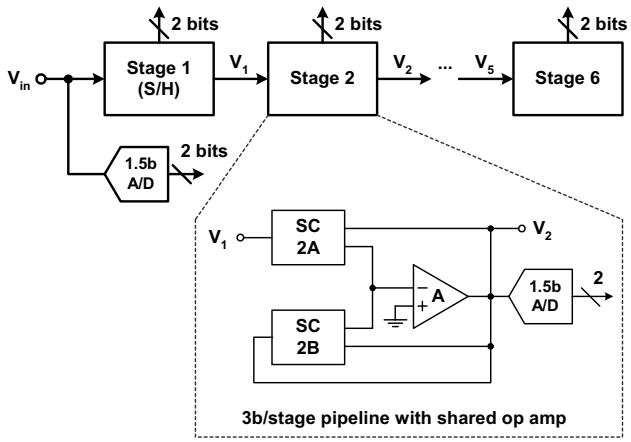

Figure 25.4.1: 14bit pipelined ADC block diagram.

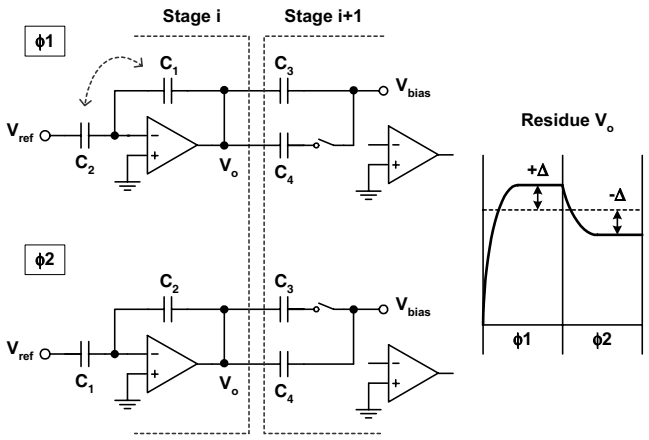

Figure 25.4.2: Passive capacitor error-averaging (PCEA).

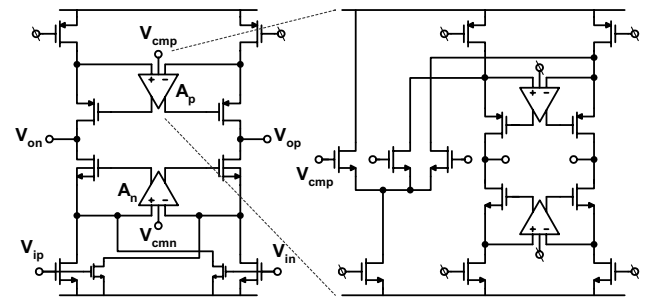

Figure 25.4.3: Nested CMOS gain-boosting amplifier.

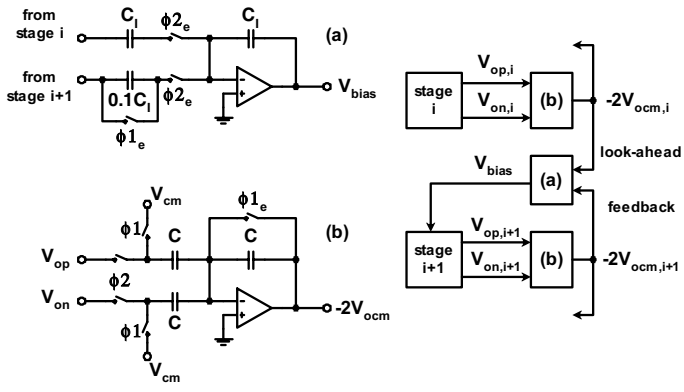

Figure 25.4.4: Δ/Σ common-mode voltage regulator.

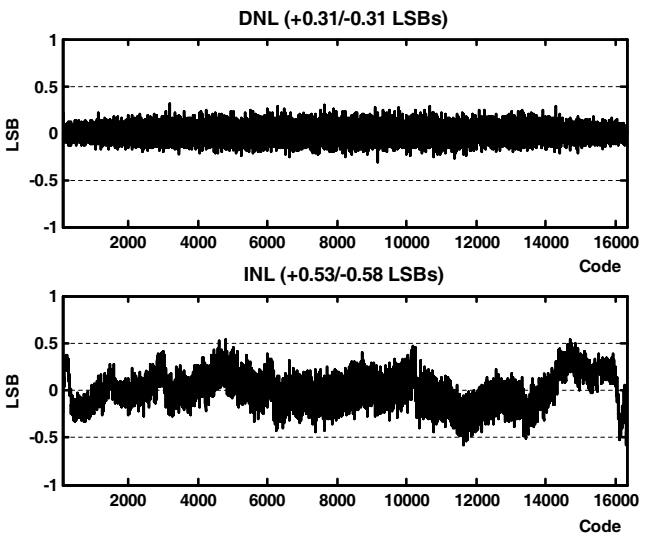

Figure 25.4.5: Measured INL and DNL at 10MS/s with 1MHz input.

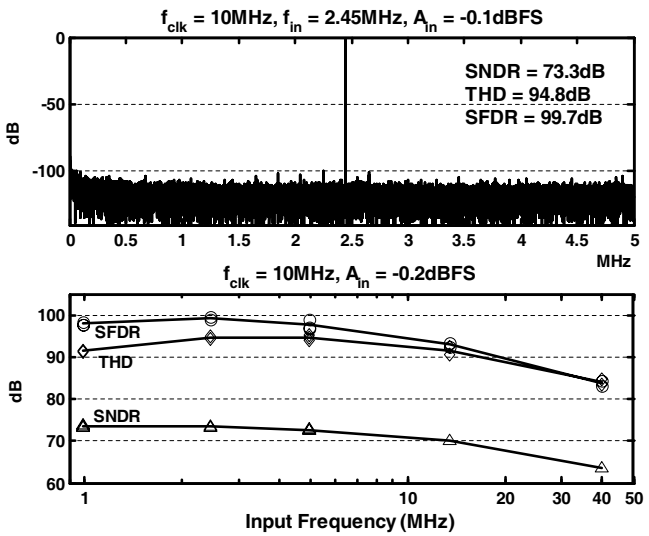

Figure 25.4.6: Measured FFT spectrum at 2.45MHz input (top); measured ADC dynamic performance (bottom).

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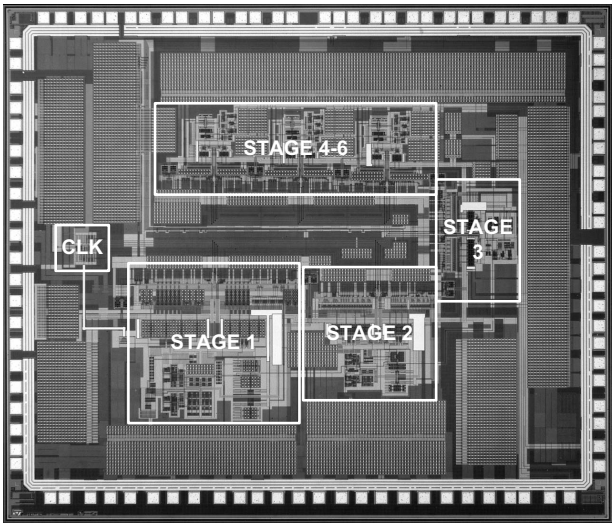

Figure 25.4.7: Die micrograph.

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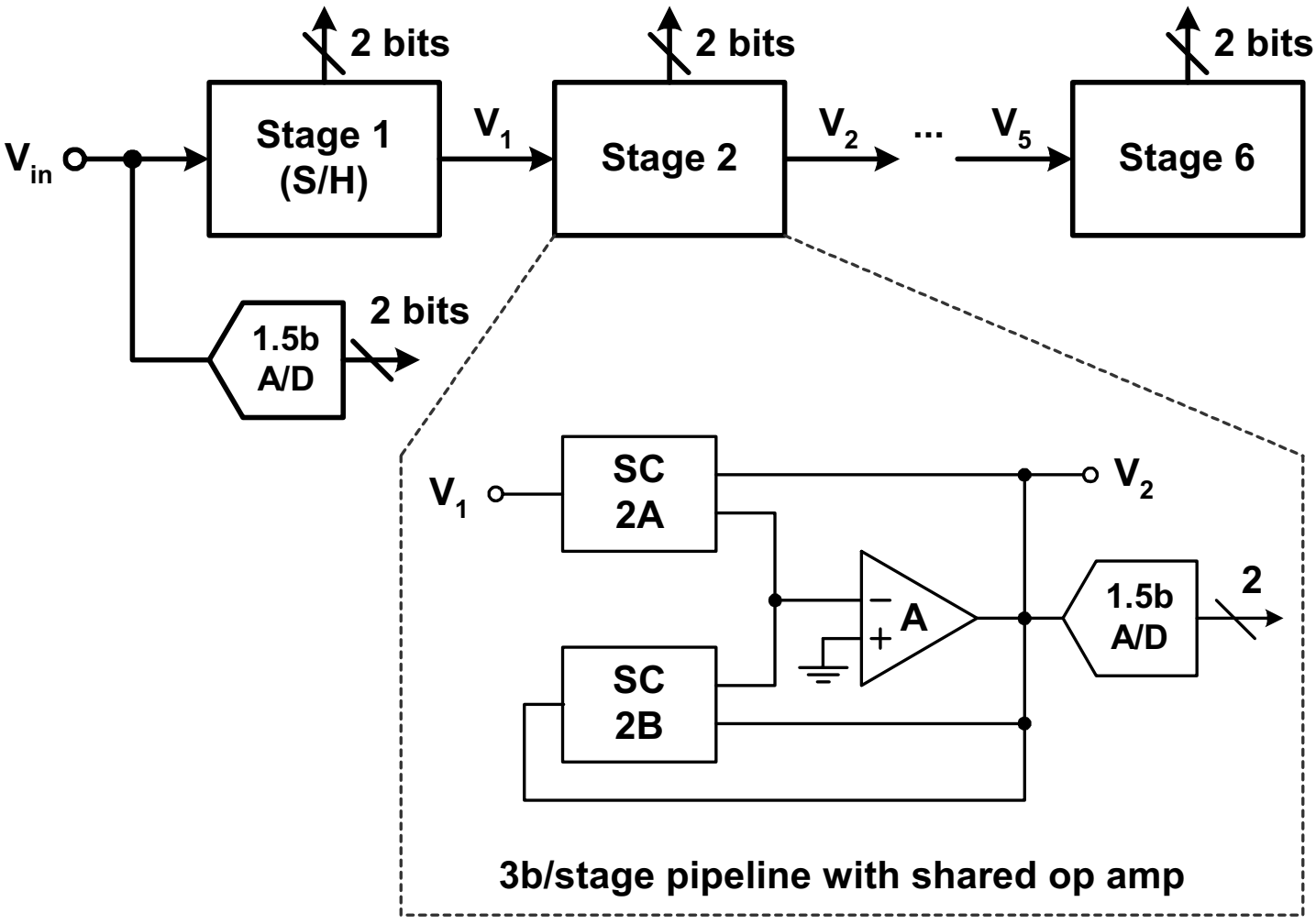

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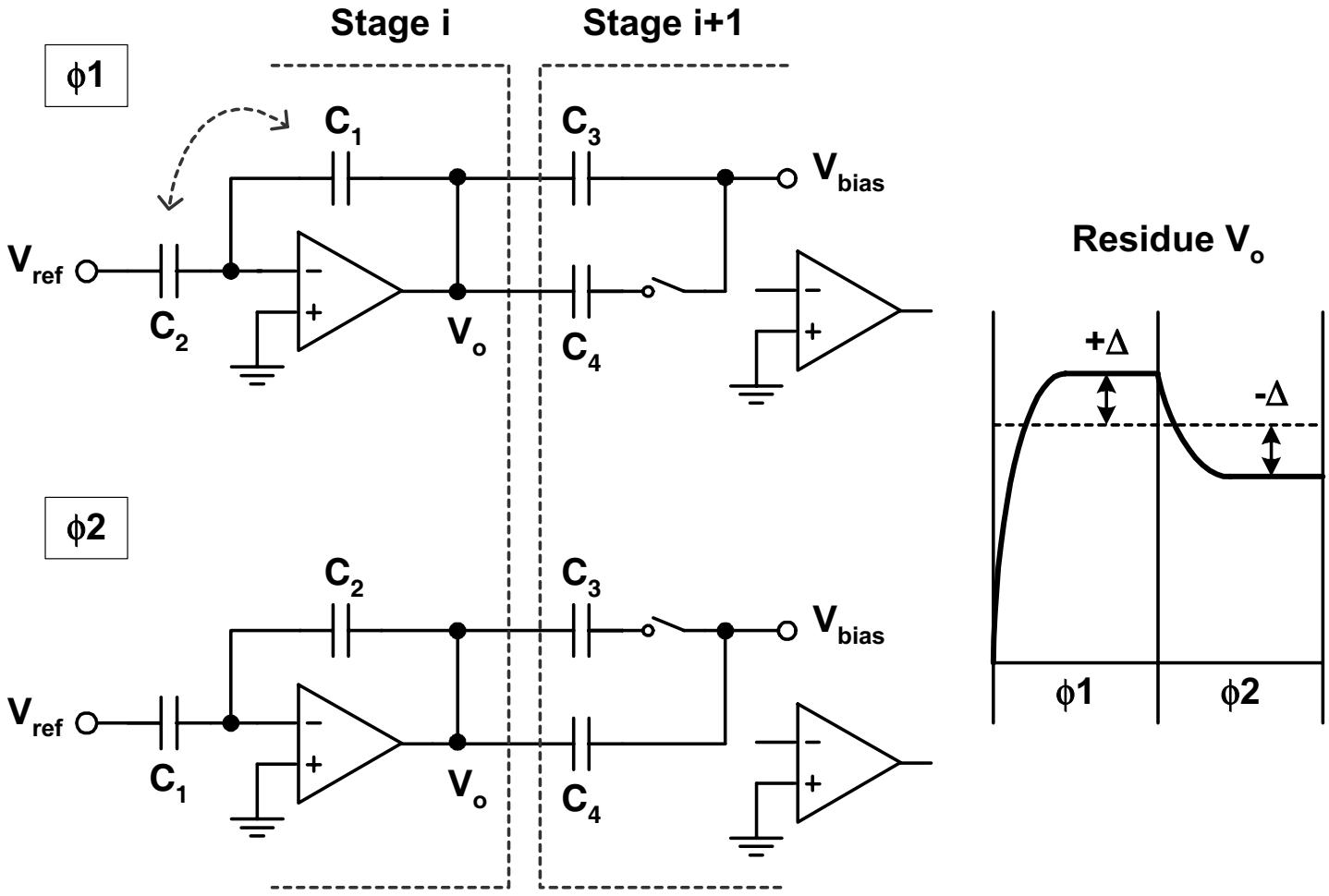

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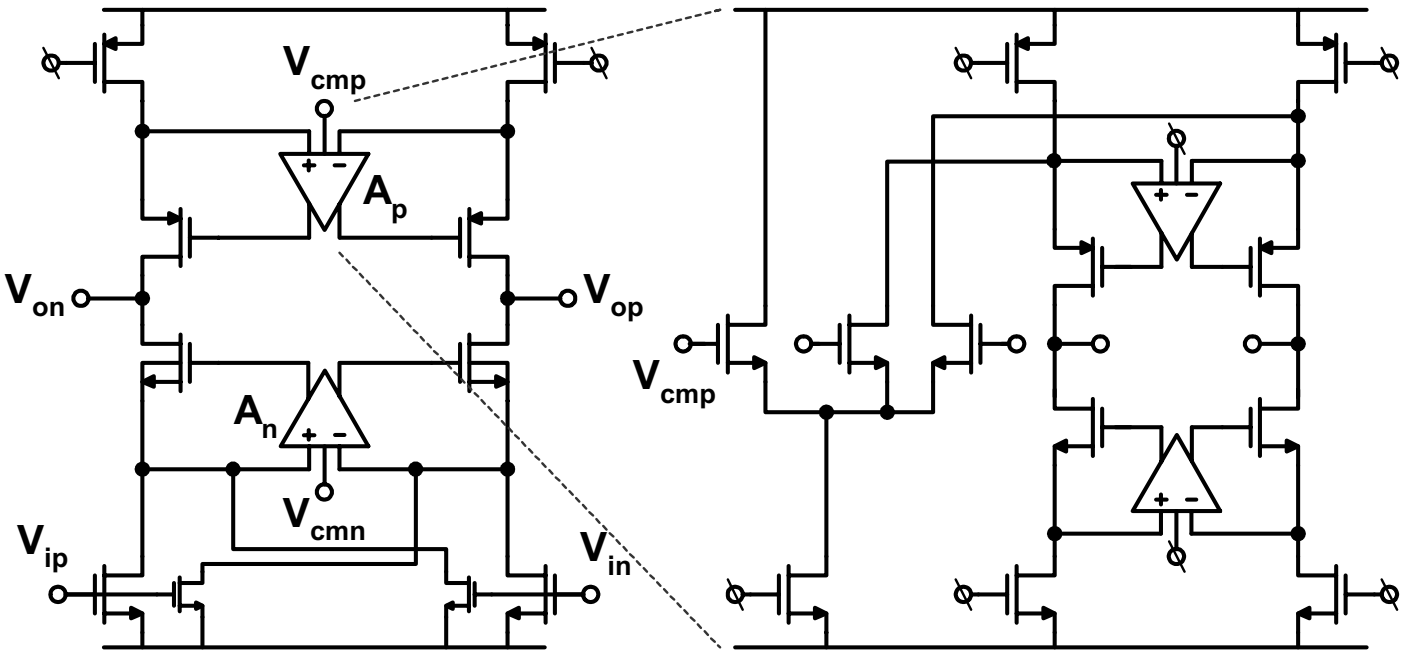
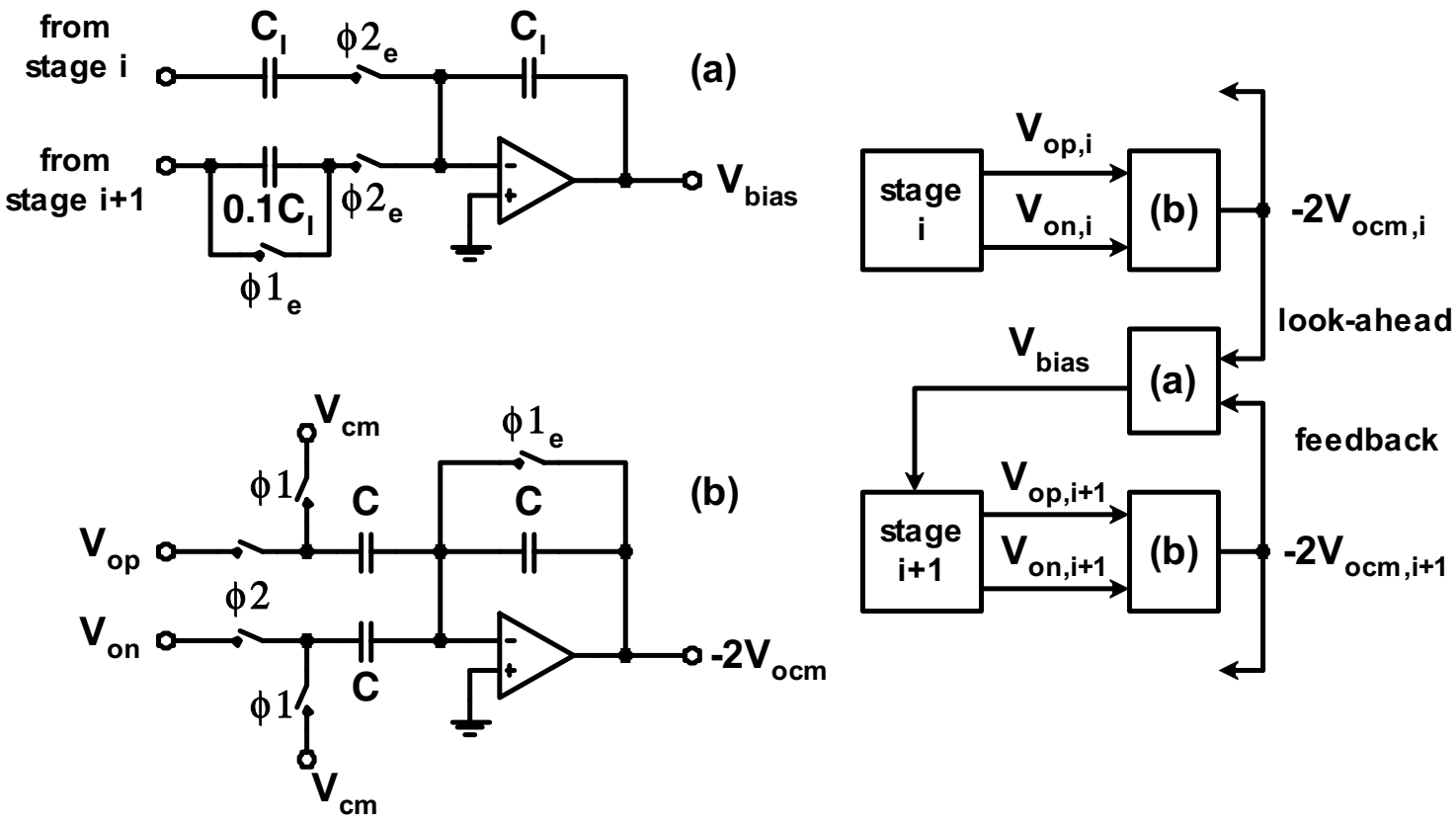


Figure 25.4.3: Nested CMOS gain-boosting amplifier.



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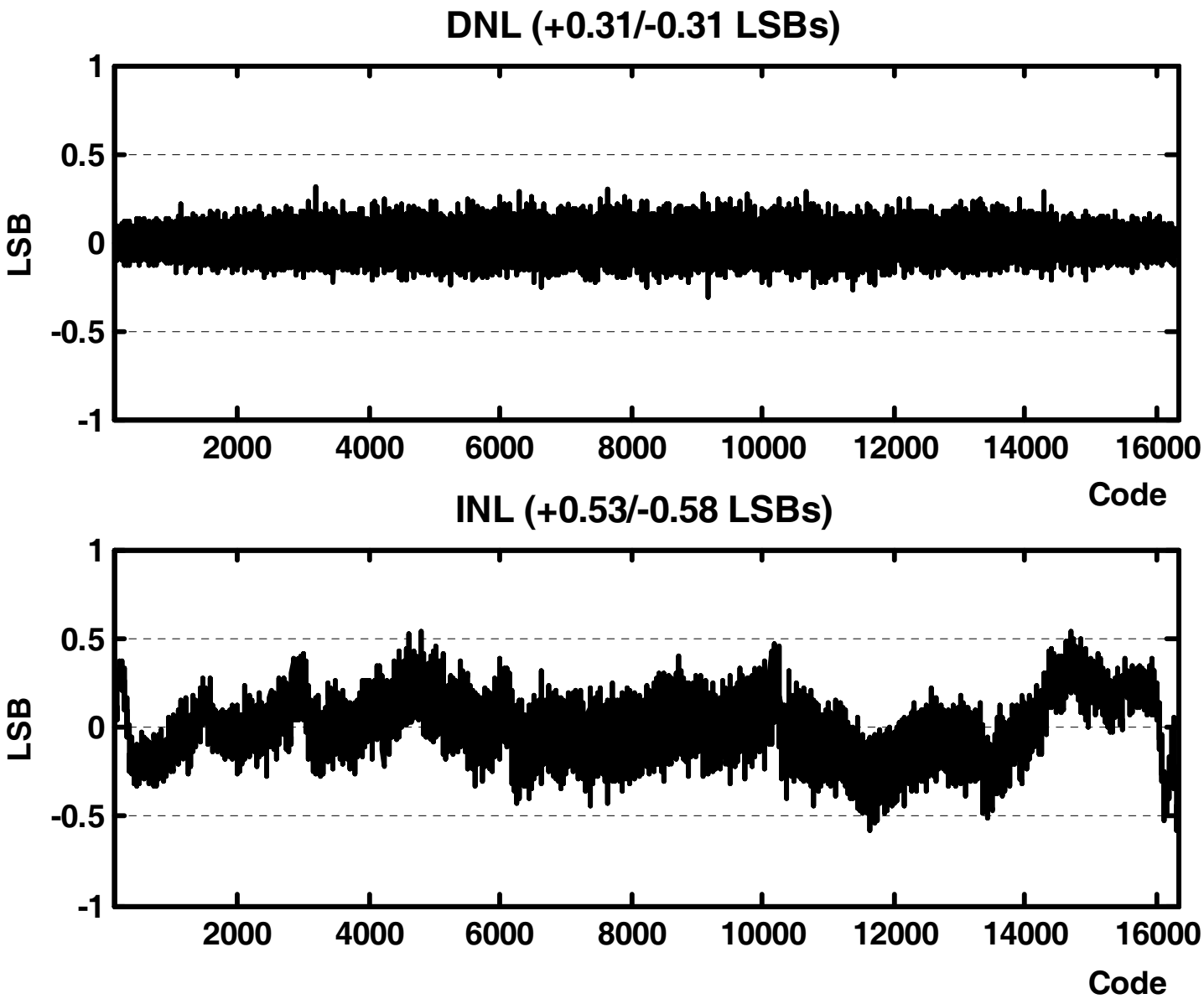

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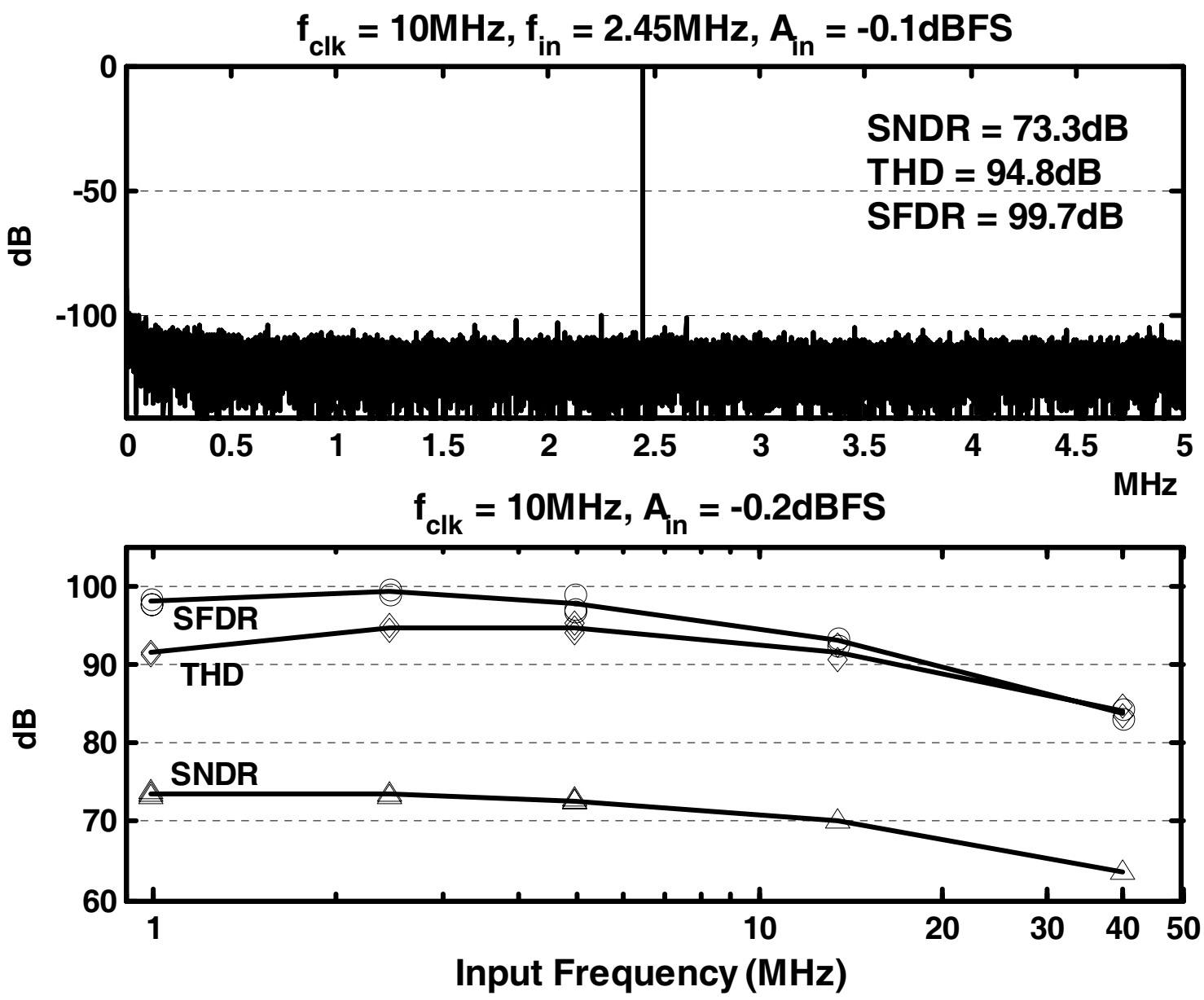

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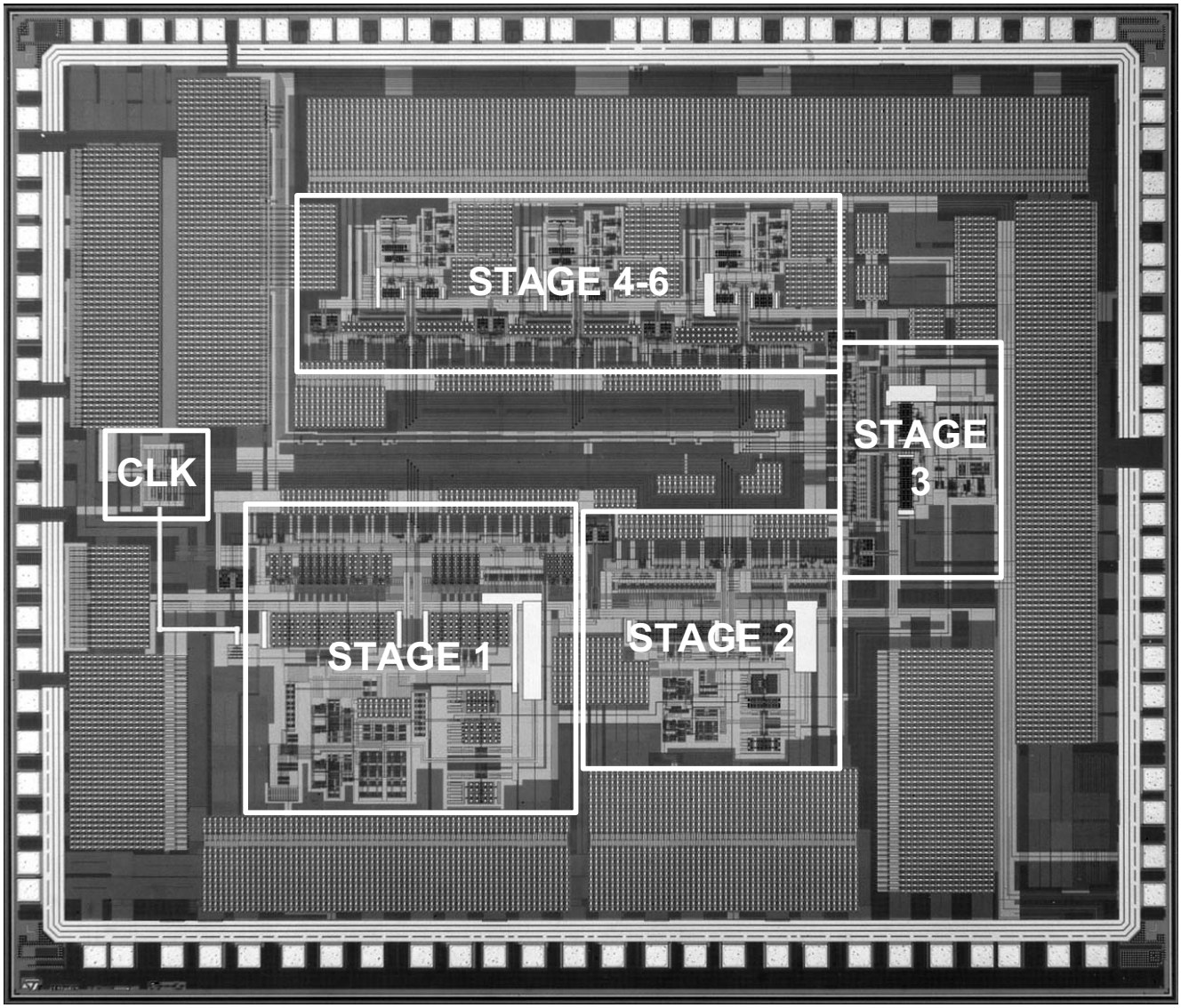

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