Current gain in bipolar transistors with a field plate over the base surface

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Abstract: Vertical *n-p-n* and lateral *p-n-p* transistor structures of an integrated circuit are studied using an electrolytic tank analogue and it is shown that the presence of a proper field plate extending from the collector-base junction over most of the base surface will improve the current-gain factor considerably. Experimental results of the analogue study, simulating typical carrier lifetimes and typical overall dimensions, are presented with various geometrical dimensions as parameters.

1 Introduction

Recently, a 2-dimensional electrolytic tank analogue[1] simulating volume recombination in the base region of bipolar transistors has been reported. The studies[1,2] have shown that the current gain of transistors is limited by the excess stored charge in the transverse region of the base and also by the transverse diffusion of minority carriers into the base contact. This simulation study has also been adopted for the study of lateral *p-n-p* transistors[3] and it has been shown that the current gain of these transistors can be increased by providing a gap in the n^+ buried layer.

The purpose of this paper is to study the effect of a field plate over the base surface and extending from the collector-base junction edge, on the current gain of vertical *n-p-n* transistors of integrated circuits, using an electrolytic tank analogue similar to the one discussed earlier.[1-3] It is shown that a field plate (i.e. m.o.s structure), spanning the major portion of the base surface (see Fig. 1*a*) and biased such that the region below is depleted, reduces the stored charge in the transverse region of vertical *n-p-n* transistors. The presence of this depletion region extending up to the collector-base junction, as shown in Fig. 1*a*, aids in improving the collection of carriers injected in the transverse direction. Thus an improvement in current gain is achieved by reducing the recombination current and aiding the collection of carriers in the transverse region. In addition to the above, it is shown that a similar field-plate structure employed in lateral *p-n-p* transistors of integrated circuits would considerably improve their current gain.

Sah[4] has given a detailed account of the effects of a field plate over the emitter-base junction of a vertical transistor and Grove[5] has discussed these results. Experimental measurements[6] on a specially designed, fabricated transistor with a field plate over the emitter-base junction for studying the surface effect on the current gain have shown that the base current and hence the current gain of the transistor depends upon the bias voltage on the metal electrode over the oxide protecting the emitter-base junction. The present study of vertical *n-p-n* transistors is different from the above studies and the field plate extends from the collector-base junction over the major portion of the base surface. It may be noted that in the present study the field plate does not extend over the emitter-base junction (Fig. 1*a*) and hence the recombination effects discussed earlier[6] are not present in the proposed structure.

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Lindmayer[7] has studied the effect of field plates over the entire base surface of lateral transistors in order to investigate the contribution of surface recombination to the base current of these transistors. His experiments have shown that the current gain of lateral transistors can be increased by a correctly biased field plate. This increase in current gain is caused by the field-effect modulation acting in parallel with the lateral transistor action. In the present study of lateral *p-n-p* transistors, as in the case of vertical *n-p-n* transistor study, the field plate does not extend over the emitter-base junction and has the advantage of avoiding the recombination effects discussed by Reddi.[6] The lateral transistor structure proposed (Fig. 2*a*) improves the current gain by producing reduction in the lateral base width without causing punch through; this is because the depletion layer below the field plate is not affected by the collector-base reverse-bias voltage.

Experiments simulating various lifetimes with different geometries confirm that the bipolar transistors (whether vertical *n-p-n* or lateral *p-n-p*) with m.o.s structure over the major portion of the base surface give rise to an increase in current gain by a factor of more than two (averaging from 3 to 4). The theory and description of the analogue are given in Section 2 and the experimental results in Section 3.

2 Experimental setup

2.1 Vertical n-p-n transistor

Fig. 1*a* shows the geometry of the vertical *n-p-n* transistor simulated. Note the m.o.s structure over the major portion of the base surface, which is the new feature proposed here for improving the gain and hence the gain bandwidth of the transistor. The base contact is assumed to be situated perpendicular to the line of symmetry XY as shown in Fig. 1*a*. In view of the symmetry, only one half of the transistor is simulated in the analogue.

Fig. 1*b* shows a schematic representation of the longitudinal section of the electrolytic tank used for the analogue setup. As discussed in earlier papers,[1-3] the resistors connected to the pins (represented by the dots in the Figure) drain out currents corresponding to volume recombination currents in the transistor-base region. The potential ϕ in the tank is analogous to the excess minority-carrier density in the base. The boundary values of minority-carrier density in the base at the emitter-base junction boundary, the collector-base junction boundary and the depletion edge below the m.o.s structure are properly taken into account in the analogue setup by using equi-

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potential surfaces (ABC, EFG and DE respectively) to simulate these boundaries. As the collector-base junction is reverse biased, the minority-carrier density in the base at this boundary is zero. The region below the m.o.s. structure is a depletion region (or an inversion layer followed by a depletion region) when properly biased, and the minority carrier density at the edge of this region is also zero. Therefore, the electrode DE which simulates this surface is kept at zero potential just as in the case of electrode EFG representing the collector-base boundary.

In a transistor having the structure shown in Fig. 1*a*, the minority-carrier electrons injected at the side walls (transverse region) of the emitter will be collected by the depletion layer below the m.o.s. structure. These carriers will either be reaching the collector directly or alternatively they will get recombined in the depleted surface where the recombination velocity can be high[8] and the recombining holes have to be replenished by the collector. In either case, the minority-carrier electrons collected by the depletion layer under the m.o.s. structure give rise to a corresponding collector current. Hence, in the analogue, the electrodes DE and EFG are connected together and the total current collected by them is a measure of the collector current. The total current drained by all the resistors connected to the pins is a measure of the base current, assuming unity emitter efficiency. The surface-recombination current on the base surface not covered by the field plate is neglected, because the surface-recombination velocity in the thermally oxidised oxide-silicon interface will only be 5 to 10 cm/s. Therefore, this surface is simulated by the portion CD of the insulating wall of the electrolytic tank. In cases of significant surface recombination, as with poor surfaces, the reduction of this base surface area (as compared to the conventional transistor) caused by the presence of the field plate should provide an additional improvement in the current gain.

The base contact is assumed to be far away from the emitter edge so that the minority carriers injected from the emitter do not reach the base contact. The ohmic drops as well as the effects of recombination in the emitter-space-charge layer are neglected. The emitter-space-charge-layer recombination affects the current gain only at extremely low values.

By varying the height and resistivity of the electrolyte, the magnitude of minority-carrier-lifetime simulated can be varied. The current gain is obtained for different geometries and lifetimes and the effect of the distance between the emitter-base boundary and the field plate on the current gain is obtained.

2.2 *Lateral p-n-p transistor*

The transistor simulated here has idealised rectangular geometry with planar junctions as shown in Fig. 2*a*. The m.o.s. structure over the major portion of the base surface

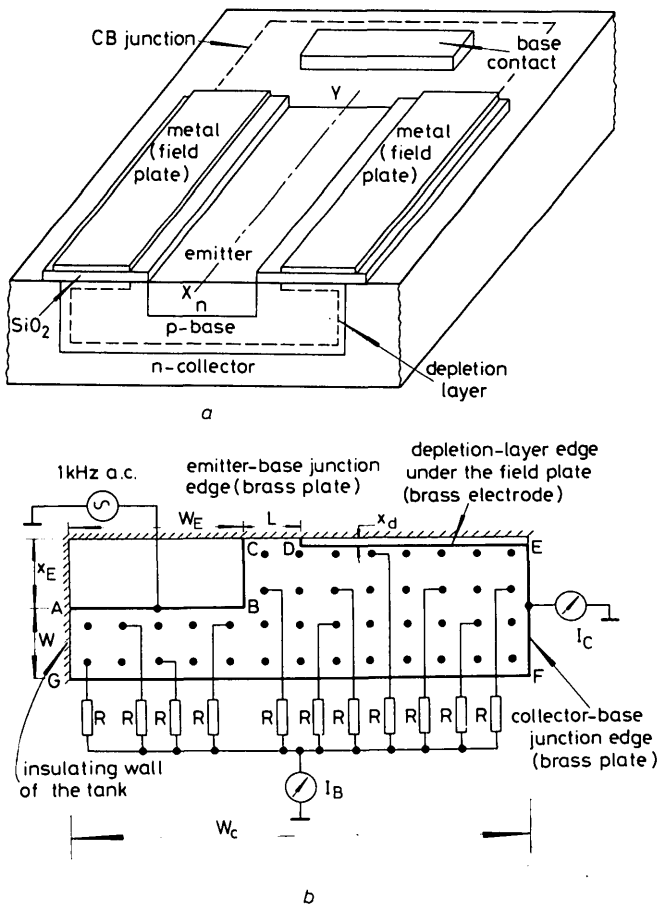

Fig. 1 *Vertical n-p-n transistor*

a Geometry simulated
b Schematic diagram of 2-dimensional analogue representation of one half of the transistor

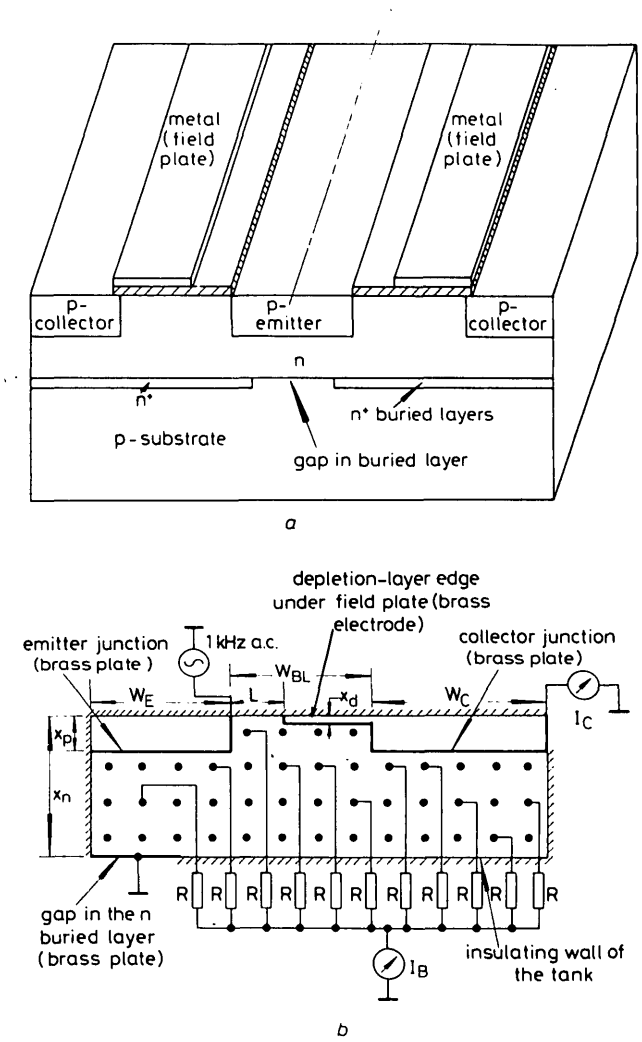

Fig. 2 *Lateral p-n-p transistor*

a Geometry simulated
b Schematic diagram of 2-dimensional analogue representation of one half of the transistor

helps in improving the current gain by reducing the lateral base width. From symmetry considerations, only one half of the transistor is simulated and the analogue setup used, along with proper boundary conditions, is shown in Fig. 2*b*. The situation is exactly similar to the one encountered in vertical *n-p-n* transistors.

3. Experimental results

3.1 Vertical n-p-n transistor

With reference to Fig. 1*b*, the choice of the overall dimensions of the transistor for our simulations study are typical of the transistors found in the integrated circuits. Fig. 3A gives the results obtained by varying the distance L between the emitter-base edge and the field plate. Two values of the depletion layer width X_d under the field plate are simulated for the purpose of illustrating the effect of voltage on the field plate. X_d depends on the voltage on the field plate and the doping in the base region. The results are plotted for two different base widths W. The current gain β is normalised with respect to the current gain β_0 which is measured in the analogue in the absence of the field plate. It may be noted that the current gain improves if the field plate is closer to the emitter edge; the improvement is better if the depletion layer width X_d is larger and that the effect of the field plate is felt more in the case of larger base width transistors.

In Fig. 3B, the effect of the depletion layer width X_d under the oxide is given for two different base widths, keeping L fixed at 0·8 μm. The larger depletion layer width X_d has the equivalent effect of reducing the recombination in the transverse base region; it also improves the collection of carriers in this direction, resulting in higher β.

The plot of carrier-density distribution in the transistor base with and without the field-plate structures are given respectively in Fig. 4*a* and *b*. These are the equipotential lines obtained in the analogue. A comparison of the two Figures brings out the following results:

(i) The equipotential lines in Fig. 4*b* are pushed towards the emitter-base junction indicating that the stored charge in the transverse region of the transistor with the field plate is much smaller than that of the transistor without the field plate. This reduction in transverse stored charge improves the current gain as well as the gain-band-width product of the transistor.

(ii) The crowding of the equipotential lines (Fig. 4*b*) in the transverse direction indicates that the collection is better in this direction than in the case of Fig. 4*a*. This is an additional factor which contributes to the improvement in β and gain-bandwidth product.

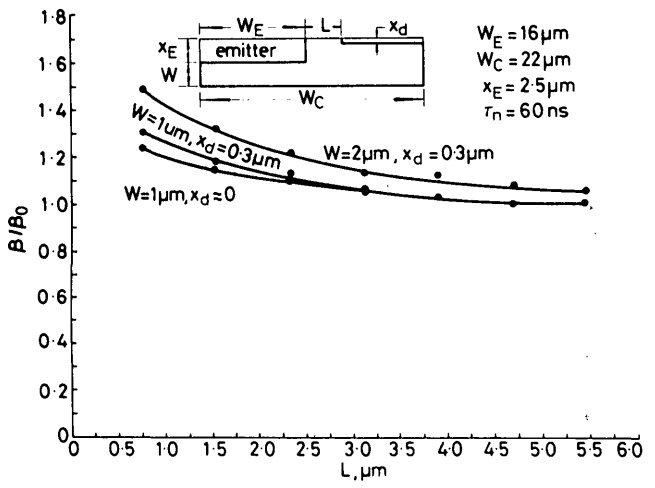

Fig. 3A *Normalised current gain of vertical n-p-n transistor as a function of the separation L between the field plate and the emitter-base edge for different values of the depletion-layer width X_d and base width W*

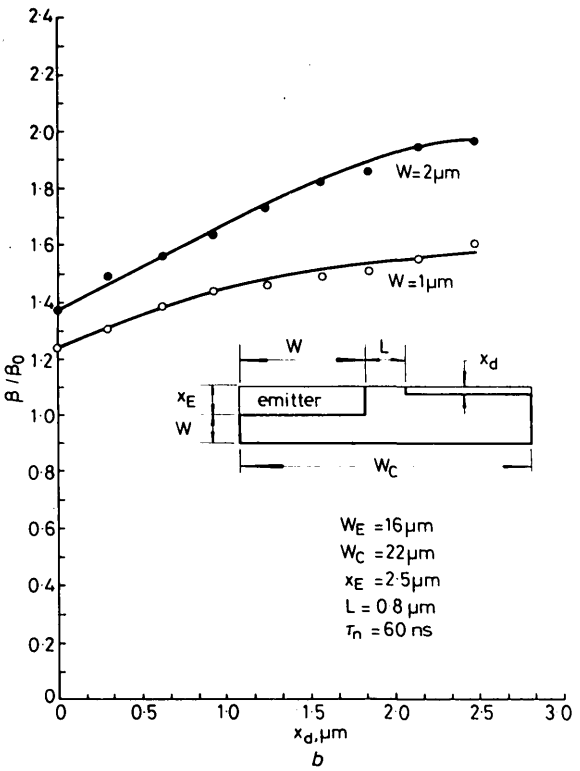

Fig. 3B *Normalised current gain of vertical n-p-n transistor as a function of the depletion-layer width X_d for two different base widths*

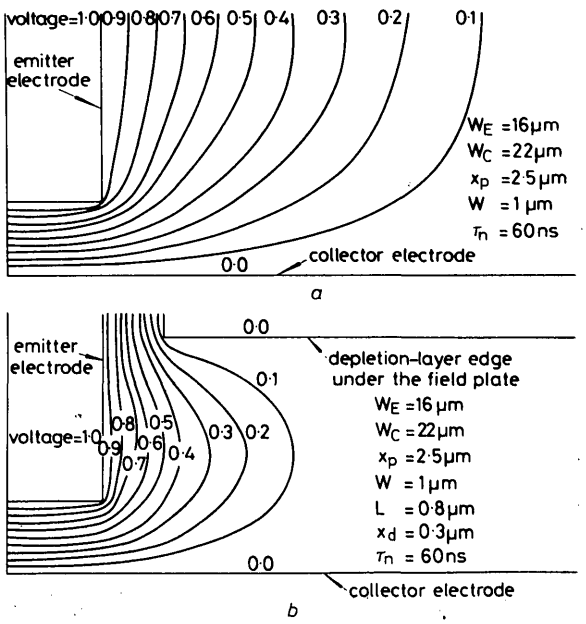

Fig. 4 *Minority-carrier density distribution in the base region of vertical n-p-n transistor*

a Without the field plate
b With the field plate

(iii) The equipotential lines in the axial region of the base are not at all affected by the presence of the field plate. This explains the better improvement factor in β when the base width is larger.

3.2 *Lateral p-n-p transistor*

While studying the effects of the field plate on the current gain of lateral transistors, the normalisation is carried out with respect to β of the transistor without the field plate and having a gap[3] in the buried layer. The magnitudes of the physical parameters simulated are given in Fig. 5. The results plotted in Fig. 5 for two values of the depletion layer width under the field plate show that an improvement factor as high as 2·5 to 3 can be achieved if the edge of the field plate is about 1·5 to 2 μm away from the emitter base edge.

Fig. 6 gives the effects for two different epilayer thicknesses X_n and Fig. 7 gives the results as a function of the depletion layer width X_d. In all cases it can be seen that very good improvement can be achieved in the current gain of lateral transistors with the help of a properly biased field plate over the base region.

4 Discussions and conclusions

It is shown that the introduction of a properly biased field plate over most of the base surface extending from the collector-base edge should enhance the current gain of vertical and lateral transistors. The field plate extending over the collector and ending within one or two micrometers from the emitter-base junction can be easily attained by the present-day techniques of shadow-masking metallisation. A fairly thick electroless plated metal contact over the emitter region should serve the purpose of casting a shadow during

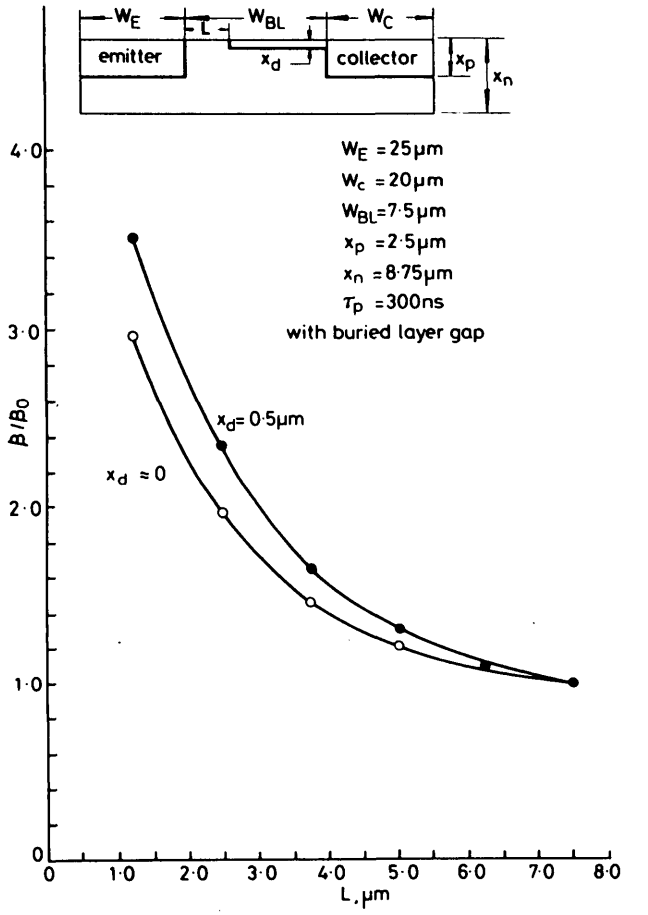

Fig. 5 *Normalised current gain of lateral p-n-p transistor as a function of the spacing L between the emitter edge and the field plate for two values of the depletion layer width X_d*

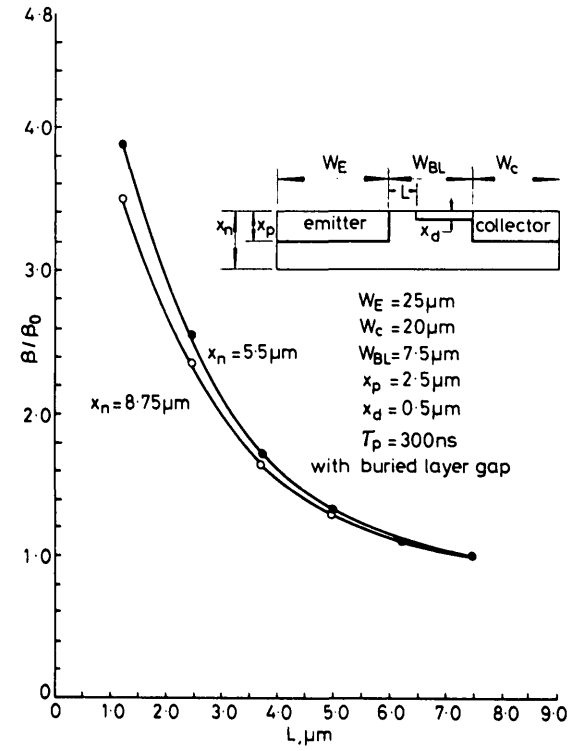

Fig. 6 *Normalised current gain of lateral p-n-p transistor as a function of the spacing L between the emitter edge and field plate for two values of epilayer thickness X_n*

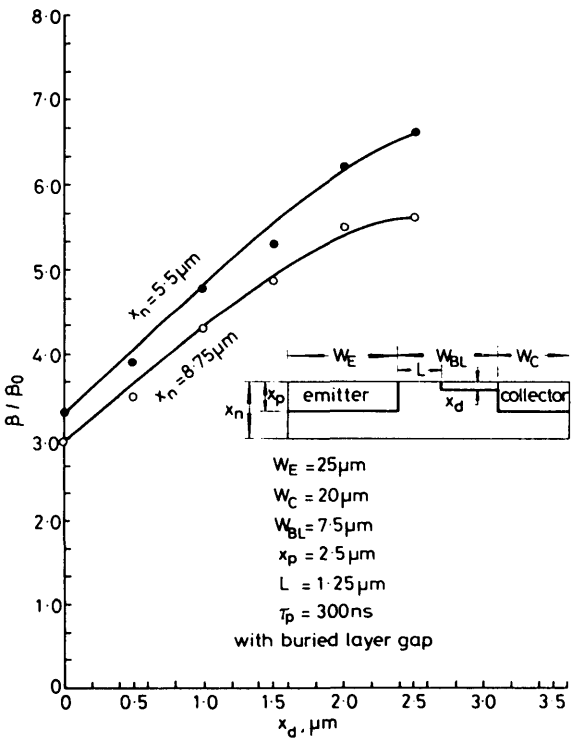

Fig. 7 *Normalised current gain of lateral p-n-p transistor as a function of the depletion layer width X_d under the field plate for two values of the epilayer thickness X_n*

the metallisation and this can keep the field plate close to the emitter (see Fig. 8).

It is essential that the field plate overlaps the collector region. In the *n-p-n* transistor, the field plate can be directly connected to the most positive voltage in the circuit so that the region below the field plate is always kept depleted. Similarly, in the *p-n-p* case, it can be connected to the most negative voltage.

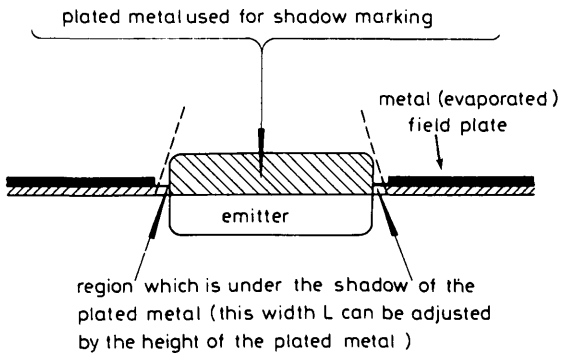

Fig. 8 *Electroless plated metal on the emitter for using as a shadow mask during evaporation of metal for the field plate.*

The boundary conditions simulated by us are those in which the field plate produces a depletion region. This, however, includes the situation when the surface is inverted because below the inversion layer there will be a depletion layer and the boundary conditions we have simulated still hold good. In practice, when the field plate in connected to the most positive voltage in the circuit (in the *n-p-n* case), the situation will be inversion layer followed by depletion layer. The width of this depletion layer will be constant and any signal-level variation reflected on the voltage of the field plate will not reflect upon the depletion-layer width and hence upon the current gain.

The case of surface accumulation under the field plate is similar to the one without a field plate and this situation will not give rise to any improvement in the current gain of transistors. On the contrary it will reduce the collector-base reverse-breakdown voltage V_{Cb0}.

A comparison of our results with the lateral *p-n-p* transistors with the relevant results of Lindmayer's work shows that the improvement factor β/β_0 that can be achieved with the present structure is comparable to the one achieved in his experimental transistor. Lindmayer's transistor makes use of the field effect modulation and hence the increase in current gain is achieved if the gate is connected to the base. The improvement in β of the structure proposed in this paper does not depend upon the field-effect modulation and the field plate need not be connected to the base. The collector-base breakdown voltage V_{cb0} and the collector-emitter breakdown voltage V_{ce0} of the present structure will not be affected by the field plate because the collector base voltage causes changes in the depletion layer around the junction only and the depletion layer below the field plate is not affected by this voltage.

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