High-Performance Bulk MOSFETs: Optimization of Device Characteristics and Series Resistance

Zhixin Alice Ye, Graduate Student, UC Berkeley

Abstract—In the 20 nm gate length, device series resistance becomes an increasing concern. Simulations were conducted on a high-performance bulk MOSFET to investigate how an optimized doping profile of a bulk device is able to impact series resistance and device performance. It was found that the device overall was able to meet the majority of ITRS requirements, though overall on current, $I_{on}$, was not met due to lack of strain implementation. Through optimization of the source drain extension profile, the tradeoffs between the tip resistance and spreading resistance through the LDD to the channel was investigated.

Index Terms—Bulk device, high performance MOSFET, 20nm gate length, high-k dielectric, metal gate, retrograde doping, series resistance.

I. INTRODUCTION

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ith scaling down the size of transistors, it is increasingly important to consider series resistance in order to optimize overall circuit performance. Parasitics including series resistance and overlap capacitance have a large impact on circuit delay; thus for overall improved circuit performance, devices should be optimized for both parasitics and series resistance. In this paper, a 20nm NMOS device was simulated in Sentaurus and optimized to have good device characteristics. Then, the series resistance of the device was studied, and the LDD doping profile concentration and junction abruptness were investigated to understand their impact on series resistance. Antimony was then used in processing simulations to attempt to simulate abrupt doping junctions and observe these effects on tip resistance.

Series resistance of a bulk MOSFET can be broken down into several different components, as illustrated in Figure 1 [1]:

- Contact resistance, $R_{co}$, which is defined as the resistance of the top metal or silicide and the diffusion underneath the leading edge of the contact. $R_{co}$ can be calculated using the following equation:

$$R_{co} = \frac{\sqrt{\rho_{d} \rho_c}}{W} \times \coth(l \sqrt{\frac{\rho_{d}}{\rho_c}})$$

Here, $\rho_d$ is the resistivity of the n+ or p+ doped silicon underneath the contact. $\rho_c$ is the resistivity of the metal or silicide, $l$ is the contact window length, and $W$ is the width of the transistor.

- Diffusion sheet resistance, $R_{sh}$, which can be measured through a number of methods. One methodology is to express $R_{sh}$ as:

$$R_{sh} = \frac{\rho S}{W X_j}$$

where $\rho$ is the average bulk resistivity of the n+ or p+ layer, $X_j$ is the junction depth, $S$ is the spacing between contact and next resistance component. For the case of a shallow source drain extension, the sheet resistance of the deep source and drain must be calculated separately from the extension.

- Tip resistance, which is broken down further into spreading resistance, $R_{sp}$, and accumulation layer resistance, $R_{ac}$, which includes the overlap between the doping layer and the gate oxide [2]. These resistances are considered together because the gradual change in resistivity in practical devices would impact both the accumulation layer and location of current spreading. Tip resistance is considered to be a strong function of the gradient of the doping profile ($\alpha e^{Kx}$), and is considered to be a large percentage of the total series resistance.

Fig. 1. Major components of series resistance through the path of current from contact to the channel [1].

Based on the above components, various options for minimizing series resistance can be explored. In this paper, the area of silicide in the contact was varied to examine impact on contact resistance, the location of the source/drain was varied to examine sheet resistance, and the LDD profile gradient was changed to study tip resistance. Overall series resistance can then be improved by then reducing each of these factors.
II. Fabrication Process

The process flow for the optimized device used a high-performance CMOS process without the implementation of strain, as shown in Fig 2. Ion implantation of indium on a p-type wafer at 35 keV and dose of 5.0e13 cm\(^{-2}\) was used to create a steep retrograde channel doping [4]. 2 nm of oxide was deposited followed by 60 nm of polysilicon, which was then anisotropically etched in RIE to form a dummy gate. A lightly doped drain was formed using ion implantation of arsenic at 2 keV and 2e14 cm\(^{-2}\) dose. Then, a 10 nm nitride spacer was used to implant the self-aligned source and drain, which used ion implantation at 3 keV and 1e17 cm\(^{-2}\) dose. A second gate-drain implant was used to suppress leakage paths underneath the source and drain, with an energy 36 keV and a dose of 1.3e14 cm\(^{-2}\). Activation of dopants was conducted through a 900°C anneal for 1ms at the end, similar to laser annealing [5]. A 42 nm thick nickel silicide was then grown and filled with aluminum.

A 2 nm oxide was deposited and flattened with CMP. The dummy gate and oxide was replaced with hafnium oxide with a K of 12.5, and titanium nitride as the metal. Contacts were etched and filled with aluminum.

Strain was not implemented due to project constraints, and halo doping was not implemented in the end because the retrograde doping was found to be sufficient to suppress punchthrough. Extensions were implanted in both the source and drain as opposed to just the drain to simplify fabrication implementation, though at the expense of potential improvement in series resistance.

Overall, a summary of the most important metrics are provided as listed in Table I, drawing primarily from ITRS 2013 HP specifications.

III. Meeting Target Specifications

A. Design Considerations

During the initial device optimization, various design choices were investigated to understand their impact.

1) Source Drain Extension: Firstly, shallow source drain extensions were included to improve gate control of the channel compared to a deep source drain. The implants were optimized to minimize gate overlap while still keeping a high doping concentration to improve on current.

2) Spacer Size: In order to determine the length of the source drain extension, a spacer was used to move the source and drain further away from the gate, preventing subsurface punch through. It was found that 0.010 nm was the optimal length for the spacer.

3) Deep Source Drain: The source and drain doping was optimized to keep a relatively small X\(_j\) for reduced characteristic length, but heavy doping concentration was used to improve on current.

4) Halo Distribution: To prevent sub-surface punchthrough when the device is in saturation, pocket implants were used. A peak concentration of around 6e10\(^{18}\) was used as per ITRS. Several different halo shapes were considered by optimizing the angle implant, dosage, and energy; however in the end a retrograde doping profile was preferred because it served to suppress punchthrough while simultaneously maintaining subthreshold slope.

5) Retrograde Doping Profile: Indium was used as an implantation ion because its heavy mass allowed a sharper retrograde doping profile compared to boron and BF\(_2\). The lighter channel doping allows for pinning of the width of the depletion layer, thus preventing subthreshold slope degradation when the device is in saturation. One drawback to using indium is that it reaches its solid solubility limit at a lower concentration than boron, so the maximum active doping is decreased, as illustrated in Fig 3.

6) Metal Workfunction: The workfunction of the metal was selected to be 4.15 eV to shift the threshold voltage of the device to 0.2V as per ITRS requirements.

7) Gate Oxide: A high k dielectric was used, HFO2, with a k of 12.5 (insert reference here!), which reduces gate capacitance, since it allows for a thicker oxide.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated Value</th>
<th>Specified Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L_{\text{effective}})</td>
<td>15.5 nm</td>
<td>16 nm</td>
</tr>
<tr>
<td>(L_{\text{metalurgical}})</td>
<td>20 nm</td>
<td>20 nm</td>
</tr>
<tr>
<td>(I_{\text{ox}})</td>
<td>522 Angstroms</td>
<td>600 Angstroms</td>
</tr>
<tr>
<td>(x_{\text{extension}})</td>
<td>9.6 nm</td>
<td>Optimized</td>
</tr>
<tr>
<td>(X_{\text{deepSD}})</td>
<td>18.7 um</td>
<td>Optimized</td>
</tr>
<tr>
<td>(I_{\text{on}})</td>
<td>0.555 mA/um</td>
<td>1.366 mA/um</td>
</tr>
<tr>
<td>(I_{\text{off}})</td>
<td>186 nA/um</td>
<td>100 nA/um</td>
</tr>
<tr>
<td>(V_{\text{Tth}})</td>
<td>0.405V</td>
<td>0.306 V</td>
</tr>
<tr>
<td>(V_{\text{Fsat}})</td>
<td>0.389V</td>
<td>0.219V</td>
</tr>
<tr>
<td>DIBL</td>
<td>154 mV/um</td>
<td>134 mV/um</td>
</tr>
<tr>
<td>SS</td>
<td>121 mV/dec</td>
<td>Optimized</td>
</tr>
</tbody>
</table>
**B. Electrical Characterization and Performance**

The device characteristics were plotted for this optimized device as shown in Figures 4-5. From the transfer characteristics, some leakage current is observed when the device is in saturation. This could potentially be due to tunneling current between the source and drain near the channel. Some subthreshold slope degradation is observed as well between the linear and saturation region, indicating that there may be punchthrough through the device. This could be improved by optimizing the halo implants or else improving the retrograde doping profile. The DIBL was measured to be 154 mV/V and could be improved by reducing the LDD or drain junction size.

**IV. Series Resistance Analysis**

Series resistance was measured by plotting the electrical potential across the device from contact to channel, as shown in Figure 6. Resistance for each component was found by measuring the drop in potential across each resistive component, and then dividing by the saturation current. A separate vertical cross section was taken of the device to calculate the contact resistance. In the initial device, the major resistance values were measured as shown in Table II.

From Table II, it can be seen that the largest contribution of series resistance was the tip resistance. This can be considered to be a combination of the contributions of both current crowding and also accumulation resistance from the LDD to the channel. To reduce this resistance, several methods...
were tried, primarily modifying the LDD doping concentration and LDD junction doping abruptness. The effect of doping concentration is shown in Fig 7, where it is generally seen that a lower doping concentration in the LDD appears to decrease the difference in electrostatic profile. For similar conditions of diffusion, a lower difference in doping profile would effectively reduce junction capacitance and thus reduce spreading resistance. On the other hand, the steeper doping profile of the highly-doped LDD would reduce the tip resistance of the device. Overall, however, it can be seen that spreading resistance appears to be the greater contributor to the difference in electrostatic potential.

Fig. 7. Electrostatic potential plots of similar devices from Sentaurus Structure Editor with different maximum doping concentrations. For a high LDD doping (1e22), tip resistance between Y=0.005 to Y=0.008 is reduced, while the spreading resistance from Y=0.01 to Y=0.015 is increased. Since spreading resistance appears to dominate, a higher doping concentration may be preferred.

Analysis of the junction steepness on tip resistance was also directly analyzed by varying the slope of the gaussian doping profile distribution via a Gaussian Spread Factor, as shown in Figure 8. A small spreading factor represents a Gaussian distribution with a small variance or sigma. In this case, the slope in the LDD near the metallurgical junction is located immediately below Y=0.01. Here it can be seen that a small Gaussian Spread Factor will result in a less steep slope, again indicating that tip resistance is improved. However, again the spreading resistance displays a tradeoff in overall series resistance.

V. PROCESS IMPLEMENTATION OF SERIES RESISTANCE IMPROVEMENTS

In order to reimplement the series resistance studies on the lightly doped drain into a process simulation, Antimony was used as the ionized dopant in the LDD instead of Arsenic. The heavier atomic number of antimony would theoretically reduce the diffusion coefficients and therefore produce a more abrupt junction. However, it was found that the diffusion of Antimony could not reach as high net doping concentrations as Arsenic, resulting in minor degradation of device on current. The impact on series resistance can still be analyzed. Comparing the doping profiles in Fig 9 to the electrostatic potential plot in Fig 10, it can be seen that there is a relatively steep junction in the Antimony LDD device between the drain and the extension at approximately Y=-0.015 um. Here, it can be seen that while the tip resistance may have decreased, the overall electrostatic potential drop for the antimony LDD is higher, indicating a higher series resistance. This can be explained as a function of spreading resistance, which would be increased due to the limited amount of carriers that are available to conduct current, causing some crowding at the source-drain and LDD interface.

VI. DISCUSSION

Comparing the three devices produced between the original optimized device, the series-resistance optimized device, and the re-implementation, we can see that the overall device characteristics were not significantly different from each other. The Sentaurus Process devices both have some leakage in saturation, indicating that there are some potential leakage paths that are not captured in the Sentaurus Device simulation. The Sentaurus Device simulation also has a poorer subthreshold slope and degraded on current; this may be improved by further refining the simulation source drain extension and retrograde doping profile to match that of the Sentaurus Process structures. The implementation of Arsenic in the structure was not found to be particularly effective, since device characteristics were slightly degraded and series

<table>
<thead>
<tr>
<th>Table II</th>
<th>Measured Series Resistance Values for the Initial Device</th>
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<tbody>
<tr>
<td>Resistance</td>
<td>Value (Ω - um)</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>54.05</td>
</tr>
<tr>
<td>Deep Source Drain Diffusion</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>Spreading from Source Drain to Extension</td>
<td>42.34</td>
</tr>
<tr>
<td>Shallow Extension Diffusion</td>
<td>11.8</td>
</tr>
<tr>
<td>Tip Resistance</td>
<td>498.16</td>
</tr>
</tbody>
</table>
Due to time constraints a number of variations on series resistance were not studied and implemented. However, it would be expected that making additional tuning to the $x_{j,ext}$, doping abruptness, and doping concentration of the LDD would be able to improve tip resistance. Compared to the original optimized device, most of the changes made in the studies of series resistance may also have an impact on device performance before developing device structures. With careful optimization, it is possible to develop devices that both perform well and minimize parasitics. Some examples of future investigation can include studying the impact of a one-sided LDD, raised source drain, or improved silicide deposition on series resistance and device performance, as well as implementing additional process steps to emulate studies conducted on the series resistance.

**VII. CONCLUSION**

Through analysis of various devices, a deeper understanding of the tradeoffs between different components of series resistance and device performance were understood. Since overall tip and spreading resistance dominate in series resistance of a device, it is crucial for device engineers to carefully consider the tradeoffs between device performance and different forms of series resistance before developing device structures. With careful optimization, it is possible to develop devices that both perform well and minimize parasitics. Some examples of future investigation can include studying the impact of a one-sided LDD, raised source drain, or improved silicide deposition on series resistance and device performance, as well as implementing additional process steps to emulate studies conducted on the series resistance.

**REFERENCES**


