ABC and ABmC Entering HWMCC'08

Robert Brayton Michael Case Aaron Hurst Alan Mishchenko

Department of Electrical Engineering & Computer Sciences, University of California, Berkeley
{brayton, casem, ahurst, alanmi}@eecs.berkeley.edu

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Abstract

This white paper outlines the unbounded and bounded model checkers (ABC and ABmC, respectively) entering Hardware Model Checking Competition 2008 (HWMCC'08), organized as a satellite event to the 20th International Conference on Computer-Aided Verification (CAV'08) held in Princeton, USA, on July 7-14, 2008.

Description

Our model checkers derive their names from the system for sequential synthesis and verification under development at Berkeley [1]. It has been shown that sequential synthesis and verification are closely related [3]. The proposed model checkers use this observation by applying a set of synergistic transforms, intending to solve the verification problem or to synthesize it down, hoping it is solved by the subsequent steps.

The integrated model checker (ABC) combines the following transforms: combinational equivalence checking [12], improved bounded model checking [8], phase-abstraction [2], minimum-register retiming with the guaranteed equivalent initial state [7], AIG-based combinational logic synthesis [11], *k*-step induction with speculative reduction [14][9], interpolation [10], and BDD-based reachability with non-linear quantification scheduling [4]. The overall pseudo-code of the model checker is discussed in [13].

The bounded model checker (ABmC) performs AIG-based synthesis, the AIG-to-CNF conversion using technology mapping [6], followed by a sequence of incremental runs of a SAT solver.

The SAT solver called internally is MiniSat-C_v1.14.1 [5], with an added capability to store learned clauses for the use in interpolation and unsatisfiable-core computation.

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