Design for Manufacturability and Power Estimation

Lecture 25
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Thanks to Prof. Jan Rabaey and Prof. K. Keutzer

Physical issues verification (DSM)

- Interconnects
- Signal Integrity
  - P/G integrity
  - Substrate coupling
  - Crosstalk
- Parasitic Extraction
- Reduced Order Modeling
- Manufacturability
- Power Estimation
Outline

• Design for Manufacturability
  – Yield
    • Parametric Yield
    • Defect-related yield
  – Statistical Design

• Power Estimation
  – Power consumption mechanisms
  – Different level of abstraction
  – Static or dynamic analysis

Physical issues verification (DSM) Manufacturability

• IC manufacturing process is affected by random disturbances
  – different silicon dioxide growth rates,
    mask misalignment, drift of fabrication equipment operation, etc….

• These disturbances are often uncontrollable and affect the circuit performance
  – How good is my chips performance?
  – How many of my chips will work?

• Yield: percentage of manufactured products that pass all performance specifications

• Yield loss mechanisms
  – Parametric yield (process variations)
  – Defect-related yield (defects)
Parametric Yield
Process variations

Process Variations – SPICE model

- Process variations are reflected into a statistical SPICE model
  - Usually only a few parameters have a statistical distribution (e.g. \{\Delta L, \Delta W, T_{OX}, V_{Th}, V_{TP}\}) and the others are set to a nominal value
  - The nominal SPICE model is obtained by setting the statistical parameters to their nominal value
Global Variations (Inter-die)

Process variations $\Rightarrow$ Performance variations

Critical path delay of a 16-bit adder

All devices have the same set of model parameters value

Local Variations (Intra-die)

- Each device instance has a slightly different set of model parameter values (aka device mismatch)
- The performance of some analog circuits strongly depends on the degree of matching of device properties
- Digital circuits are in general more immune to mismatch, but clock distribution network is sensitive (clock skew)
Statistical Design

• Need to account for process variations during design phase

• Statistical design
  – Nominal design
  – Yield optimization
  – Design centering
Design for Manufacturability (DFM) Approaches

1) Worst-Case Approach: choose the SPICE model giving the worst possible behavior
   - Traditional choice is pessimistic and lead to circuit overdesign (neglects any kind of correlation)
   - Other techniques to choose the SPICE model values (accounting for correlation)

2) Probability Density Function Approach: keep track of the whole distribution
   - Expensive: need smart ways to do it

Defect-related Yield

Manufacturing process may introduce some defects in the layout

Defect-related Yield
Defect-layout relationship

- Yield in terms of area and design rules
  - Larger area $\rightarrow$ lower yield
  - Smaller geometries $\rightarrow$ higher sensitivity to defects
  $\Rightarrow$ trade-off: yield loss must be expressed in terms of the defect size and layout characteristics rather than in terms of area alone

Defect-related Yield
Critical area

- Model relationship between defect characteristics (density and size distribution) and the probability of the defect
- The critical area, for a defect radius $R$, is defined as the area on the layout where, if the center of a defect is deposited a fault occurs:

Physical issues verification (DSM) Power Estimation

- Higher speed and shrinking geometries
  - Increased power consumption and heat dissipation
    - Higher packaging costs
  - Higher on-chip electric field
    - Decreased reliability

⇒ power dissipation of VLSI circuits becomes a critical concern

⇒ Accurate and efficient power estimation (and optimization) techniques are required

Low Power Challenges

- Multifaceted approach adopted:
  - Reducing chip capacitance through process scaling
  - Reducing voltage
  - Employing better architectural and circuit design techniques

From 2D to 3D optimization problem

Power and Synthesis Flow

- Behavioral
- RTL
- Gate
- Switch

Potential for Power Savings vs. Accuracy of Power Estimation

Design Abstraction Levels

- HDL
- Behavioral Synthesis
- RTL Synthesis
- Logic Optimization
- Transistor Optimization
- Place & Route

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Power Consumption Mechanisms in CMOS

- **Static Consumption**
  - Small component (increasing importance for DSM)
  - Leakage diodes and transistors

- **Dynamic Consumption**
  - Due to load capacitance
    - Largest component
  - Due to direct-path currents

CMOS Power Consumption Mechanisms

**Static consumption**

- Ideally zero
- Due to:
  - Leakage current through reverse biased diode junction between source (or drain) and the substrate
  - Subthreshold current of the transistor

\[
P_{stat} = I_{leak} V_{DD}
\]
CMOS Power Consumption Mechanisms
Dynamic consumption – Load Capacitance

- Major component
- Energy/transition:
  \[ P_{\text{dyn}} = C_L \cdot V_{\text{dd}}^2 \cdot f \]
  if the gate is switched on and off \( f \) times per second
- Note: it is not a function of gate size!

CMOS Power Consumption Mechanisms
Dynamic consumption – Switching activity

- Consider switching a CMOS gate for \( N \) clock cycles
  \[ E_N = C_L \cdot V_{\text{dd}}^2 \cdot n(N) \]
  \( E_N \): the energy consumed for \( N \) clock cycles
  \( n(N) \): the number of 0->1 transition in \( N \) clock cycles

\[
P_{\text{avg}} = \lim_{N \to \infty} \frac{E_N}{N} \cdot f_{\text{clk}} = \left( \lim_{N \to \infty} \frac{n(N)}{N} \right) \cdot C_L \cdot V_{\text{dd}}^2 \cdot f_{\text{clk}}
\]

\[
\alpha_{0 \to 1} = \lim_{N \to \infty} \frac{n(N)}{N}
\]

\( \alpha_{0 \to 1} \) is called the switching activity
\( C_{\text{eff}} = \alpha_{0 \to 1} \cdot C_L \) is called the effective capacitance
CMOS Power Consumption Mechanisms
Dynamic consumption – Short Circuit current

• Ideally zero
• Not zero since rise and fall time \( t_r \) and \( t_f \) are not zero
• Power=Energy/transition:

\[
P_c = I_{\text{peak}} \cdot V_{DD} \cdot \left( \frac{t_r + t_f}{2} \right) \cdot f
\]
– if the gate is switched on and off \( f \) times per second
– \( I_{\text{peak}} \) determined by the saturation current of the devices
Power Estimation

Dynamic Analysis

• Simulation
  – requires representative simulation vectors
    • Derived by designer
    • Automatic (Monte Carlo)

• Transistor level (PowerMill)
  – Very accurate
  – Much faster than SPICE

• Gate level (Powergate, DesignPower)
  – Faster than transistor level
  – Still very accurate due to good modeling of power
dissipation at cell-level

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Power Estimation

Static Analysis

• Propagation of switching probabilities
  – No input vectors needed
  – Much faster than simulation
  – Less accurate than simulation
    • Hard to model real delays
    • Glitches?
**Power Estimation**

Static Analysis – Probability Propagation

**AND gate**

sp(1) = sp1 * sp2

\[ tp(0 \rightarrow 1) = sp \times (1 - sp) \]

**Example**

\[ sp = 0.5 \times 0.5 = 0.25 \]

\[ tp = 0.25 \times (1 - 0.25) = 0.1875 \]

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**Power Estimation**

Static Analysis – Probability Propagation

<table>
<thead>
<tr>
<th></th>
<th>( P_{0 \rightarrow 1} )</th>
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<tbody>
<tr>
<td>AND</td>
<td>((1 - P_A P_B)P_A P_B)</td>
</tr>
<tr>
<td>OR</td>
<td>((1 - P_A)(1 - P_B)(1 - (1 - P_A)(1 - P_B)))</td>
</tr>
<tr>
<td>EXOR</td>
<td>((1 - (P_A + P_B - 2P_A P_B))(P_A + P_B - 2P_A P_B))</td>
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Switching Activity for Static CMOS Gates

**Switching Activity for Precharged Dynamic Gates**

**Ignores Temporal and Spatial Correlations**

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Power Estimation
Static Analysis – Probability Propagation: Problems

Problem: Reconvergent Fan-out:
Creates spatial correlation between signals

Becomes complex and untractable real fast

Power Optimization

• Supply voltage reduction
  – Most effective: quadratic improvement
  – Implies performance degradation
  – Use of multiple-$V_{DD}$ (not below the sum of thresholds)
  – Increase of leakage current
• Effective capacitance reduction
  – Reduce physical capacitance
  – Reduce switching activity

• True at all levels of abstraction: trade-off between impact on the design and accuracy
Summary

- Design for Manufacturability
  - Yield
    - Parametric Yield
    - Defect-related yield
  - Statistical Design

- Power Estimation
  - Power consumption mechanisms
  - Different level of abstraction
  - Static or dynamic analysis

Class Review

- **Fundamentals of Circuit Simulation**
  - Formulation of circuit equations
  - Solution of linear equations
  - Solution of nonlinear equations
  - Solution of ordinary differential equations
  - Analog Circuits Simulation
  - Analog Hardware Description Languages

- **Digital Systems Verification**
  - Overview
  - Equivalence Checking
  - FastMOS simulation
  - Timing Analysis
  - Hardware Description Languages
  - System C

- **Physical Issues Verification**
  - Interconnects
  - Signal Integrity
  - Parasitic Extraction
  - Reduced Order Modeling
  - Manufacturability
  - Power Estimation