Death, Taxes and Failing Chips

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and TU/Eindhoven
Outline

• “The era of probabilistic design”
• Three aspects of the problem
  – modeling
  – methodology
  – analysis + synthesis
• Characteristics of a good statistical timer
• Our analysis efforts
Catastrophic vs. parametric

Chip behavior in the face of environmental and manufacturing variations

Catastrophic yield loss
- Critical area
- Voronoi diagrams
- Redundant via insertion
- Wire bending/spacing

Parametric or “circuit-limited” yield loss
- Statistical timing
- Yield prediction
- Design centering
- Design for manufacturability

Digital ASICs
Bounded vs. probabilistic analysis

Varying temperature, mean = 25, sigma = 25

[Data courtesy K. Kalafala]
Bounded vs. probabilistic analysis

[Data courtesy K. Kalafala]
Bounded vs. probabilistic analysis

[Data courtesy K. Kalafala]
Bounded vs. probabilistic analysis

Yield vs. Slack

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The era of probabilistic design

[T. Karnik, S. Borkar, V. De, ICCAD 2002]
Statistical timer

- Netlist + assertions
- Delay and slew models
- Statistics of the sources of variability
- Dependence on sources of variability

1. Yield curve
2. Diagnostics
The full picture

Modeling

Methodology

Analysis
Methodology

- Process models
- Transistor models
- Gate delay models
- Static timing

- Statistical process models
- Statistical transistor models
- Statistical gate delay models
- Statistical static timing
## Methodology issues

<table>
<thead>
<tr>
<th>ASIC</th>
<th>Microprocessor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>No at-speed test, often no AC test</strong></td>
<td>Sorted</td>
</tr>
<tr>
<td><strong>Large, flat</strong></td>
<td>Hierarchical</td>
</tr>
<tr>
<td><strong>Library-based</strong></td>
<td>Custom circuits and library-based</td>
</tr>
<tr>
<td><strong>Focus on worst-case timing</strong></td>
<td>Focus on nominal (and best case!) timing</td>
</tr>
</tbody>
</table>
Definition of yield

• Risk management
  – with PSROs (Performance-Sensitive Ring Oscillators) and appropriate sign-off criteria
  – at multiple levels
  – with/without AC or at-speed test

• Environmental vs. manufacturing variations
  – require 100% yield in environmental window
  – guaranteed 100% yield in the manufacturing window is overkill
Other methodology implications

• Number of timing runs is excessive
  – early and late mode
  – LCD (Linear Combination of Delay) or “interval delay” to model ACLV
  – CPPR (Common Path Pessimism Removal)
  – NBTI (Negative Bias Temperature Instability)
  – BEOL variations
  – coupling noise

Opportunity!
Design methods

• Examples:
  – adaptive body bias
  – mixing of logic families
Modeling

- What are the sources of variation that really matter?
  - mathematical vs. empirical answers
- What are the means, deviations and correlations of the sources of variation?
- What is the dependence of the delay and slew of each edge of the timing graph to each source of variation? Is this computed during the library characterization?
- What about custom circuits?
Analysis wish list
Number 1: path sharing
Number 2: clock correlation
Number 2: clock correlation

• Importance of correlations
  – consider a circuit with 50K latches, each with a setup and hold test, each of which has a 99.99% probability of being met
  – if all tests are perfectly correlated, yield=99.99%
  – if all tests are perfectly independent, yield is 0.005%
  – the truth is closer to the perfectly correlated case!
Number 3: global correlation
Number 3: global correlation
Number 4: bounded vs. statistical

- Bounded
  - input vectors
  - environmental variables
  - PLL jitter

- Statistical
  - manufacturing parameters
  - coupling noise?

- Should be easy to switch between columns

- Large vs. small number of random variables
Number 5: slew/load dependence
Number 6: deterministic vs. random ACV

[From M. Orshansky, L. Milor, P. Chen, K. Keutzer, C. Hu, ICCAD 2000]
Number 7: the tail matters!

- Avoid pessimism
- Capture correlations
Numbers 8 and 9

• Number 8
  – fit well with rest of existing methodology
  – reduce number of timing runs required

• Number 9
  – provide diagnostics
### Number 10: flexibility

<table>
<thead>
<tr>
<th><strong>Quick and dirty</strong></th>
<th><strong>Slow and accurate</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>For optimization</strong></td>
<td><strong>For sign-off</strong></td>
</tr>
<tr>
<td><strong>Incremental</strong></td>
<td><strong>Not incremental</strong></td>
</tr>
<tr>
<td><strong>Usually block-based,</strong></td>
<td></td>
</tr>
<tr>
<td><strong>performance-space</strong></td>
<td><strong>Usually path-based,</strong></td>
</tr>
<tr>
<td><strong>methods</strong></td>
<td><strong>parameter-space</strong> methods</td>
</tr>
</tbody>
</table>
Performance-space vs. parameter-space

Feasible region

JPDF of global parameters
Our analysis efforts

- Three slides deleted
- See DAC ’03 submission for details
- Example: reduced run time from 68 hours for repeated EinsTimer runs on a 200K gate ASIC to about 15 minutes
Conclusions

• Brave old world of probabilistic design
• Statistical considerations must influence all stages of design
• Comprehensive solution required encompassing methodology, modeling, analysis, synthesis, test, design methods
• The computation will not prove to be the hard part; if nothing else, Monte Carlo with intelligent sampling will come to the rescue