Resume

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Alan Mishchenko, Ph.D.

Computer Scientist, Researcher, Software Developer

Contact Information

Berkeley Verification and Synthesis Research Center, BVSRC (http://bvsrc.org)
Department of EECS, UC Berkeley, 545F Cory Hall, Berkeley, CA 94720, USA
Email: alanmi at berkeley dot edu Webpage: http://people.eecs.berkeley.edu/~alanmi/

Education

1997	**Ph.D., Computer Science.** Glushkov Institute of Cybernetics, National Academy of Sciences of Ukraine, Kiev, Ukraine
1993	**M.S. in Applied Mathematics (with honors).** Moscow Institute for Physics and Technology, Moscow, Russia
1987	**High-School Education (with honors).** Physical and Mathematical Lyceum, Kiev National University, Kiev, Ukraine

Professional Experience

2002 – present	**Assistant/Associate/Full Research Engineer,** Department of Electrical Engineering and Computer Sciences, UC Berkeley, Berkeley CA
1998 – 2002	**Research Scientist**, Department of Electrical and Computer Engineering, Portland State University, Portland OR
1993 - 1998	**Junior Research Worker**, Glushkov Institute of Cybernetics, National Academy of Sciences of Ukraine, Kiev, Ukraine
1997 - 1998	**Instructor** (part-time), PhysTech Center, Kiev Department of Moscow Institute of Physics and Technology, Kiev, Ukraine

Professional Activities

- Senior member of IEEE
- Reviewer for conferences and technical journals
- Co-teacher of graduate classes at UC Berkeley
- Co-adviser of graduate students at UC Berkeley and other universities
- TPC member at FMCAD 2007, ICCAD 2008-2009, DAC 2010, IWLS 2004-2014

Research Profile

- Architecting and developing ABC: A System for Sequential Synthesis and Verification (https://github.com/berkeley-abc/abc)
- Computationally efficient logic synthesis and formal verification
- Boolean satisfiability and its applications
- Decision diagrams and their applications
- Arithmetic logic synthesis and verification
- Hardware design in Verilog
- High level synthesis
- Machine learning

Selected Publications (16 out of 150+)

1. A. Mishchenko, R. Brayton, A. Petkovska, M. Soeken, L. Amaru, and A. Domic, "**Canonical computation without canonical representation**", *Proc. DAC'18*.
2. A. Q. Dao, N.-Z. Lee, L.-C. Chen, M. P.-H. Lin, J.-H. R. Jiang, A. Mishchenko, and R. Brayton, "**Efficient computation of ECO patch functions**", *Proc. DAC'18*.
3. B. Schmitt, A. Mishchenko, V. Kravets, R. Brayton, and A. Reis, "**Fast-extract with cube hashing**", *Proc. ASP-DAC'17*.
4. H. Savoj, A. Mishchenko, and R. Brayton, "**m-inductive property of logic circuits**", *IEEE TCAD*, Vol. 35(6), June 2016, pp. 919-930.
5. A. Mishchenko, R. Brayton, W. Feng, and J. Greene, "**Technology mapping into general programmable cells**", *Proc. FPGA'15*.
6. A. Mishchenko, "**An introduction to zero-suppressed binary decision diagrams**", Chapter 1 in *'Applications of zero-suppressed decision diagrams'*, T. Sasao and J. T. Butler (eds.), Morgan & Claypool Publishers, December 2014.
7. A. Mishchenko, N. Een, R. Brayton, J. Baumgartner, H. Mony, and P. Nalla, "**GLA: Gate-level absraction revisited**", *Proc. DATE'13*.
8. A. Mishchenko, R. Brayton, S. Jang, and V. Kravets, "**Delay optimization using SOP balancing**", *Proc. ICCAD'11, pp. 375-382*.
9. R. Brayton and A. Mishchenko, "**ABC: An academic industrial-strength verification tool**", *Proc. CAV'10*, Springer, LNCS 6174, pp. 24-40.
10. J.-H. R. Jiang, C.-C. Lee, A. Mishchenko, and C.-Y. R. Huang, "**To SAT or not to SAT: Scalable exploration of functional dependency**", *IEEE Trans. Comp*, April 2010, Vol. 59(4), pp. 457-467.
11. A. Mishchenko, R. Brayton, J.-H. R. Jiang, and S. Jang, "**Scalable don't care based logic optimization and resynthesis**", *Proc. FPGA'09*, pp. 151-160.
12. A. Mishchenko, M. L. Case, R. K. Brayton, and S. Jang, "**Scalable and scalably-verifiable sequential synthesis**", *Proc. ICCAD '08*, pp. 227-233.
13. A. Mishchenko, S. Cho, S. Chatterjee, and R. Brayton, "**Combinational and sequential mapping with priority cuts**", *Proc. ICCAD '07*, pp. 354-361.
14. A. Mishchenko, J. S. Zhang, S. Sinha, J. R. Burch, R. Brayton, and M. Chrzanowska-Jeske, "**Using simulation and satisfiability to compute flexibilities in Boolean networks**", *IEEE Trans. CAD*, Vol. 25(5), May 2006, pp. 743-755. (TCAD Best Paper Award)
15. A. Mishchenko and R. Brayton, "**A theory of non-deterministic networks**, *IEEE Trans. CAD*, Vol. 25(6), June 2006, pp. 977-999.
16. A. Mishchenko. "**Fast computation of symmetries in Boolean functions**", *IEEE Trans. CAD, Vol. 22(11),* November 2003, pp.1588-1593.

Grants and Awards

2003-2018, Research funding from industrial sponsors including Altera, Cadence, IBM, Intel, Mentor, Microsemi, Synopsys, Verific.
2008-2017, Winner of Hardware Model Checking Competitions affiliated with FMCAD and CAV.
2016-2017, Co-advisor of winning teams at ICCAD CAD competitions.
2016, SRC grant "SAT-based methods for scalable synthesis and verification" (three-year - ongoing).
2012, NSF grant "Bit-level formal verification: Keeping pace with industrial needs" (three-year).
2011, SRC grant "A logic synthesis toolbox with enhanced quality and scalability" (three-year).
2011, Semiconductor Research Corporation Technical Excellence Award (with Robert Brayton).
2010, SRC grant "Advancing liveness property verification" (Intel-custom, three-year).
2008, SRC grant "Exploiting synergy of synthesis and verification" (three-year).
2007, NSF grant "Sequentially transparent synthesis" (three-year).
2006, SRC grant "Innovative sequential synthesis and verification" (Intel-custom, three-year).
2005, SRC grant "Synthesis for verification" (three-year).
2001, Intel grant for research in logic structuring and technology-dependent decomposition.