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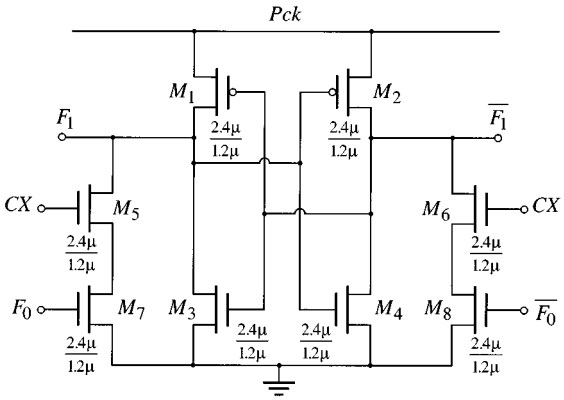

Fig. 1. CAL inverter.

Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply

Dragan Maksimović, Vojin G. Oklobdžija, Borivoje Nikolić, and K. Wayne Current

***Abstract*—The design and experimental evaluation of a clocked adiabatic logic (CAL) is described in this paper. CAL is a dual-rail logic that operates from a single-phase ac power-clock supply. This new low-energy logic makes it possible to integrate all power control circuitry on the chip, resulting in better system efficiency, lower cost, and simpler power distribution. CAL can also be operated from a dc power supply in a nonenergy-recovery mode compatible with standard CMOS logic. In the adiabatic mode, the power-clock supply waveform is generated using an on-chip switching transistor and a small external inductor between the chip and a low-voltage dc supply.**

Circuit operation and performance are evaluated using a chain of inverters realized in a 1.2 μm CMOS technology. Experimental results show that energy savings are achieved at clock frequencies up to about 40 MHz as compared to the nonadiabatic mode. Since CAL can operate both in adiabatic and nonadiabatic modes, power management strategies may be based upon switching between modes when necessary.

***Index Terms*—Adiabatic computing, adiabatic logic, digital CMOS, energy recovery logic, low-power computing.**

I. Introduction

Energy-recovery or "adiabatic" logic circuits have been investigated with the objective of reducing energy consumption of VLSI logic functions [1]–[16]. Weaknesses of previously proposed adiabatic logic circuits approaches include the need for multiphase ac power-clock supplies for proper interfacing between stages, and correspondingly high complexity of both the logic and the required power-clock generator [1]–[9].

This paper describes the design and experimental evaluation of the clocked adiabatic logic (CAL) operated from a single-phase power-clock generator integrated with logic [11]. Operation of the logic is verified over frequency and supply voltage ranges and CAL energy consumption is compared to the case when the logic is operated from a dc power supply in a nonadiabatic mode. To provide proper interfacing between stages, an auxiliary clock, derived from a power clock, is used to enable logic evaluation in alternate logic stages.

CAL circuit configuration and operation are reviewed in Section II. Implementation issues and the test chip are discussed in Section III. Measurement results are presented in Section IV. Section V concludes the paper.

II. Adiabatic Logic with a Single Power Clock

The basic CAL gate, the inverter, is shown in Fig. 1. Cross-coupled CMOS inverters, transistors $M_1 - M_4$, provide the memory function. In order to realize an adiabatic inverter and other logic functions with a single power clock [10], we introduced auxiliary timing control clock signal CX, as shown in Fig. 1. This signal controls transistors M_5 and M_6 that are in series with the logic trees represented by M_7 and M_8. The CX-enabled devices M_5 and M_6 allow operation with a single power clock Pck. In general, the devices M_7 and M_8 can be replaced with NMOS logic trees to perform switching involved in the evaluation of an arbitrary binary function. As an example, implementation of a 2:1 MUX stage is shown in Fig. 2. The CAL topology is similar to the logic proposed by Denker [6], but timing differs significantly.

Idealized CAL timing waveforms are shown in Fig. 3. In the clock period A, the auxiliary clock CX enables the logic evaluation. For $F_0 = 0$, M_8 and M_6 are on, causing $\overline{F_1} = 0$ and M_1 to be on, and thus allowing output F_1 to closely follow the power clock waveform. In the next clock period B, the auxiliary clock $CX = 0$ disables the logic evaluation. The previously stored logic state repeats at the outputs F_1 and $\overline{F_1}$ regardless of the inputs, so that the stage that follows can perform logic evaluation.

System waveforms are shown in Fig. 4. All logic stages are supplied by the same power clock Pck. The logic evaluation is enabled in alternate logic stages by the auxiliary clock CX and its complement $\overline{CX}$, at half the power clock rate. Therefore, CAL takes the new input in every other power clock cycle. Because of the memory function, pipelining is inherent, as in other memory-based adiabatic schemes. The auxiliary clocks drive only MOS transistor gates, so that the additional energy

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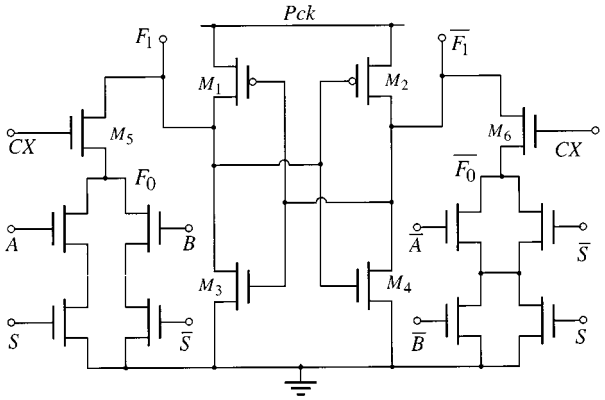

Fig. 2. The 2:1 MUX implemented with CAL.

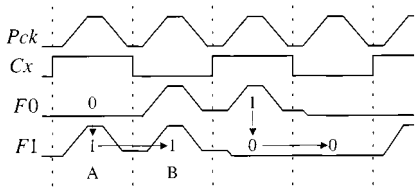

Fig. 3. CAL Inverter waveforms: Pck is power clock, CX is auxiliary clock, $F0$ is the logic input, and $F1$ is the logic output.

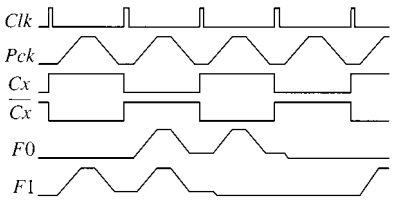

Fig. 4. Idealized system timing waveforms.

loss is minimized by reducing the clock amplitudes. Energy loss could be further reduced by using a high-efficiency resonant clock scheme. The overhead loss is relatively small, especially when more complex logic functions are implemented in logic stages. Since this logic operates with a single power clock, a very simple, power- and area-efficient power clock generator can be applied. The low-power auxiliary clock signals can be distributed using the same techniques used in conventional clocked CMOS. Therefore, power and clock distribution are simpler and more efficient than in multiphase power clock adiabatic logic families [5]–[7]. In addition, it is important to note that CAL can also be operated as a conventional clocked logic with a dc power supply connected to Pck.

III. Implementation of Adiabatic Logic with Integrated Power Clock

In Fig. 5, a cascade of single power clock logic functions, the power clock's switching transistor, and a flip-flop to generate the necessary auxiliary clock signals CX and $\overline{CX}$ are shown. The dotted line indicates the boundary between on- and off-chip components. The dc source is $V_{DD}/2$. The auxiliary clocks, CX and $\overline{CX}$, are obtained easily from the gate drive signal Clk for the switch Q in the power clock generator. Both the gate drive and the auxiliary clocks are 0-to-$V_{DD}/2$ square waves. In [10], the gate-drive amplitude (1.5 V) is very close to the optimum ($2V_t$) value.

Fig. 5 is a block diagram of the experimental CAL chip built as a chain of $n = 736$ dual-rail inverters in 1.2 μm CMOS technology. Fig. 6 shows the test chip die photo.

The device sizes in the CAL logic stages are indicated in Figs. 1 and 5. For testing purposes, 12 of the inverters have both outputs connected to the output pins, via conventional output buffers that serve as voltage comparators. The conventional output buffers and the circuits used to generate the auxiliary clocks are supplied from a separate dc supply V_{DD}. The inductor L and the low-voltage dc source V_B are used for energy-recovery (adiabatic) operation of the CAL chip. The ac power-clock waveform Pck is generated using a single NMOS device Q in parallel with the CAL logic. The device Q is turned on during a small fraction of the clock period at the point when Pck is approximately zero, resulting in the class E mode of operation. During this time, energy is added to sustain oscillation in the resonant circuit formed by the external inductance L and the equivalent logic capacitance C_{eq}. When Q is clocked close to the resonant frequency, Pck swings between *0* and a peak value approximately equal to $2 \cdot V_B$ [11]. The switching transistor Q takes a small fraction of the total chip area, as shown in Fig. 6.

Given a desired power-clock frequency f, the required inductance L can be found from

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

where $C_{eq} = 101$ pF is the measured equivalent chip capacitance at the Pck node. The equivalent chip capacitance was measured by connecting a resistor R between V_B and Pck and by measuring the time constant RC_{eq} of the charge-up transient after the device Q is turned off. The logic can also be operated from a dc supply connected directly to Pck, while the power-clock device Q is disabled. This nonadiabatic mode of operation is used to evaluate how much energy can be recovered by the power clock.

IV. Experimental Results

Operation of the circuit is illustrated by the waveforms shown in Fig. 7 for an input sequence of 1100 and two power-clock frequencies. The pair of quasi-sinusoidal pulses that corresponds to the logic high output is observed as a pair of rectangular pulses through the conventional, dc-supplied output buffers. The signal source limited the maximum operating frequency at which we could test this circuit to 50 MHz. In addition, the external discrete inductor would also limit the maximum clock rate. Higher operating frequencies, up to 167 MHz, are predicted by simulation for the 1.2 μm process [10]. Recently, CAL circuits were simulated in 0.5 μm CMOS by another research group, and were found to be functional at up to 280 MHz [15].

Energy consumption of the CAL chip (excluding the consumption of the output buffers) was measured as a function of frequency for three cases.

1) For adiabatic operation when 3 V peak-to-peak sinusoidal Pck was supplied from an external function generator and the on-chip power-clock device Q was disabled. Energy was measured by measuring a voltage drop on a series resistor connected to the function generator.
2) For adiabatic operation with quasi-sinusoidal Pck generated using $V_B = 1.5$ V and an external L, and by clocking Q as shown in Fig. 5. Energy was measured by measuring a voltage drop on a series resistor connected to the dc power supply.
3) For nonadiabatic operation with the minimum dc supply voltage $V_B = 2.5$ V for which the dc-supplied logic was found to function properly. This supply voltage provides approximately the same noise margins as in the case of ac power clock.

In all three cases, the activity factor (defined as the normalized number of input transitions) is equal to one. The results are shown in Fig. 8. The

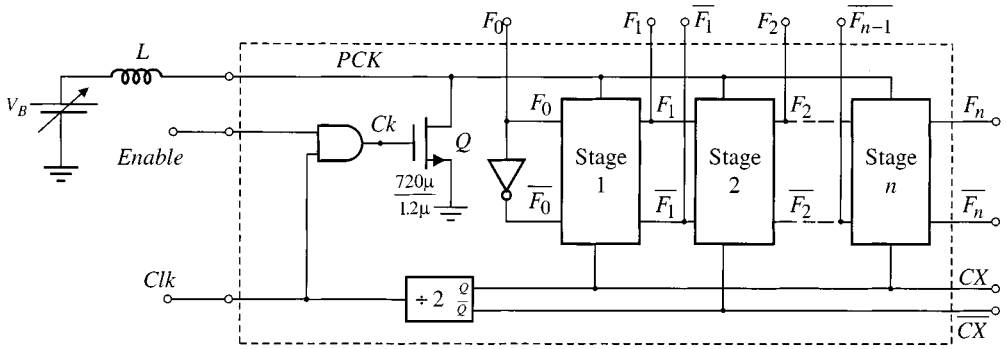

Fig. 5. Chain of CAL logic gates with on-chip power-clock generation. For adiabatic operation, $Enable = 1$, and inductor L is connected between Pck and the dc supply V_B; for nonadiabatic operation, $Enable = 0$ and $Pck = V_B$.

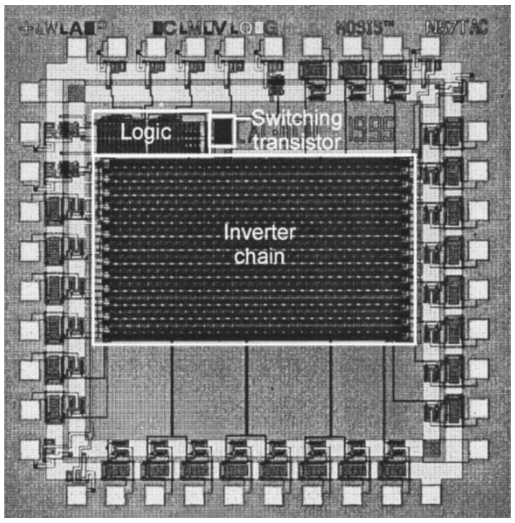

Fig. 6. Test chip die photo.

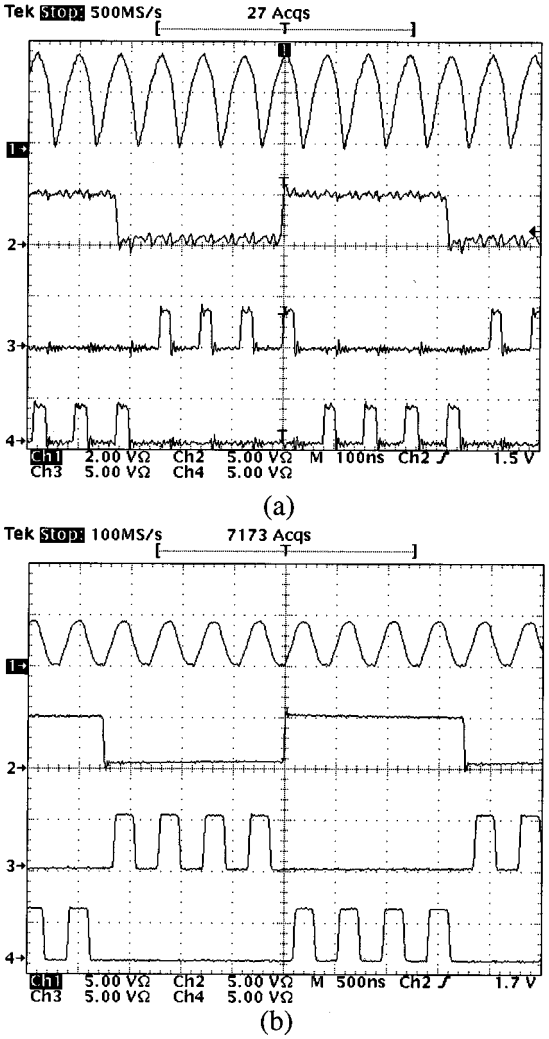

Fig. 7. Measured CAL waveforms: Ch1: power clock Pck, Ch2: logic input F_0, Ch3: buffered logic output F_1, Ch4: buffered complementary logic output for (a) $f = 12.5$ MHz, the logic is supplied from $V_B = 1.8$ V, while the dc supply for the conventional output buffers is $V_{DD} = 4$ V and (b) $f = 2.36$ MHz, the logic is supplied from $V_B = 1.5$ V, the dc supply for the output buffers is $V_{DD} = 5$ V.

nonadiabatic energy consumption is approximately constant at about 0.58 pJ per inverter per cycle. The theoretical nonadiabatic energy consumption, based on the measured $C_{eq} = 101$ pF, is 0.61 pJ per inverter per cycle. The small difference comes from the fact that C_{eq} includes capacitance of the Pck distribution, which is not switched during nonadiabatic operation. These results show that the energy consumption of the CAL operated from the dc supply is indeed equal to CV^2 losses. Therefore, the results in Fig. 8 show how much of the CV^2 can be recovered through the power clock during adiabatic operation of the chip with external or internal power clock. Energy savings are very large at low operating frequencies and diminish as the frequency approaches $f = 30$ MHz. The results with the externally supplied power-clock waveform are significantly better than the results with the internally generated Pck. The losses in the power clock generator are a function of transistor resistance, which was found to be higher than expected. In reported results, switching transistor pulse width was adjusted for minimum energy dissipation.

By changing the activity factor at a constant power-clock frequency, it was found that the CAL power consumption at the activity factor equal to zero is approximately one half of the power consumption at the activity factor equal to one, as shown in Fig. 9. This confirms that at low activity factors nonadiabatic operation from a dc supply can be significantly more efficient.

The CAL ability to operate from either a single-phase ac power-clock supply or from a dc supply opens interesting possibilities to combine adiabatic and nonadiabatic modes of operation to achieve energy-efficient operation for a very wide range of throughput rates and activity factors.

The energy consumption measurements shown in Figs. 8 and 9 included only the part of the circuit operated from the supply V_B: the

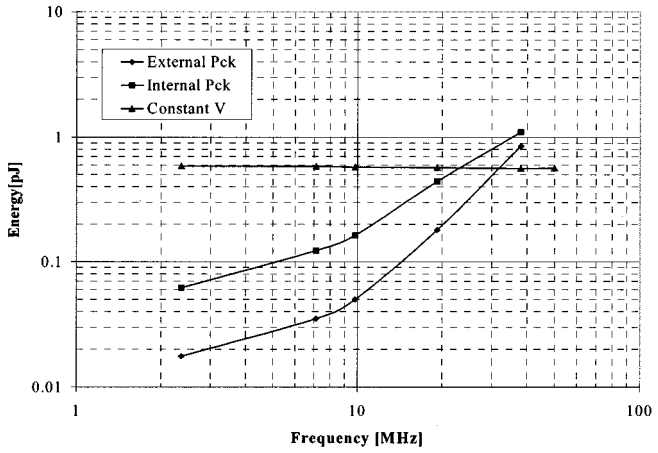

Fig. 8. Energy/inverter per cycle versus frequency.

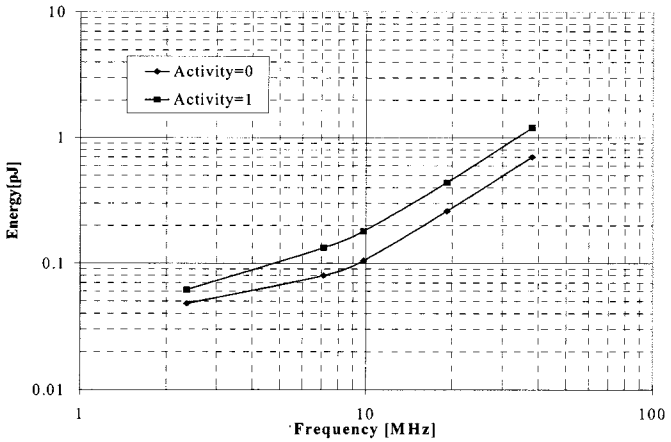

Fig. 9. Energy/inverter versus frequency for different activity factors.

logic and the switching transistor Q. The measured energy consumption per cycle of the circuits supplied from the constant dc voltage $V_{DD} = 1.5$ V (auxiliary clocks and the driver for the switching transistor Q) is about 30 pJ, or about 8% of the total nonadiabatic energy consumption. This low power consumption in the auxiliary clocks is due to reduced voltage swing as well as half frequency operation. However, this consumption becomes significant at low frequencies of operation with externally supplied adiabatic clock. It can be reduced by applying adiabatic switching to auxiliary clocks. Several modifications of CAL that eliminate the need for auxiliary clocks have recently been proposed [15], [16]. Simulation results in [15] show that CAL offers energy savings with respect to standard CMOS, which are comparable to other adiabatic logic families.

V. Conclusion

The proposed clocked adiabatic logic (CAL) operates from a single-phase power-clock supply. The test chip, a chain of inverters, is implemented in a 1.2 μm CMOS technology.

Operation of the logic and its energy consumption are measured for adiabatic operation using an external power-clock generator or using a simple on-chip power-clock generator. These results are compared to the energy consumption measured in nonadiabatic operation when the chip is powered from a dc voltage source. Experimental results show tenfold energy savings in the clock range from 1 MHz to 5 MHz and significant savings at clock rates up to 40 MHz, with power-clock generation included. The CAL ability to operate from either ac power-clock supply or from a conventional dc supply opens further possibilities for energy-efficient operation in a very wide range of throughput rates by combining adiabatic and nonadiabatic modes of operation.

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