Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters

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***Abstract*—We present an adaptive digital technique to calibrate pipelined analog-to-digital converters (ADCs). Rather than achieving linearity by adjustment of analog component values, the new approach infers component errors from conversion results and applies digital postprocessing to correct those results. The scheme proposed here draws close analogy to the channel equalization problem commonly encountered in digital communications. We show that, with the help of a slow but accurate ADC, the proposed code-domain adaptive finite-impulse-response filter is sufficient to remove the effect of component errors including capacitor mismatch, finite op-amp gain, op-amp offset, and sampling-switch-induced offset, provided they are not signal-dependent. The algorithm is all digital, fully adaptive, data-driven, and operates in the background. Strong tradeoffs between accuracy and speed of pipelined ADCs are greatly relaxed in this approach with the aid of digital correction techniques. Analog precision problems are translated into the complexity of digital signal-processing circuits, allowing this approach to benefit from CMOS device scaling in contrast to most conventional correction techniques.**

***Index Terms*—Adaptive digital background calibration, capacitor mismatch, code domain, finite op-amp gain, finite-impulse response (FIR), linear equalizer (LE), least mean square (LMS) algorithm, noise enhancement, pipelined analog-to-digital converter (ADC).**

I. Introduction

CMOS switched-capacitor pipelined analog-to-digital (A/D) converter architecture provides an approach to A/D conversion when high throughput and high resolution must be realized simultaneously [1]. The 1.5-bit/stage architecture [2], [4] is widely used due to its low per-stage complexity and the large feedback factor of its residue amplifier. In the absence of post-fabrication component trimming or calibration, pipelined A/D converter (ADC) accuracy is usually limited to about 10 bit [3]. In addition to the front-end track-and-hold (T/H) bandwidth limitation given a certain IC technology, prominent analog impairments include sampling capacitor mismatch, finite op-amp gain, and switch-induced charge injection errors [1]–[5]. Analog circuit techniques [6]–[11] have long been conceived to treat these imperfections, but the associated penalty is severe: complicated analog circuitry has to be used and the conversion speed is often reduced, not including the fact that analog techniques hardly benefit from CMOS device scaling that has been improving the performance of digital circuits all along.

Digital calibration techniques [12]–[21], albeit presenting major advances in pipelined ADC design, have also proven to be insufficient in that analog signal paths are always disturbed during calibration, independent of being performed in the foreground [12]–[15] or background [16]–[21]. Foreground calibration further suffers from lack of tracking capability, therefore is sensitive to temperature, supply voltage drift and device aging. Tampering with analog signal paths is inevitable for conventional approaches as they all use the "accuracy bootstrapping" algorithm: calibration is performed stage by stage from least-significant-bit (LSB) stage to most-significant-bit (MSB) stage; calibrated lower rank stages are included in the circuit apparatus used to calibrate more significant ones until all stages are exhausted. The sequential operation is cumbersome to implement in practice, as it often requires switching precision analog circuitry in and out of the pipeline during the calibration. This complicates the backend digital control logic and, more importantly, adds overhead to analog circuitry. The complexity associated with calibration is usually translated into either higher power consumption or reduction of conversion speed [12]–[19].

In contrast, this paper presents a new architecture for correcting pipelined ADC errors—analog impairments are treated in analogy to distortion in communication channels; component errors from all stages of the pipeline are removed simultaneously using an adaptive finite-impulse response (FIR) digital filter. The analog signal path is completely intact and thus can maintain maximum conversion speed allowed by certain device technology. This approach can correct dominant memoryless linear errors caused by capacitor mismatch, finite op-amp gain and switch-induced offset errors. By relaxing the stringent requirement on precision matching and high open-loop gain of analog components, the proposed correction technique can be utilized to improve the effective conversion accuracy and conversion speed, and/or to reduce power consumption.

II. Adaptive Digital Calibration Algorithm

An *a priori* model of pipelined ADC errors is essential in developing digital correction techniques. Following a short analysis, we postulate that errors in a pipelined ADC can be modeled as distortion in code domain. This representation is analogous to the distortion in communication channels and therefore can be treated similarly. Following this, we introduce an adaptive

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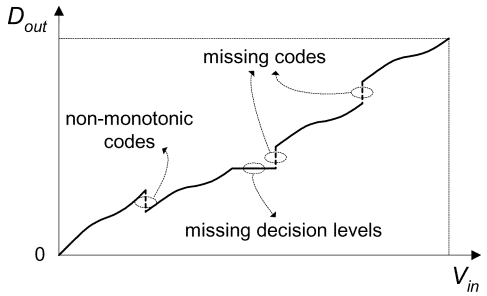

Fig. 1. Typical transfer function of a pipelined ADC.

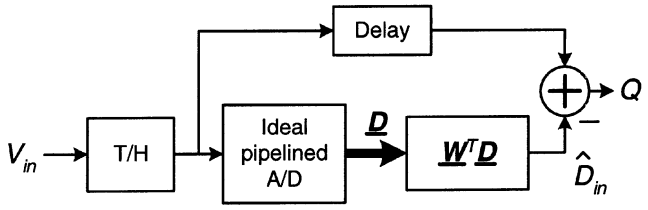

Fig. 2. Ideal pipelined ADC: weighted sum decision making.

linear equalization (LE) technique to remove memoryless linear errors. In this approach, constructing a compact state space for filtering proves to be the key to achieve an efficient calibration. The "channel" postulation is also validated in conjunction with the LE formulation.

A. Nonlinear Channel Model

An ideal N-bit pipelined ADC takes a sampled analog input and converts it into an N-bit binary code subject to quantization errors. The conversion process suffers from analog impairments at various stages. The front-end T/H amplifier has a finite input bandwidth. For analog inputs that contain frequency components other than dc, the T/H amplifier exhibits memory effect and results in harmonic distortion. The higher the input signal frequency, the worse the distortion. Sampling clock jitter is another source of error and its effect is stochastic and is usually quantified as signal-to-noise ratio (SNR) degradation [22].

The pipelined converter following T/H usually suffers from both dynamic and static errors. Finite bandwidth and slew rate of residue amplifiers introduce memory. Capacitor mismatch, finite op-amp gain and nonlinearity, switch-induced charge injection, as well as various sources of offset result in static errors manifesting as differential nonlinearity (DNL), integral nonlinearity (INL), input-referred offset, and overall gain error. Fig. 1 shows a typical pipelined ADC transfer function. It should be emphasized that, even when all circuit components are perfectly linear and memoryless, capacitor mismatch and finite op-amp gain still highly distort the overall transfer function—it assumes a piecewise linear curve with misaligned end-points between segments. These misalignments introduce missing codes and nonmonotonic codes as shown in Fig. 1.

Define a decision code vector $\underline{D} = (\, D_1 \quad D_2 \quad \dots \quad D_N \,)^T$, where D_k is the decision from the kth stage. Shown in Fig. 2, for a typical 1.5-b/stage topology, the final decision $\hat{D}_{\rm in}$ is obtained by taking the inner product of $\underline{D}$ and a weighting vector $\underline{W} = (2^{N-1} \quad 2^{N-2} \quad \cdots \quad 2^0)^T$

$$\hat{D}_{\rm in} = \underline{W}^T \underline{D} = \sum_{k=1}^{N} 2^{N-k} D_k. \tag{1}$$

We recognize (1) as a simple linear transform of the code vector $\underline{D}$. This yields the correct decision when all circuit components are ideal. In this case, the ADC does not introduce distortion (i.e., ideal channel). The output error signal Q in Fig. 2 is quantization error.

A real ADC exhibits nonlinearity and memory effect. A straightforward compensation is to perform Volterra filtering on the digital output $\underline{W}^T\underline{D}$. However, the correct decision cannot be recovered when a multiple-to-one mapping from analog input ($V_{\rm in}$) to digital output ($\underline{W}^T\underline{D}$) occurs (such as nonmonotonic codes) [26]. Furthermore, the misalignment mentioned before in the transfer function can be very problematic—a power series expansion that can closely approximate this would easily involve hundreds of terms.

Since the complexity of a Volterra filter increases geometrically as a function of its order [23]–[26], we conclude that a brute-force Volterra filtering approach is not practical. As an alternative, we postulate that the correct decision $\hat{D}_{\rm in}$ can be obtained by a nonlinear transform of the code vector $\underline{D}$

$$\hat{D}_{\rm in} = f(\underline{D}). \tag{2}$$

This is shown in Fig. 3. The postulation is equivalent to state that analog impairments can be modeled as a code-domain nonlinear "channel" response. Thus, the compensation is to perform equalization correspondingly.

We recognize that (2) is still a form of Volterra filter, but the operand is vector $\underline{D}$ in lieu of the scalar $\underline{W}^T\underline{D}$ (this substitution actually has a profound implication and will become clear after the discussion of sufficient statistics concept). The error e now contains not only the quantization error, but also residual analog impairments that cannot be removed by the equalization. It is important to note that it is a strong argument to assume $\underline{D}$ as a sufficient statistic for $D_{\rm in}(= V_{\rm in}/V_r$, the quantized version of $V_{\rm in})$ when quantization error is ignored. The sufficiency lies in the built-in redundancy of $\{D_k\}$.

B. Code Space and Sufficient Statistics

A unique feature of the pipelined ADC is the large redundancy built into stage decisions $\{D_k\}$ with the intention to combat comparator offset, resulting in the digital error correction (DEC) technique [2], [4]. In a sense, the final decision is not made until the last stage resolves where circuit nonidealities are negligible due to large residue gain accumulated. The redundancy embedded in $\{D_k\}$ is the key that makes digital calibration work.

Omitting quantization noise, $\{D_k\}$ can be interpreted as a binary decomposition of $D_{\rm in}$. The code space of $D_{\rm in}$ is fully spanned by $\{D_k\}$ as long as no missing decision levels (Fig. 1) occur [13]. When this condition holds, $\{D_k\}$ represent a set of sufficient statistics for $D_{\rm in}$, i.e., a purely digital operation performed on $\{D_k\}$ can in theory perfectly recover $D_{\rm in}$ when quantization noise and circuit noise are ignored. The compensation is not susceptible to the problem of inherent segmental nonmonotonicity (multiple-to-one mapping) that is not correctable by direct filtering of $\underline{W}^T\underline{D}$ as pointed out in Section II-A.

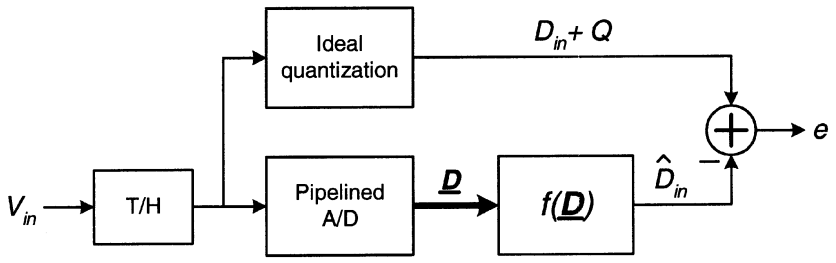

Fig. 3. Error correction of pipelined ADC: code-domain nonlinear "channel" equalizer.

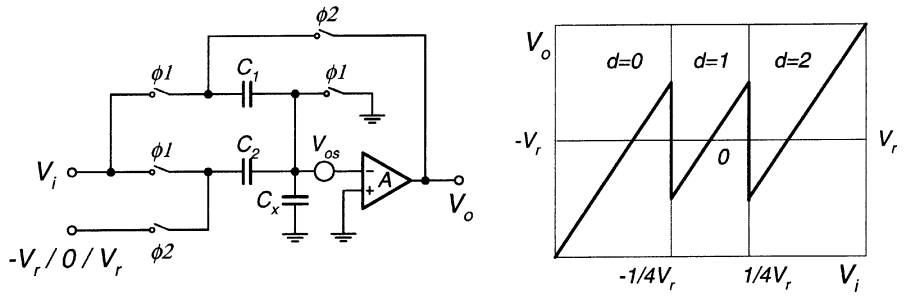

Fig. 4. Residue amplifier of a 1.5-bit/stage pipelined ADC and its voltage transfer function. C_1 and C_2 are sampling capacitors, and C_x is the parasitic capacitor. $V_{\rm os}$ is the input-referred offset voltage of the op-amp.

C. LE Approach

For the rest of the discussion, we focus on the dominant, memoryless linear errors, i.e., the capacitor mismatch, finite op-amp gain, and various switch-induced offsets. Fig. 4 shows the residue amplifier of a typical switched-capacitor 1.5-b/stage pipelined ADC and its voltage transfer function. The residue voltage can be derived as

$$V_o = \frac{V_i(C_1+C_2) - (d-1)V_rC_2 + V_{\rm os}(C_1+C_2+C_x)}{C_1 + \frac{C_1+C_2+C_x}{A}} \tag{3}$$

where V_r is the reference voltage, $V_{\rm os}$ is the input-referred offset voltage of the op-amp, C_x is the virtual ground parasitic capacitance, A is the op-amp dc gain (constant), and d (which takes on a value of 0, 1, or 2) is the decision of the current stage. Equation (3) is equivalent to

$$\begin{aligned} V_i\left(\frac{C_1+C_2}{C_1}\right) &= V_o\left(1+\frac{C_1+C_2+C_x}{C_1}\frac{1}{A}\right) \\ &\quad + V_r\,(d-1)\,\frac{C_2}{C_1} \\ &\quad - V_{os}\left(\frac{C_1+C_2+C_x}{C_1}\right). \end{aligned} \tag{4}$$

If we divide each term by V_r and define $D_i = V_i/V_r$, $D_o = V_o/V_r$, and $D_{\rm os} = V_{\rm os}/V_r$, we obtain a purely digital representation of (4) as

$$\begin{aligned} D_i\left(\frac{C_1+C_2}{C_1}\right) &= D_o\left(1+\frac{C_1+C_2+C_x}{C_1}\frac{1}{A}\right) \\ &\quad + (d-1)\,\frac{C_2}{C_1} \\ &\quad - D_{\rm os}\left(\frac{C_1+C_2+C_x}{C_1}\right). \end{aligned} \tag{5}$$

Equivalently, we can write

$$D_i = D_o\alpha + (d-1)\,\beta - D_{\rm os}\gamma \tag{6}$$

where $\alpha = (C_1/C_1+C_2)\,(1+(C_1+C_2+C_x/C_1)(1/A))$, $\beta = (C_2/C_1+C_2)$, and $\gamma = (C_1+C_2+C_x/C_1+C_2)$. Denote the kth stage input voltage as $D_{i,k} = V_{i,k}/V_r$, the kth stage output voltage as $D_{o,k} = V_{o,k}/V_r$, and the kth stage decision D_k. Note that $D_{i,k} = D_{o,k-1}$. We get a recursive relationship when (6) is applied to each stage in sequence, shown as

$$\begin{aligned} D_{\rm in} = D_{i,1} &= \{[\cdots]\,\alpha_2 + (D_2-1)\beta_2 - D_{os,2}\gamma_2\}\,\alpha_1 \\ &\quad + (D_1-1)\beta_1 - D_{{\rm os},1}\gamma_1 \\ &= (D_1-1)\beta_1 + \cdots + D_{o,N}\alpha_N\cdots\alpha_1 \\ &\quad - D_{{\rm os}1}\gamma_1 - \cdots. \end{aligned} \tag{7}$$

We can express $D_{\rm in}$ as the sum of three terms

$$D_{\rm in} = A + B + \Gamma \tag{8}$$

where

$$\begin{aligned} A &= (D_1-1)\beta_1 + (D_2-1)\beta_2\alpha_1 \\ &\quad + \cdots + (D_{N-1})\beta_N\alpha_{N-1}\cdots\alpha_1 \\ &= \sum_{k=1}^{N}(D_k-1)f_k \\ B &= D_{o,N}\alpha_N\alpha_{N-1}\cdots\alpha_1 \\ &= D_{o,N}\prod_{k=1}^{N}\alpha_k \\ \Gamma &= -D_{{\rm os},1}\gamma_1 - D_{{\rm os},2}\gamma_2\alpha_1 - \cdots \\ &\quad - D_{{\rm os},N}\gamma_N\alpha_{N-1}\ldots\alpha_1 \\ &= -\sum_{k=1}^{N}D_{{\rm os},k}f_{{\rm os},k}. \end{aligned}$$

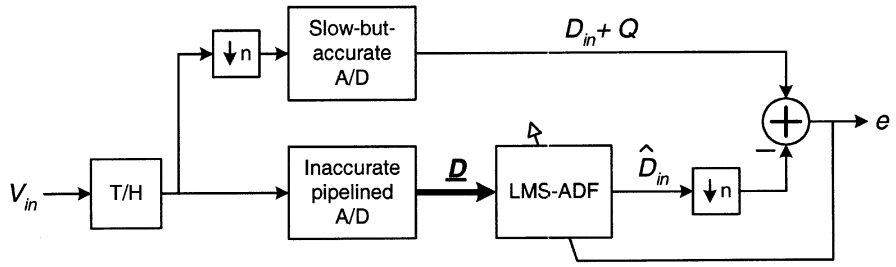

Fig. 5. Error correction of pipelined ADC: code-domain LMS adaptive LE.

TABLE I
CIRCUIT PARAMETERS OF THE 1.5-b/STAGE PIPELINED ADC USED IN THE SIMULATION

Pipeline stage	Sampling cap mismatch	Op-amp DC gain	Op-amp input-referred offset	Comparator offset	Comparator noise	C_x/C_l
1 - 4	20%	50×	10% V_{ref} (3σ)	10% V_{ref} (3σ)	1% V_{ref} (3σ)	40%
5 - 11	1/64 (3σ)	50×	10% V_{ref} (3σ)	10% V_{ref} (3σ)	1% V_{ref} (3σ)	40%

Equation (8) formulates an FIR filter, the core of the LE we are seeking. The first term is the weighted sum of $\{D_k\}$, the second term is quantization error, and the third term is total input-referred offset. The nominal value of α_k's and β_k's is 1/2 and the nominal value of γ_k's is 1. If the ADC is ideal, (8) degenerates into (1) and $f_k = 2^{-k}$.

In reality, the tap values are not known due to mismatch, finite gain, and offset errors; adaptive techniques can be applied to obtain them on the fly. This leads to the adaptive digital background calibration scheme using the steepest gradient descent algorithm shown in Fig. 5: the output vector $\underline{D}$ of a high-speed, inaccurate pipelined ADC is decimated and applied to an adaptive digital filter (ADF); a parallel, slow-but-accurate ADC is used to obtain $D_{\rm in}$; the ADF tap values are updated using a least mean square (LMS) algorithm driven by the error signal $e = D_{\rm in} - \hat{D}_{\rm in}$ and the update is performed at the speed of the slow ADC. After initial acquisition, it is only required to be fast enough to track temperature variation, supply voltage drift, and component aging.

It should be pointed out that the analog signal path of the pipelined ADC is completely intact in this approach, and (8) does not limit the scale of analog impairments that is correctable. The analog overhead is a slow-but-accurate ADC, which can be algorithmic or sigma–delta (Σ/Δ). The digital approach allows this algorithm to benefit from the fast scaling of CMOS devices, translating analog precision problems into the complexity of DSP circuits.

III. SIMULATION RESULTS

To demonstrate the effectiveness of the proposed calibration approach, a 10-bit prototype ADC is simulated. Using this technique, the gain requirement of op-amps can be greatly reduced, and simple and inherently fast amplifier topologies can be used to enhance the conversion speed. To reduce simulation time, the decimation stage is removed, i.e., adaptation is running at the sampling speed of the pipelined ADC. The slow ADC output is 16 b; the pipelined ADC raw output is 12 b; the net resolution after calibration is 10 b. A normalized LMS (nLMS) algorithm [27] is chosen to update the filter taps. The initial parameter setting is listed in Table I.

We first set the sampling capacitor mismatch as shown in Table I and all other circuit components as ideal. The input signal is uniformly distributed on $[-1,\ 1]$. The step size μ of the nLMS adaptation is set to 0.1 ($0 < \mu < 2$ for stability [27]). The learning curve of the algorithm is shown in Fig. 6(a). The mean-square error (MSE) of the system in the steady state is approximately equal to 12-bit quantization noise.

Finite op-amp gain effect is the next impairment examined. Again, all other circuit components are set ideal and the gain is set to 50 ×. The learning curve of the algorithm is shown in Fig. 6(b). The steady-state MSE is close to 11 b. Finally, all static error sources are included in the simulation (Table I). With the same step size, convergence speed is roughly the same as that of the finite gain scenario. The steady-state MSE is approximately equal to 10-bit quantization noise. The system learning curve is shown in Fig. 7(a).

Fig. 8 shows DNL and INL profiles of the ADC before and after calibration. More than half of the codes (at the 10-bit level) are missing before calibration due to large errors in ADC transfer function. After adaptation is complete, linearity errors are reduced to less than ± 1 LSB.

It was found in simulation that input signal statistics have little effect on the convergence rate of the ADF. The learning curves with saw-tooth and sine wave inputs are shown in Fig. 9. Compared to the one with random input (Fig. 6), the difference is rather small.

IV. PERFORMANCE ANALYSIS

In Section II, we formulated a code-domain adaptive filter that compensates linear errors of pipelined ADCs. Comparing

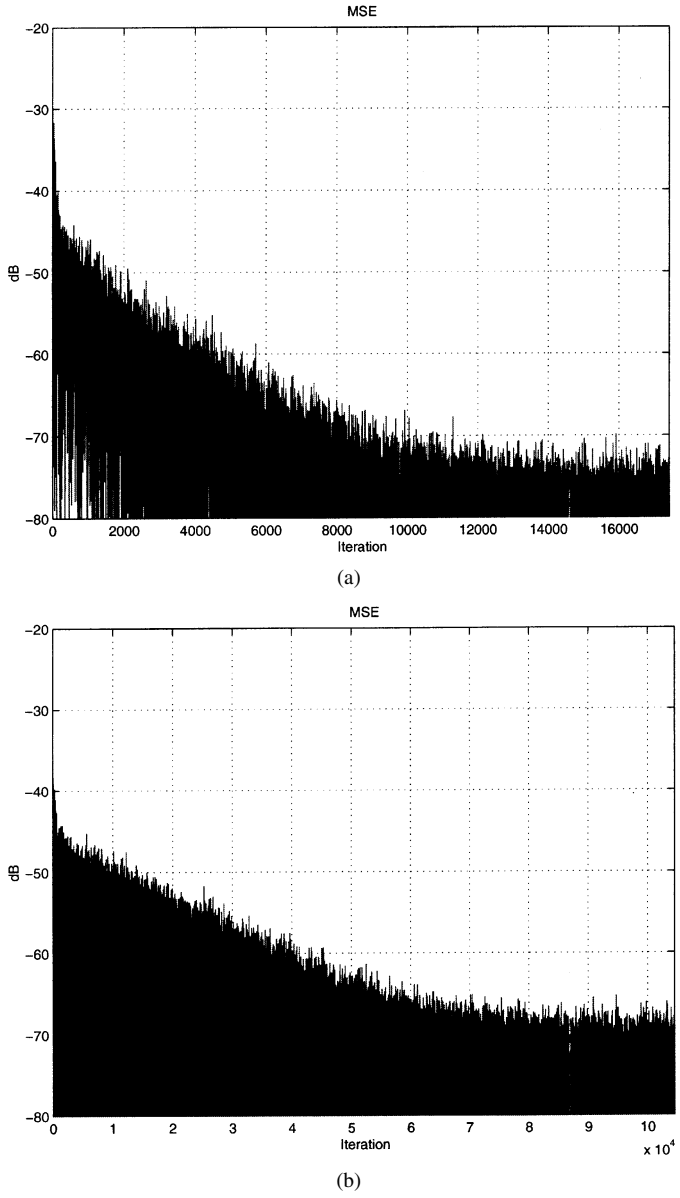

Fig. 6. Learning curves for (a) capacitor mismatch and (b) finite op-amp gain errors.

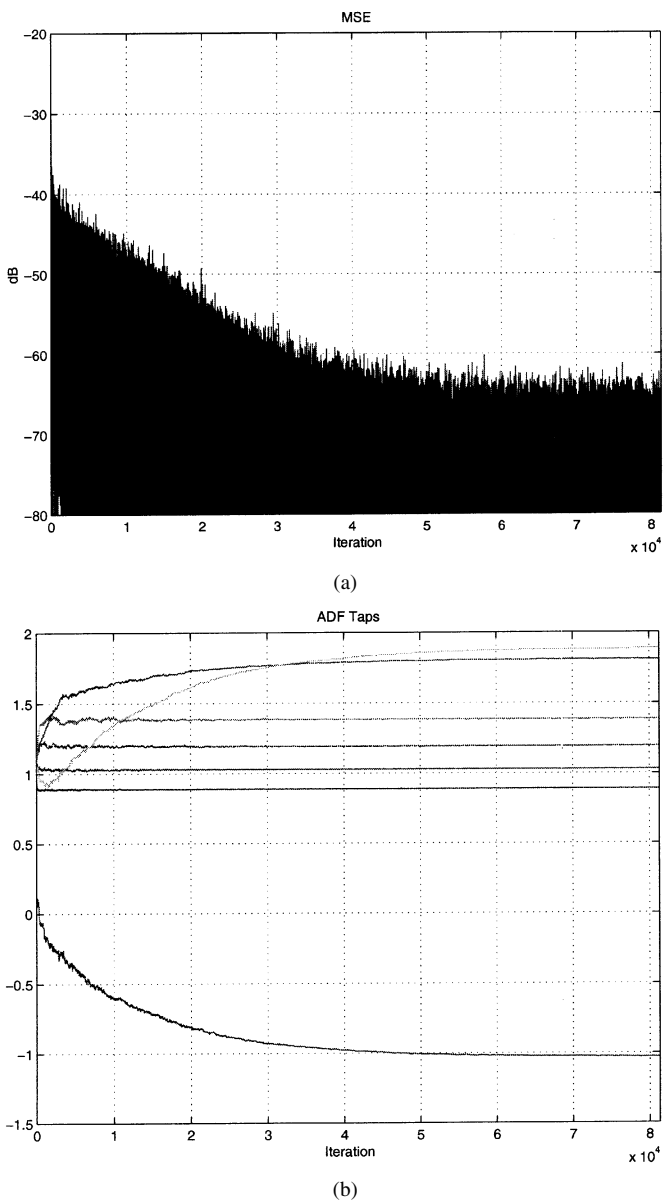

Fig. 7. Learning curves for (a) combinational errors and (b) LE tap values.

this filter to its time-domain counterpart used in communication receivers, the difference is significant: the distortion is not between successive samples, i.e., no intersymbol interference (ISI) is present. This follows from the fact that the "channel" is memoryless. It also differs from a memoryless Volterra series (i.e., a Taylor series) in that no nonlinear term is present [26]. This code domain is unique to pipelined ADCs due to the built-in redundancy of the decision levels. Instead of giving a thorough treatment of performance analysis, we summarize a few observations as following:

A. Steady-State MSE

When op-amp nonlinearity is excluded, the filtering formulation derived in (8) is exact. This indicates that memoryless linear errors can be fully removed when quantization noise is negligible (noise enhancement will be covered in the next part). This argument is justified by computer simulations: steady-state MSE close to 12 b, which is the word length of the raw code, is constantly achieved in spite of the presence of various other errors in the ADC. The MSE is also a function of the step size μ; a gear-shifting algorithm can be used to further reduce the MSE in the steady state.

B. Noise Enhancement

It is widely known in communication theory that LE suffers from a noise enhancement problem when the power spectrum of the input signal is not flat [27]. It is hard to quantify the noise enhancement effect of the proposed calibration algorithm as the concept "frequency" in code domain is not well understood. However, we point out the following case where quantization noise is enhanced due to equalization: if many output codes are missing, i.e., all $\alpha(k)$'s in (8) are substantially larger than 1/2, the second term in (8) which is normally the quantization noise

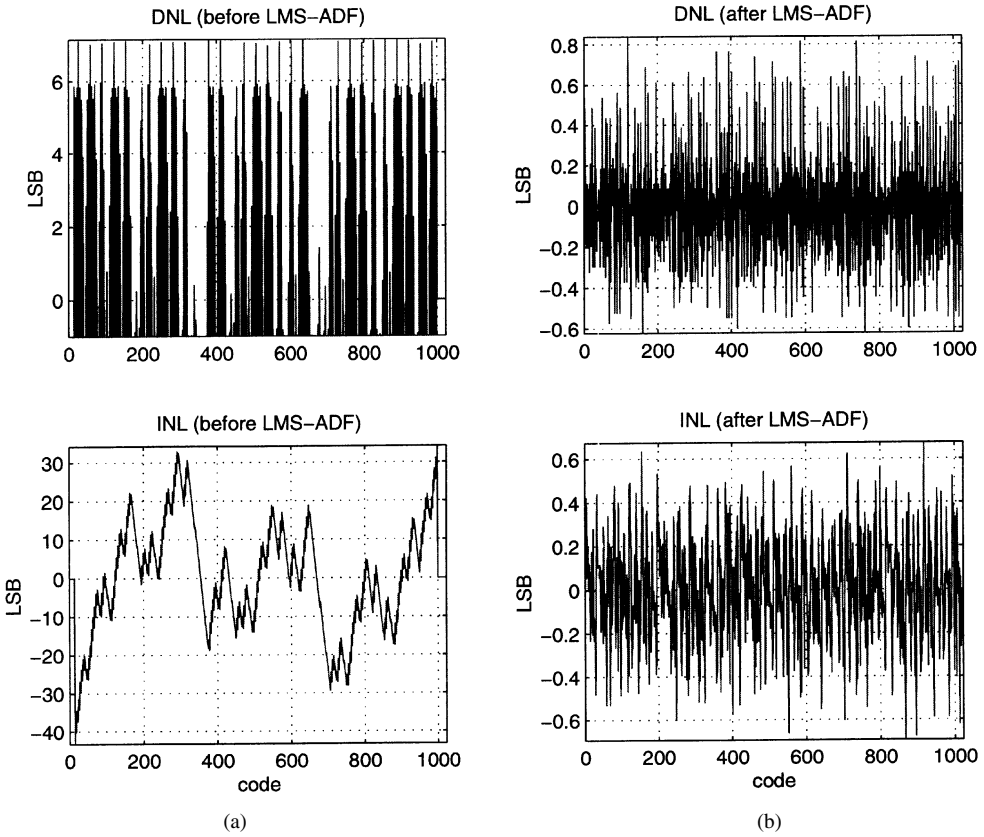

Fig. 8. DNL and INL (a) before and (b) after LMS calibration.

will be greatly magnified. This happens when capacitor mismatch or finite op-amp gain effect is severe. A code density test (CDT) reveals nulls in the statistics (DNL in Fig. 8) of the output code. This may serve as an intuition for the nonflatness of the "spectrum." The remedy to this problem is to increase the word length of the raw code, i.e., to add more stages. This occurs with low overhead of power consumption since an optimum pipeline design often employs stage scaling where power consumption is dominated by the front-end amplifiers.

C. Singularity

The filtering problem can be approached using a least-squares formulation [27] as well. As before, define a code domain vector $D(n) = [\,D_1(n) \quad D_2(n) \quad \dots \quad D_N(n)\,]^T$ for ADC decisions on the nth sample. Augment $D(n)$ by a dc component $D_0(n)$, $D(n) = [\,D_0(n) \quad D_1(n) \quad \dots \quad D_N(n)\,]^T$. We want to solve the linear equations (9), shown at the bottom of the page, for F subject to least-squares criteria, where Y is a vector of $(N+1)$ input samples, F contains $(N+1)$ unknown tap values of the filter, and X is a matrix of $(N+1) \times (N+1)$ decision codes of the ADC made across time (rows) and stages (columns).

Note that we have formulated X as a square matrix for illustration purpose. In general, it can be rectangular, and numerical techniques such as singular value decomposition (SVD) can be applied to the problem. In case when X is nonsingular, the solution to (9) is trivial, shown here as

$$F = X^{-1}Y. \tag{10}$$

In theory, this means that a set of $(N+1)$ noiseless observations of D_{in} and $\underline{D}$ should yield enough information to determine $(N+1)$ unknown tap values. This statement has a profound implication: it means that the input signal V_{in} does not have to exercise the whole input range to make the digital correction work; a limited set of $(N+1)$ noiseless samples is enough. But singularity can occur if V_{in} is confined to a small region which is a subset of $[-V_{\text{ref}}, V_{\text{ref}}]$, where $D_1(n)$ does not toggle for all $(N+1)$ samples as an example. This means the second column of X is constant, making it linearly dependent on the

$$\begin{bmatrix} D_{\text{in}}(n) \\ D_{\text{in}}(n+1) \\ \dots \\ D_{\text{in}}(n+N) \end{bmatrix} \approx \begin{bmatrix} D_0(n) & D_1(n) & \dots & D_N(n) \\ D_0(n+1) & D_1(n+1) & \dots & D_N(n+1) \\ \dots & \dots & \dots & \dots \\ D_0(n+N) & D_1(n+N) & \dots & D_N(n+N) \end{bmatrix} \begin{pmatrix} f_0 \\ f_1 \\ \dots \\ f_N \end{pmatrix}$$

or

$$Y \approx XF \tag{9}$$

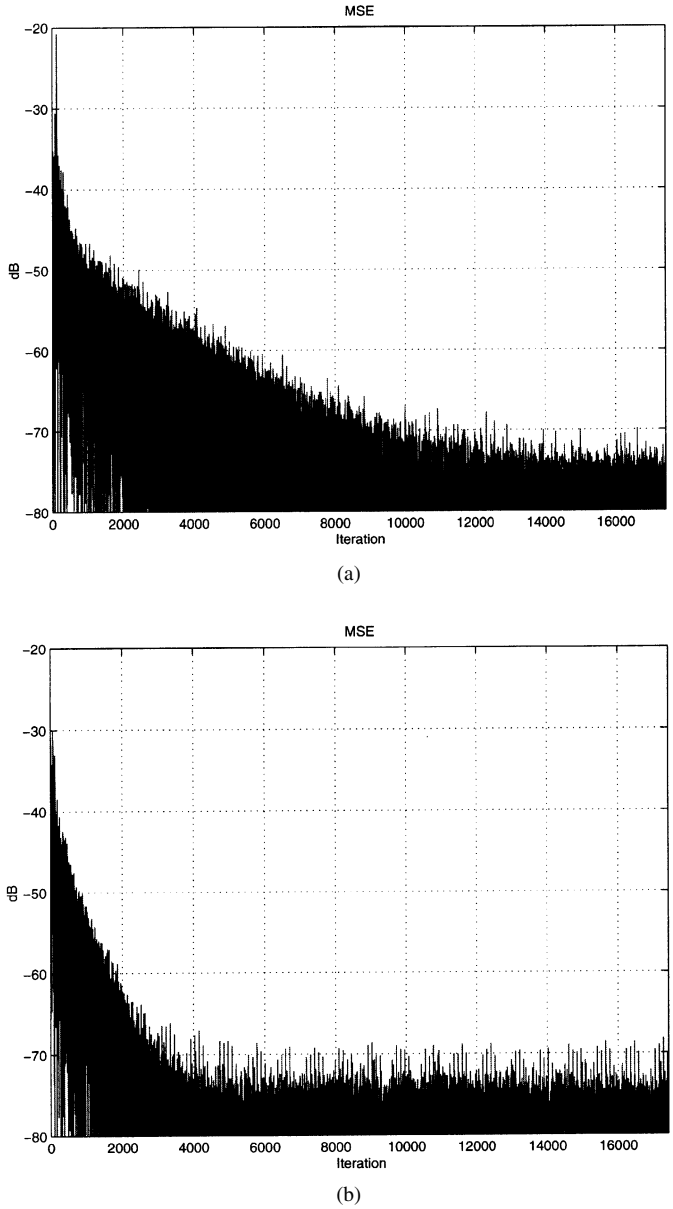

Fig. 9. Learning curves with (a) saw-tooth and (b) sine input signals.

first column that is also a constant (the dc tap). Thus, rank (X) is at most N, i.e., the matrix is singular.

Fortunately, when X is singular, a solution to (9) still exists, but it is not unique. Adaptive filtering theory says that an LMS or a recursive-least-squares (RLS) algorithm will still work [27]. The difference is that the error surface $|\varepsilon(f_0, f_1, \ldots, f_N)|^2$ as a function of the filter tap values will not be a nice bowl shape with a global minimum, but instead will be a valley where $|\varepsilon|^2$ is minimum everywhere inside; instead of converging, f_0 and f_1 wander around subject to a linear constraint. As (8) says the global optimum filter is unique, this indicates that a subset of the solution (f_2 to f_N) has been found and this solution is still optimal inside the limited region of observation. As V_{in} excursion reaches outside of this region, the degeneration is lifted and more tap values can be determined. On the other hand, when more degeneration occurs, i.e., the second stage of the ADC also outputs a constant, f_2 will also fail to converge, and an even smaller subset of the solution yields. The above phenomena have been observed through simulation.

Another way of interpreting this is that ADF adaptation follows the input signal: it will adapt to the right local solution wherever the input signal resides. This occurs when the system of (9) becomes underdetermined. The local solution will converge to the unique global optimum when enough information is obtained from samples and X goes out of singularity. In other words, this indicates that calibration will yield better performance where the ADC is more frequently used.

V. Volterra Filtering

In general, the op-amp transfer function is nonlinear due to the use of active devices. The linear (Wiener) filtering approach introduced in Section II cannot remove this error, therefore a Volterra filter must be used instead [23]–[26]. Fig. 3 shows the general form for error compensation that makes use of a nonlinear filter $f(\underline{D})$. The complexity of a Volterra filter, however, increases geometrically in terms of its order. For example, if the linear filter used in Section II has N taps, the corresponding Volterra filter of order three will have $3N + (3/2)N(N-1) + (1/6)N(N-1)(N-2)$ taps. On the other hand, if a "bootstrapping" calibration algorithm is adopted, then the filter complexity for each stage will only be linearly proportional to its order. But we have argued that this only yields a suboptimal calibration due to the tampering of analog signal path. Alternatively, a frequency-domain LMS algorithm [27] may be used to reduce the tap numbers.

VI. Conclusion and Future Research

We have presented a new background calibration algorithm for pipelined ADCs. This algorithm is all-digital, adaptive, and data-driven. Relaxing the stringent requirement on the precision of analog components potentially leads to very high conversion speed. The derivation of this algorithm greatly resembles the adaptive equalization concept widely used in digital communications. A linear equalizer is formulated to correct linear errors of pipelined ADCs; these errors include capacitor mismatch, finite op-amp gain, and various input-referred offsets. The proposed calibration algorithm is verified through computer simulations. A short analysis of steady-state MSE, noise enhancement, and some convergence issues of the ADF is also discussed.

The work presented here opens up several potential future research topics. On the theory side, a thorough treatment and rigorous formulation of the filtering problem in code domain will be useful. An extension of this approach to nonlinear (Volterra) filtering is important to treat nonlinearities. On the implementation side, an efficient realization of a Volterra filter compatible with VLSI technology and applicable to this subject has yet to be developed. Digital complexity of these filters is the key problem. But as CMOS device scaling continues and on-chip DSP capacity increases, more sophisticated digital

algorithms are expected to be implementable in the future. Therefore, the new approach will eventually prove to benefit from it.

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