

Design and Optimization of Sense-Amplifier-Based Flip-Flops

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Abstract

An improved design of a sense-amplifier-based flip-flop is presented. The new design overcomes the problems of floating nodes, which is a weakness of previously reported solutions. This is achieved by systematic derivation of flip-flop equations and rearranging the resulting network. The resulting flip-flop outperforms earlier published structures, exhibiting T_{CQ} of 190ps when driving 100fF load in a 0.18 μ m CMOS technology.

1. Introduction

Sense-Amplifier-based Flip-Flops (SAFF) have been used in high-performance and low-power digital systems. Recently reported modifications of SAFFs exhibit very small delay, calculated as a sum of setup time and clock to output delay in high-speed datapath applications. These flip-flops have differential outputs, and single or differential inputs can be used accordingly. SAFF present a small clock load, since only three transistors are connected to the clock signal [1,2,3]. The initial design of a SAFF was based on the sense amplifier in the first and the NAND-based cross-coupled SR latch in the second stage, Figure 1 [1]. Modified SAFF improves the output stage to reduce the overall delay [3].

2. Analysis of operation

The sense amplifier stage [1] is precharged during the interval when clock signal is low. The high state of \bar{S} and \bar{R} keeps M_{N3} and M_{N4} on, charging their sources up to $V_{DD} - V_{IN}$ because there is no path to ground due to the off state of the clocked transistor M_{N6} . Since either M_{N1} or M_{N2} is on, the common node of M_{N1} , M_{N2} , and M_{N6} is also precharged to $V_{DD} - V_{IN}$. Therefore, prior to the leading clock edge, all the capacitances in the differential tree are precharged. Rising edge of the clock generates falling transition on only one of sense amplifier outputs, \bar{S} or \bar{R} . This negative pulse is being

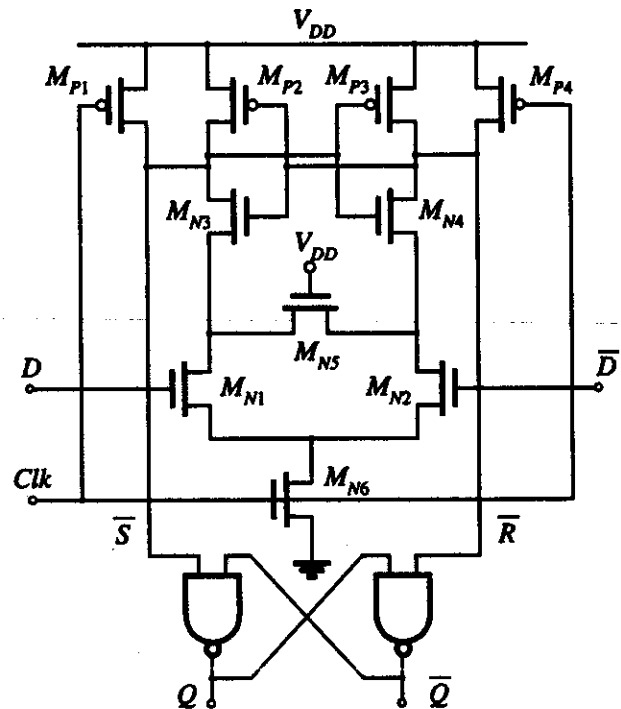


Figure 1. Sense amplifier-based flip-flop

captured by the SR latch and held until the end of the cycle.

As reported in [1], SAFF did not include the transistor M_{N5} . The additional transistor M_{N5} allows static operation, providing a path to ground even after the data is changed. This prevents the potential charging of the low output of the sense-amplifier stage, due to the leakage currents.

Outputs of the first stage are incompletely defined logic functions, with NMOS pull-down trees implementing $\bar{S} = Clk \cdot \bar{R}' \cdot D$, $\bar{R} = Clk \cdot \bar{S}' \cdot \bar{D}$ functions and PMOS pull-up trees implementing $\bar{S} = Clk \cdot \bar{R}'$, $\bar{R} = Clk \cdot \bar{S}'$, represented by Karnaugh maps shown in Figure 2.a and Figure 2.b. \bar{S}' and \bar{R}' represent previous values of signals \bar{S} and \bar{R} .

Values marked as "don't cares" (x) in Figure 2, actually represent floating outputs of the logic function, that are neither forced to 0 nor to V_{DD} . Essentially, the

truth table includes four more don't cares, since both \bar{S} and \bar{R} can not be zero at the same time. When clock is low, both \bar{S} and \bar{R} are precharged to high logic level. During the clock transition from low to high signals \bar{S} and \bar{R} evaluate new logic values.

Ideally, when Clk is changing from 0 to 1, and $D = 0$, the value of the \bar{S} node should remain unchanged, as well as the value of the node \bar{R} when Clk is rising and $D = 1$, to obtain proper flip-flop operation. The consequences of having don't cares in the Karnaugh map are explained in the case of \bar{R} :

(a) $Clk = 1, D = 1, \bar{R}' = 1$: This Karnaugh map entry is exercised when Clk changes from low to high logic level, causing the triggering of the flip-flop. With D being high, branch evaluating \bar{S} is being pulled to low logic level. Signal \bar{R} initially floats, causing a glitch, as illustrated in Figure 5, and slowing down the transition. Elimination of this situation would involve addition of another parallel pull-up PMOS branch, leading to diminishing returns in terms of speed. Because of this 'don't care' the new value of \bar{R} is not forced directly by the branch evaluating it, but indirectly through transistor M_{P3} and the change of \bar{S} .

(b) $Clk = 1, D = 0, \bar{R}' = 0$: This value corresponds to the case of the sense amplifier output \bar{R} being forced low at the leading edge of the clock. If the data changes after the leading edge of the clock, leakage currents could charge this node, and eventually change the state of the flip-flop.

This problem was noticed in [2], and proposed modification is shown in Figure 1. Additional transistor, M_{N5} , in Figure 1, allows static operation, providing a path to ground even after the data changes. This prevents eventual charging of the low sense-amplifier output, due to leakage currents, to the value when it could trigger the latch. This solution has two major disadvantages:

- the glitch on \bar{S} is more emphasized due to the conducting path through M_{N5} , Figure 5;
- direct gate connection to long metal lines (V_{DD} or ground) is prohibited. This is due to very small gate thickness in deep-submicron technologies.

3. Flip-flop optimization

This problem of floating nodes can be solved in a more consistent way, by covering the Karnaugh maps as shown in Figure 2:

$$\bar{S} = Clk \cdot \bar{R}' \cdot \bar{D} \cdot \bar{S}', \quad \bar{R} = Clk \cdot \bar{S}' \cdot D \cdot \bar{R}'.$$

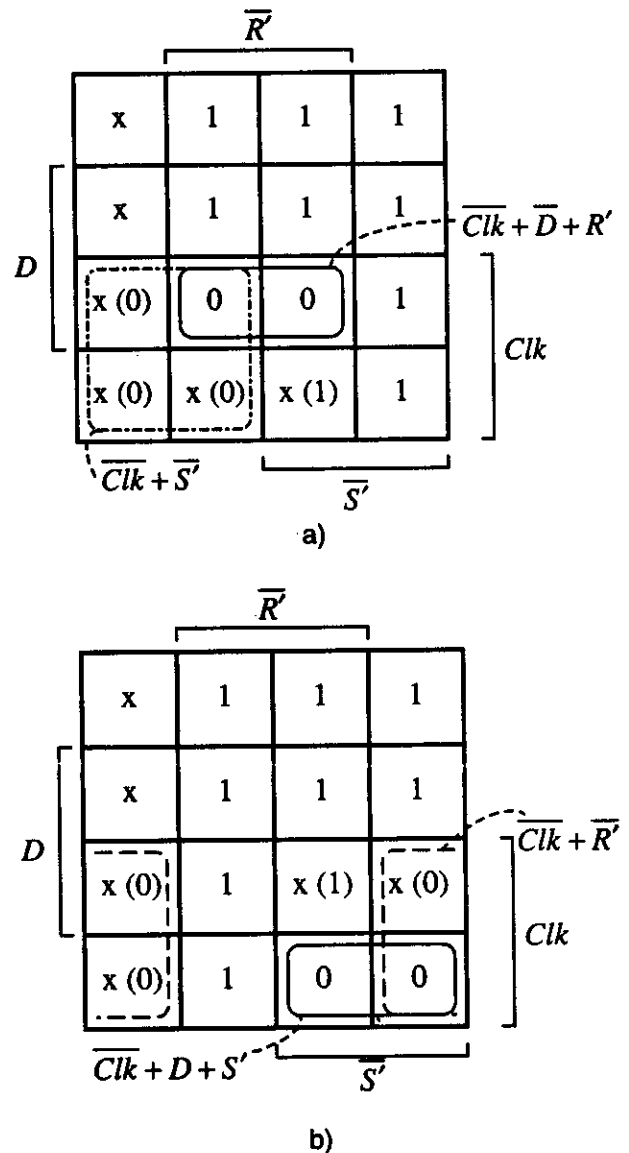


Figure 2. Karnaugh maps for a) \bar{S} , b) \bar{R}

This modification involves addition of one NMOS transistor per each pull-down tree. Since the implementation of the SAFF as shown in [3], already includes the signals S and R , the gates of added transistors M_{N5} and M_{N6} are connected to existing inverter outputs, so their addition does not change the input loading, and reduces the glitch magnitude. Additional inverters I_3 and I_4 are used to decouple the loading of critical nodes \bar{S} and \bar{R} by transistor M_{N3} and M_{N4} gates [4], speeding up the flip-flop operation.

The second stage of the flip-flop is a SR latch as presented in [3]. This output stage produces equal delays of rising and falling transitions at both true and complementary outputs. It has equal delays of simultaneous transitions at both true and complementary outputs regardless of the load on the other output.

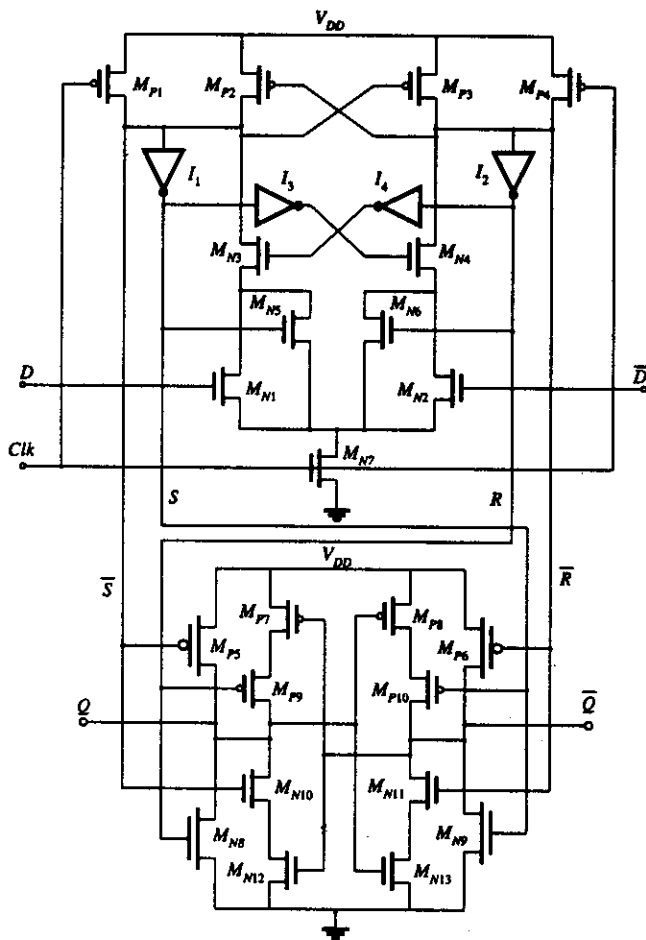


Figure 3: Modified sense amplifier-based flip-flop

4. Results

In addition to reliability improvement, proposed modification of the SAFF shows 5-10% faster operation over the design with cross transistor [2], as shown in Figure 6. This flip-flop was designed in 0.18 μm L_{eff} CMOS, with improved output stage [3], optimized to drive the loads between 100 and 150fF [5]. Clock to output delay is 190ps when driving 100fF load at both outputs. It is possible to design the falling edge-triggered SAFF with the same driving capability, Figure 4. This flip-flop has the same setup time of -20ps and its delay characteristic is equidistant to the characteristic of the rising edge SAFF, with clock to output delay of 240ps when driving 100fF load. This is not the case with originally proposed design, based on cross-coupled NOR gates [1]. The results from Figure 6 are obtained with the same sizes of the transistors in the input and output stage [3]. Two lines for SAFFs from [1] in Fig. 6, represent the cases when *i*) only one or *ii*) both outputs are loaded. Improved output stage design [3] has equal delays for both outputs, that is independent of the load on the other output.

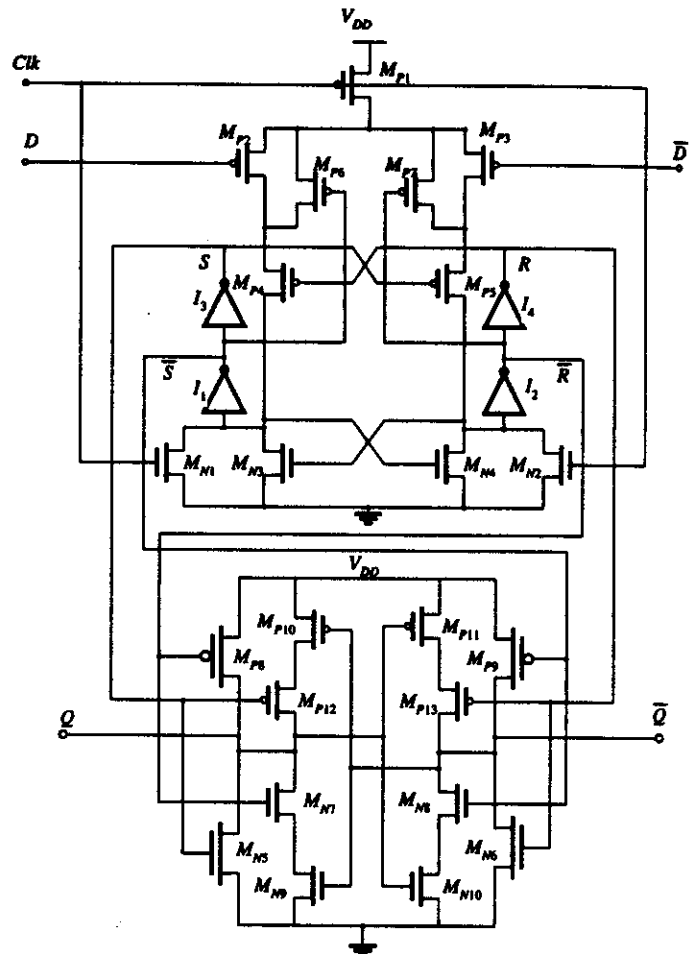


Figure 4: Falling edge-triggered flip-flop

5. Conclusion

A new design of sense-amplifier-based flip-flop is presented that eliminates floating nodes in the sense amplifier stage. By using decoupling inverters this modification results in improved switching speed. The reliability of the circuits is improved as compared to previous solutions. In addition, the falling edge flip-flop was designed with equidistant delay vs. load line to the rising edge flip-flop. The resulting flip-flop outperforms earlier published structures, exhibiting clock to output delay of 190ps with -20ps setup time when driving 100fF load in a 0.18 μm CMOS technology.

References

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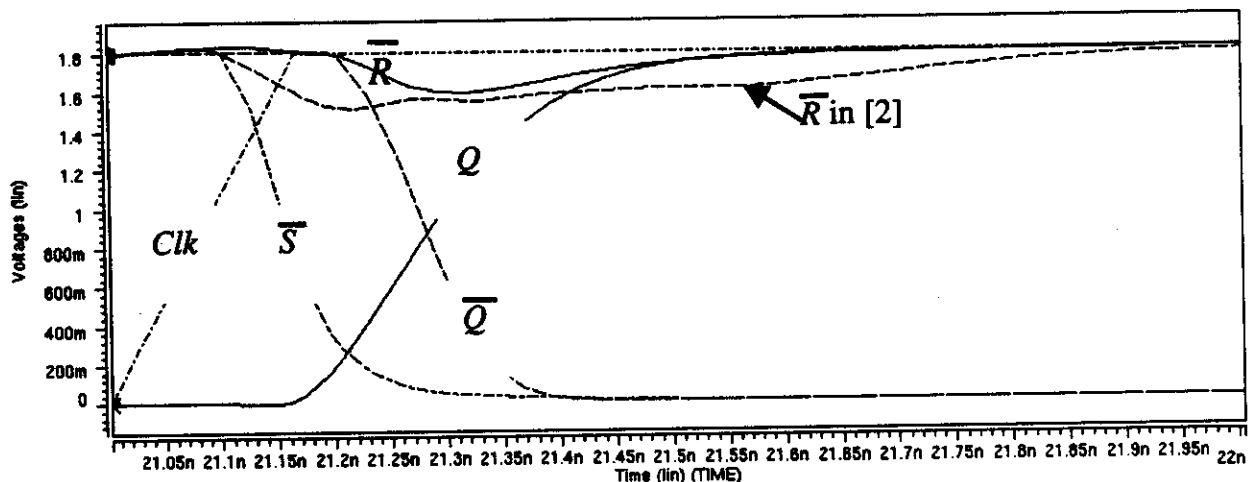


Figure 5: Typical SAFF waveforms

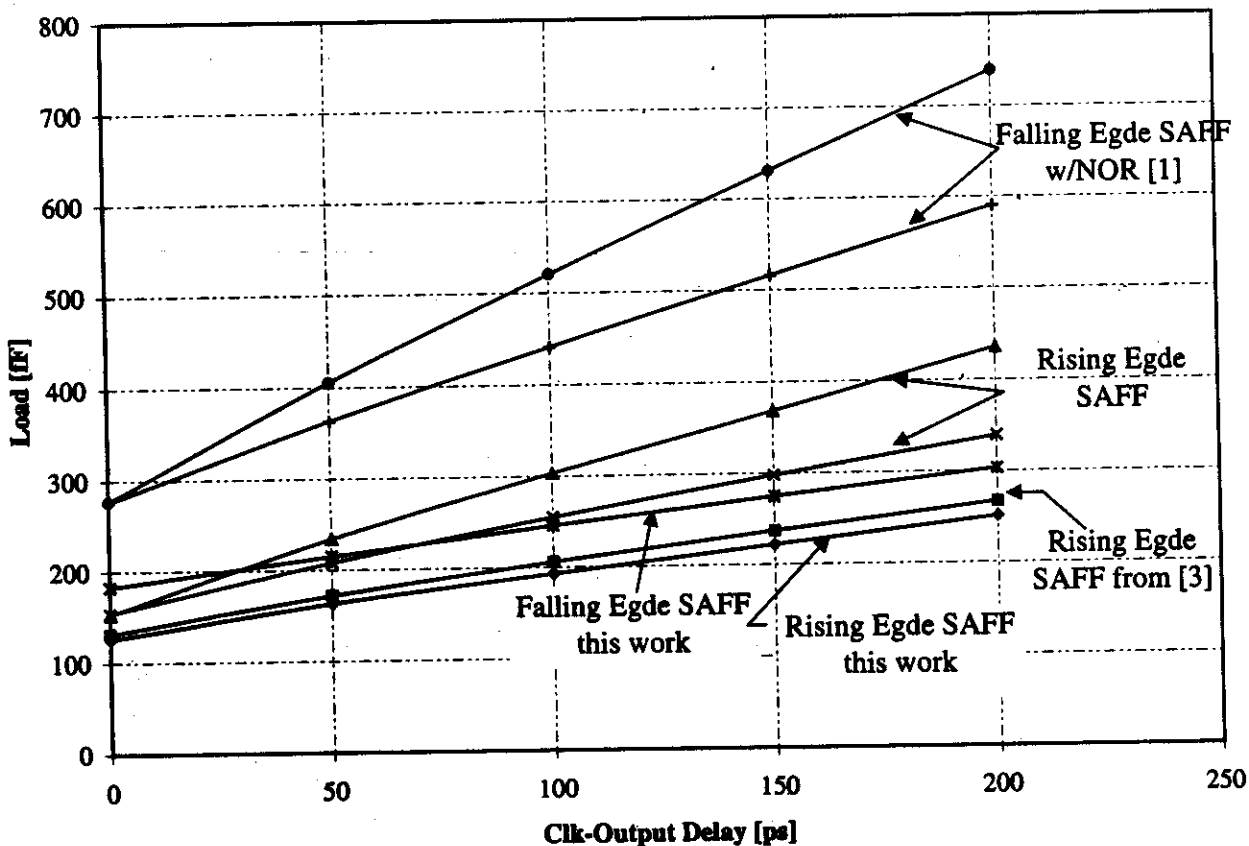


Figure 6: Delay vs. load for different SAFFs