Analysis and Design of Integrated Active Cancellation Transceiver for Frequency Division Duplex Systems

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***Abstract*— An active transmitter (TX) cancellation scheme enabling integration of the antenna interface for frequency division duplex systems is presented. A replica of the TX current is synthesized in shunt with the receiver (RX) by a digital-to-analog converter (DAC). The replica DAC virtually shorts out the TX signal at the RX input while having minimal impact on the TX insertion loss. Propagation of the TX phase noise in the RX band is analyzed and shown to be feed-forward cancelled in the proposed system. A prototype chip including integrated TX, measurement RX, and cancellation circuits, operating on a single-shared antenna, is implemented in 65-nm CMOS. The cancellation replica demonstrates > 50 dB cancellation of a +12.6 dBm peak 20-MHz TX signal across a wide range of center frequencies and up to 5:1 voltage standing-wave ratio at the antenna interface. The RX is able to down-convert the RX signal at 40-MHz offset with < 4.3 dB noise figure degradation in the presence of the residual TX signal.**

***Index Terms*— Active cancellation, digital-to-analog converter (DAC), electronicsubtraction, frequency division duplex (FDD), integratedduplexer, phase noise cancellation, self-interferencecancellation, shared antenna interface, switched-capacitorpower amplifier (SCPA), wideband transceiver.**

I. Introduction

THE adoption of 3G and 4G communication technologies has led to a proliferation of wireless bands. The rapidly increasing complexity has led to the demand that a single multi-mode radio transceiver IC supports the varying requirements. Techniques such as digital power amplifier (PA) architectures on the transmitter (TX) side and current-mode inductor-less architectures on the receiver (RX) side have enabled transceiver chains operating over the majority of low-frequency wireless bands [1]–[5]. It is thus not the TX or RX which provides the main limitation for radio reconfigurability, but rather the discrete off-chip components and filters used to provide interference rejection at the antenna interface [6].

In particular, the largest interferer the RX experiences is often a TX signal from within the same system. For example, the long-term evolution (LTE) standard has led to the adoption of 35 frequency division duplex (FDD) bands, in which the TX and RX operate simultaneously in separate frequency bands over the same antenna. The large dynamic range between the TX and RX, for example, +23 dBm TX power and −100 dBm RX sensitivity, must be filtered within a sharp stop band, as low as twice the signal bandwidth. This necessitates off-chip duplexers, which are high-Q, and therefore difficult to tune.

Prior work has attempted to integrate the off-chip duplexers on the transceiver chip. The passive hybrid technique [7]–[10] constructs networks which force the TX signal to appear as a common mode perturbation across the RX port. A fundamental TX insertion loss (IL) versus RX noise figure (NF) tradeoff is inherent to the structure, due to its passive reciprocity [11]. In particular, the roughly 3-dB TX IL causes 50% of the TX power to be lost, prohibitively degrading TX efficiency. The network is difficult to balance across the operating range of antenna impedances in [10]; a 10-bit *RC* digital-to-analog converter (DAC) covers a limited voltage standing-wave ratio (VSWR) of 1.5:1.

Analog subtraction has recently gained interest in the wireless systems community as a technique for cancelling TX self-interference. In this method, a portion of the transmit signal is tapped or synthesized through a replica chain, and injected into the RX to perform feed-forward cancellation of the TX leakage [12], [13]. The difficulty in adapting this technique to a wireless transceiver stems from matching the frequency selective response of the TX to RX leakage network across a wide bandwidth, while maintaining high RX sensitivity. A series of integrated electronic subtraction works has been reported in [14]–[19], however, it remains difficult to isolate $> +10$ dBm TX output power over a 20-MHz modulation bandwidth at 40-MHz duplex spacing with low impact to RX NF. In particular, only Yang *et al*. [17] and Zhou *et al*. [19] fully integrate the antenna interface on-chip. However, Yang *et al*. [17] provide only 25-dB TX to RX isolation, and significant NF penalty even at low (< 0 dBm) TX power. In [19], operation is limited to < 0 dBm TX power at the antenna, although it operates in full duplex, with no TX–RX band separation. Off-chip couplers are used on the TX signal path to feed a cancellation network in [14]–[16] and [18]. These representative works require additional external isolation at the antenna interface to achieve $> +4$ dBm operation, although [16] operates in

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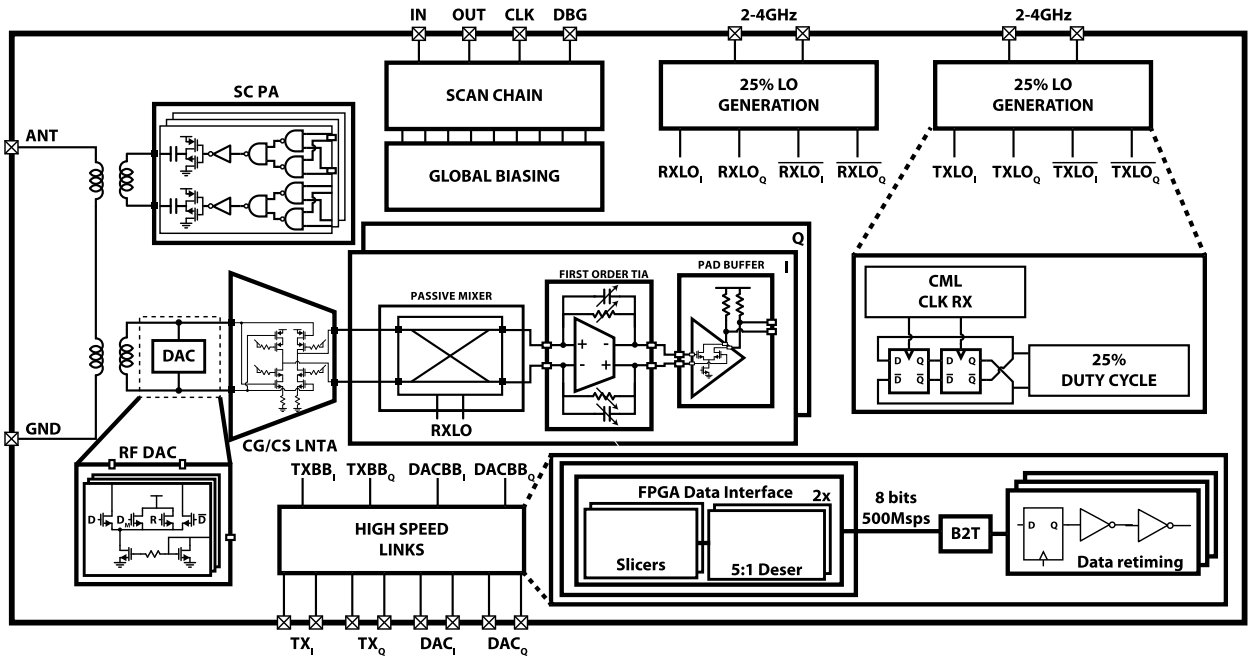


Fig. 1. Top level proposed system schematic.

full duplex. Additionally, Zhou *et al*. [14] provide isolation over a narrow TX modulation bandwidth. Finally, only van den Broek *et al*. [16] and Yang *et al*. [17] integrate the TX on-chip, which is necessary to accurately capture all TX/RX leakage mechanisms and TX distortion terms at the RX input.

This paper describes an electronic subtraction transceiver with a fully integrated antenna interface, expanding the conference publication [20] with added analysis of the system's fundamental performance bounds and design details. The chip advances the state of the art in several performance metrics, including TX/RX isolation, and TX/RX bandwidth and spacing. In particular, a DAC cancellation replica source, with its input data digitally adapted, is used to provide high TX/RX isolation across a 20-MHz modulation bandwidth, over a tunable range of center frequencies. The chip achieves 50 dB of TX signal cancellation at the RX input, while minimizing non-deterministic thermal and phase noise sources that fall in the RX band. This cancellation enables linear RX operation simultaneously with the TX, such that the residual TX signal and its nonlinear terms due to deterministic quantization error can be subtracted from the RX output in the digital domain.

II. System Concept

The proposed FDD transceiver is shown in Fig. 1. The TX and RX are connected in series with the antenna through series stacked impedance matching transformers. The operation of this structure is illustrated in the simple model shown in Fig. 2. A cancellation current DAC placed in shunt with the RX acts as a controlled current source, reproducing the TX current induced on the RX side of the transformer. As the TX current in the RX secondary is shunted by the cancellation DAC, only the residual difference in current, set by the resolution of the cancellation DAC, flows into the RX load impedance. This is the only portion of the current that can generate a voltage swing across the RX port, and accordingly the residual TX power at the RX input in dBm is simply

$$P_{\text{Residual}} = (P_{\text{TX,MAX}} - 6N_{\text{BITS,DAC}}). \tag{1}$$

Note that as long as the DAC full-scale current is sized to cancel the $P_{\text{TX,MAX}}$ current, the scheme produces a constant residual interference at the RX input set by the resolution of the cancellation current, with no dependence on instantaneous TX power level. This differs from a standard duplexer, which provides a fixed rejection, rather than fixed residual power.

As little voltage swing is generated by the TX across the RX, the receive port appears as a virtual ground to the TX signal. For any other signal, the cancellation current DAC does not create the virtual ground condition. This virtual ground condition has two implications. First, the RX port is shielded from the TX voltage swing. The cancellation DAC also experiences only this small residual voltage swing and can maintain linear performance. Second, the virtual ground shields the TX from the RX's load impedance. Due to the shunt cancellation, the TX cannot induce a voltage change across the receive port, regardless of its output current or the RX load impedance. Accordingly, the TX appears to be connected directly between the antenna and ground, and the duplexing network has minimal impact on TX efficiency.

On the receive side, the TX's impedance appears in series with the antenna connection, and the DAC's impedance appears in shunt. A TX with low series output impedance in the RX band must be designed—a large impedance would form a voltage divider, resulting in RX side IL. Additionally, it is desirable for this TX impedance to be TX amplitude-independent, to avoid a time-varying voltage division. In general, the voltage at the RX input port due to a TX amplitude dependent $R_{\text{TX}}(A_{\text{TX}})$ term can be simply expressed as

$$V_{\text{Input}} = \frac{V_{\text{RX}} R_{\text{LNA}}}{R_{\text{LNA}} + R_{\text{ANT}} + R_{\text{TX}}(A_{\text{TX}})}. \tag{2}$$

For this paper, a switched-capacitor PA (SCPA) is chosen as a TX due to its low amplitude-independent impedance.

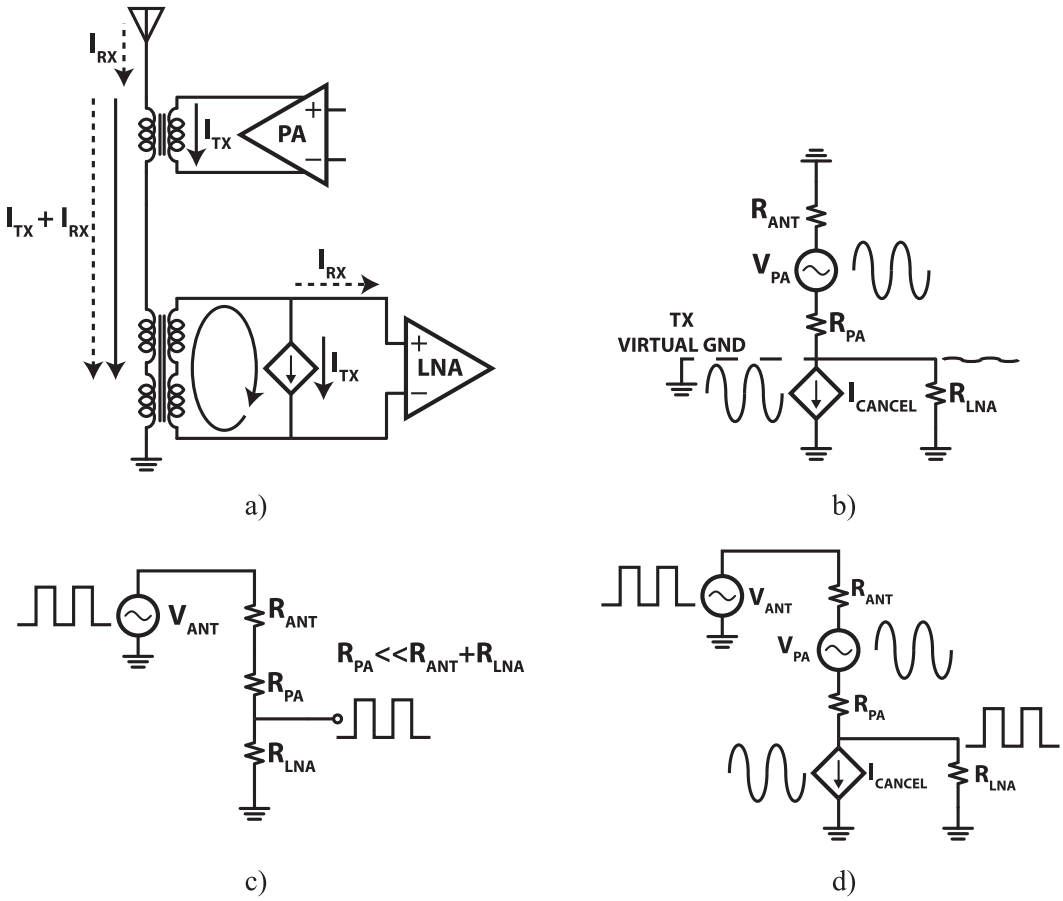


Fig. 2. (a) Proposed antenna interface. (b) TX operation. (c) RX operation. (d) Combined operation.

To minimize shunt loss, the current DAC output impedance should be significantly higher than the RX input impedance in the RX band.

This architecture is scalable to cancellation of high TX powers and cancellation for wide modulation bandwidth TX signals. The replica current is fed directly into the low-impedance TX virtual ground node—accordingly, aside from the antenna side of the transformer, which contains no active devices, no node experiences a large voltage swing. The cancellation signal from the DAC is a current, which can be synthesized in CMOS technology with high linearity. The difficulty in providing cancellation across a wide modulation bandwidth stems from the difficulty in matching the frequency dependence of the TX/RX coupling path [15]. The use of a cancellation DAC enables digital adaptation and predistortion of the input data to the DAC to match the frequency dependence. Additionally, this digital adaptation scheme can replicate nonlinearity from the TX or DAC, as well as slow time-varying effects from temperature and antenna VSWR drift. In this paper, an off-chip nonlinear digital filter is used to capture leakage network effects.

A. Power Consumption of the Cancellation DAC

In order to realize the floating current source of Fig. 2, this work builds a differential DAC with dc common mode current drawn from the transformer center tap. Lowering this center tap supply voltage allows cancellation to occur with significantly lowered power consumption as compared with the TX power. In practice, some voltage headroom must be maintained across the current source transistor, resulting in a power/noise tradeoff—reducing the supply headroom requirement, i.e., transistor overdrive, at a fixed current increases the current source noise, desensitizing the RX. This tradeoff is described in detail in Section II-D.

To compute the power penalty of the cancellation, the DAC can be modeled as a current source fed through a hard-switched mixer, as described in Section III-B and pictured in Fig. 3(a). The required DAC dc current to cancel the maximum TX current at the fundamental frequency I_{TX} can be expressed in terms of the RX balun turns ratio as

$$I_{\mathrm{DAC}} = I_{\mathrm{TX}} \frac{\pi}{2N_{\mathrm{turns}}}. \tag{3}$$

The TX dc power consumption is the TX current scaled by the TX efficiency

$$P_{\mathrm{TX,dc}} = \frac{1}{2} \mathrm{I}_{\mathrm{TX}}^2 R_{\mathrm{ANT}} \frac{1}{\eta_{\mathrm{TX}}}. \tag{4}$$

Accordingly, the power consumption of the TX normalized by that of the DAC is

$$\eta_{\mathrm{Cancellation}} = \frac{N_{\mathrm{turns}} \sqrt{2P_{\mathrm{TX,dc}}} \sqrt{R}_{\mathrm{ANT}}}{\pi \sqrt{\eta}_{\mathrm{TX}} V_{\mathrm{DD,DAC}}}. \tag{5}$$

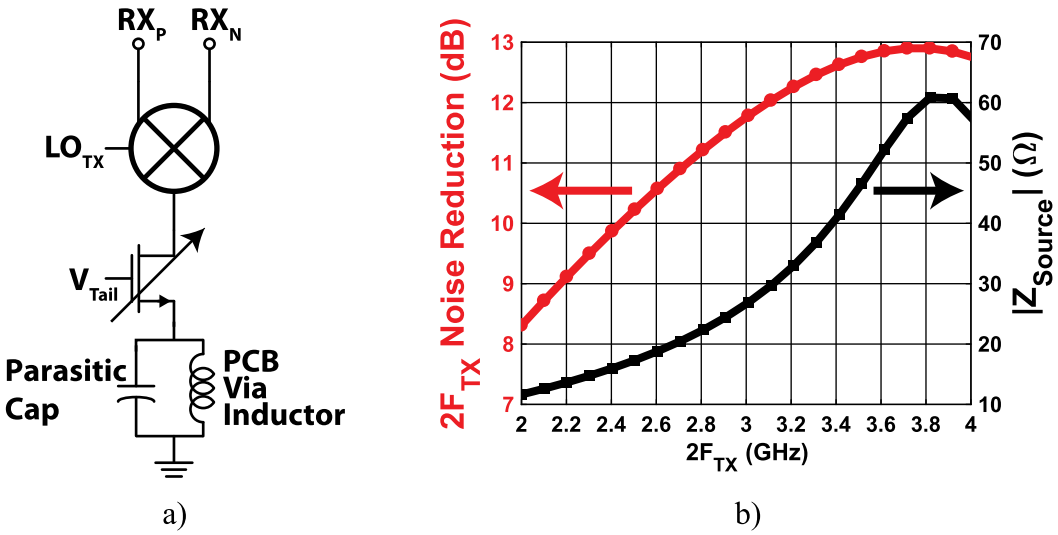


Fig. 3. (a) Conceptual picture of cancellation DAC. (b) EM simulation of degeneration impedance.

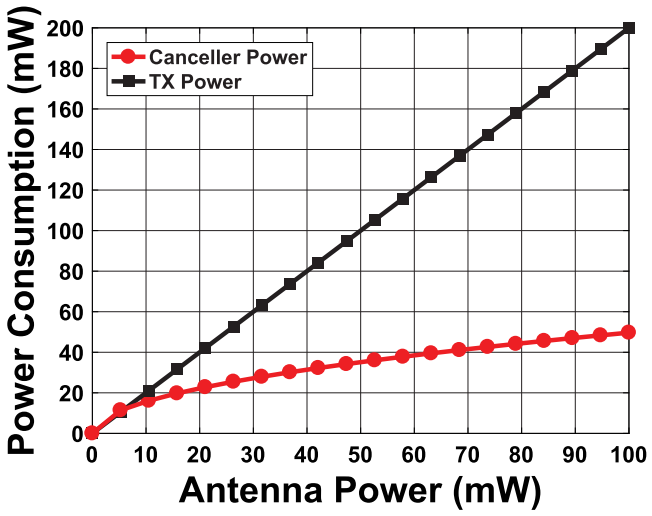


Fig. 4. Cancellation power versus TX power at the antenna.

The transformer turns ratio and the DAC supply voltage are the only free design parameters; TX power and antenna impedance are fixed by the system. The TX power from the supply and replica power consumption are plotted against the TX power at the antenna in Fig. 4, under the specific assumptions of a 1:2 turns ratio, 1-V center tap supply, and 50% TX drain efficiency. The key point is that the voltage swing across the DAC is not fundamentally coupled to the TX output voltage, but rather the residual voltage swing after cancellation. This allows the DAC's power consumption to be substantially reduced with respect to the TX.

B. TX Phase Noise

Phase noise in the TX local oscillator (LO) at the duplex offset from the carrier appears in the RX band as it upconverts the TX data. This noise power increases dB for dB with TX power, heavily desensitizing the RX at high TX output powers. For example, a source LO with a phase noise density of -150 dBc/Hz at the duplex spacing, when mixed with a +20 dBm TX signal, results in a -130 dBm/Hz noise density at the RX band, corresponding to a 44-dB NF.

Given that the TX and DAC can share a LO, the opportunity exists for cancellation of the TX LO source phase noise in the RX band [21]. Sharing the DAC and TX LO forces a high degree of correlation in their output phase noise, implying it can be feed-forward cancelled in the same manner as the signal, as shown in Fig. 5.

For a single-tone input, the TX modulates its LO and phase noise by a complex scaling factor $A_{\mathrm{TX}}e^{j\varphi_{\mathrm{TX}}}$, representing the TX baseband amplitude and phase. This TX signal leaks to the RX input through an analog network with a complex frequency-dependent transfer function, $f_{\mathrm{Leak}}(j\omega)$, which again scales the close-in phase noise by the same factor as the main tone. In order to cancel the main TX tone, the DAC scales its LO by $A_{\mathrm{TX}}|f_{\mathrm{Leak}}(j\omega_{\mathrm{TX}})|e^{j(\angle f_{\mathrm{Leak}}(j\omega_{\mathrm{TX}})+\phi_{TX})}$, causing the DAC to match the main tone in both amplitude and phase. If the DAC LO phase noise is identical to that of the TX LO, then TX phase noise experiencing the same amplitude scaling and phase shift as the main tone is also cancelled, as in Fig. 5. It is thus beneficial for the leakage network to have as wide of a bandwidth as possible, in order to maximize the bandwidth over which the phase noise and main tone are scaled by the same factor. Note that the cancelled TX phase noise sees a virtual short at the RX input. The relevant network is thus the TX–RX network with shorted RX port, and any filtering impedance at the RX input for rejecting blockers does not affect phase noise cancellation bandwidth.

For the architecture used in this paper, scaling and phase shifting for both the TX and the DAC are performed by I/Q weighting. Consider the case where the TX outputs 1 mA in the I direction, and $f_{\mathrm{Leak}}(j\omega_{\mathrm{TX}}) = j$. The TX outputs a scaled version of the I LO, and the leakage channel shifts the signal by +90°, producing 1 mA in the Q direction at the input of the RX. Because the DAC and TX share LOs, to cancel this tone, the DAC scales its Q LO to produce 1 mA. The TX phase noise at the RX input is thus the I LO's phase noise shifted

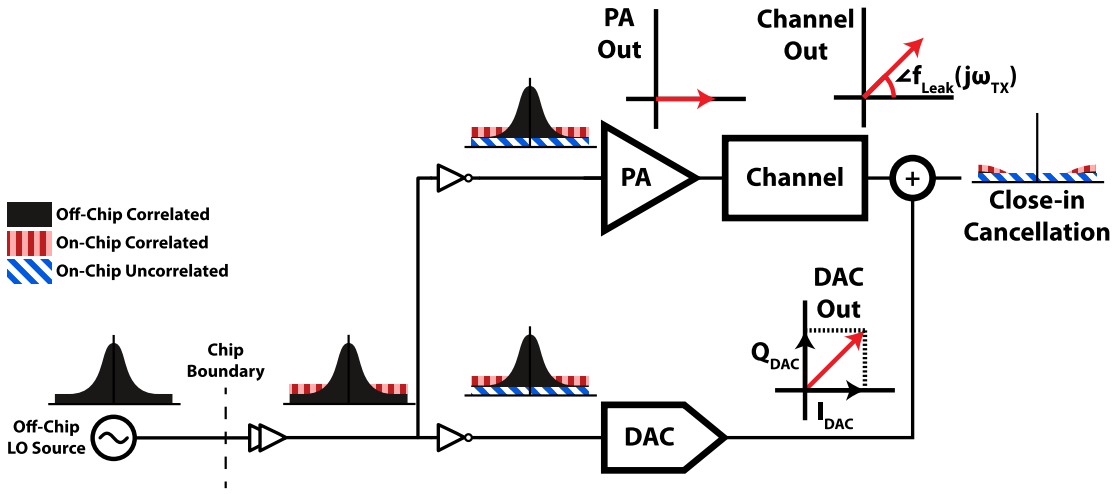


Fig. 5. Feed-forward cancellation path for source phase noise.

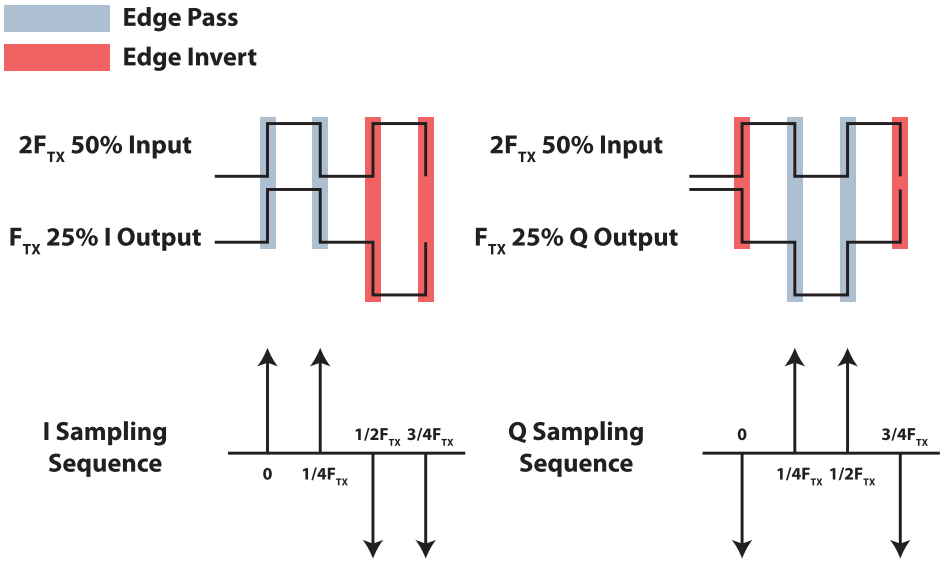


Fig. 6. Edge passes/inversions and associated sampling sequences for I and Q LO generation.

by +90°, while the DAC phase noise at the RX input is the Q LO's phase noise. Accordingly, in order for the TX and DAC phase noise to feed-forward cancel, the I LO phase noise shifted by +90° must equal the Q LO phase noise. A common LO architecture, used in this paper, consists of a 2x clock divider, a 25% generator, and LO buffers and routing. This architecture can be analyzed to determine what portions of the input phase noise spectrum appear at the I and Q LO outputs with the required +90° relationship.

The divider and 25% generation circuit pass or invert the input edges of the 2x frequency input clock to generate the edges of the differential 25% I and Q waveforms, seen in Fig. 6. In [22], a hard-switched waveform with timing noise can be represented as the ideal waveform plus noise pulses at each edge. The noise pulses on the input LO edge are transferred to the I and Q LOs with a positive sign if the associated input edge is passed to the output, and with a negative sign if the associated input edge is inverted to the output. Consequently, in the time domain, the input phase noise is multiplied with the I and Q sampling sequences shown in Fig. 6 to produce the phase noise on the I and Q LOs. In the frequency domain, the source phase noise is thus convolved, or folded, by the Fourier series coefficients of these I and Q sampling sequences. These coefficients can be computed as $I_{\text{Sample,Noise}} \propto (1 - j^n)$ and $Q_{\text{Sample,Noise}} \propto -(1 + j^n)$ for odd n, and 0 otherwise, where n is the index of the harmonic.

The effect of the Fourier series coefficients on noise folding is shown in Fig. 7. The nonzero coefficients give insight into which source noise terms fold to the fundamental. The phase of the coefficients dictate the phase relationship of the noise translated from the source to the I and Q LOs. The sequences have no dc term and contain only odd harmonics. Accordingly, phase noise around $\pm 2kF_{\text{TX}}$ is folded to the TX fundamental. Noise around $\pm 2(2k+1)F_{\text{TX}}$ folds with a +90° phase relationship onto the I and Q LOs, while noise around

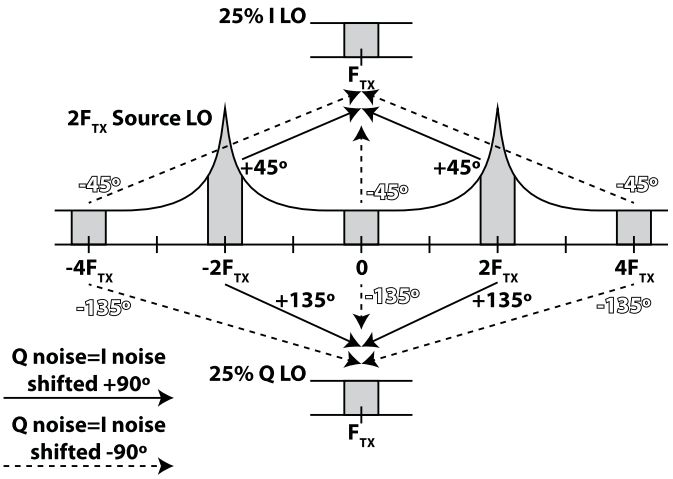


Fig. 7. Phase difference between source phase noise folded to I and Q outputs.

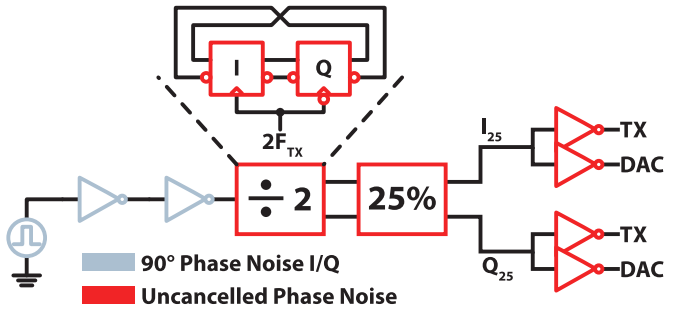


Fig. 8. LO chain annotated with correlated versus uncorrelated$I$ LO and Q LO noise components.

$\pm 4kF_{\mathrm{TX}}$ folds with a $-90°$ relationship and accordingly cannot be cancelled. This is due to the alternating $+90°$ /$-90°$ relationship between the Fourier series coefficients of $I_{\mathrm{Sample,Noise}}$ and $Q_{\mathrm{Sample,Noise}}$.

Additionally, noise injected by the current-mode logic clock divider in Fig. 8, does not maintain the required $+90°$ I/Q noise phase relationship. Because the I and Q divided LOs output from separate latches, output edge information is not shared between the latches; e.g., skew added by the latch on an I edge does not affect a Q edge. Therefore, the injected I noise is uncorrelated with Q noise. The TX/DAC LO chain, with indication of which sources have cancelled phase noise, is shown in Fig. 8.

The relevant design principle from this section is, therefore, to minimize the amount of uncorrelated noise between the TX and DAC LOs which does not maintain the +90° phase relationship between I and Q. This includes the folded far-from-carrier phase noise, noise in the clock divider, noise from buffers unshared between the I and Q LO paths, and noise from buffers unshared between the TX and DAC. The split point in the TX/DAC clock tree must therefore be pushed as close to the end of the signal chain as possible.

C. TX Thermal Noise

As stated in Section II, the TX must provide a low code-independent output impedance in order to minimize the IL on the receive side. As an SCPA is used as the TX, the real part of its output impedance reflected through the TX transformer acts as a loss element preceding the RX, degrading RX NF. The noise model is shown in Fig. 9, where the TX is replaced by its Thevenin equivalent. The RX NF is computed as:

$$10\log_{10}\left(1+\frac{R_{\mathrm{TX}}}{R_{\mathrm{ANT}}}+\frac{V_{\mathrm{n,RX}}^2}{V_{\mathrm{n,ANT}}^2}\right) \tag{6}$$

where R_{TX} and $R_{\mathrm{ANT}}$are TX and antenna resistances, and $V_{\mathrm{n,RX}}$ and $V_{\mathrm{n,ANT}}$ are the RX and antenna noise voltages.

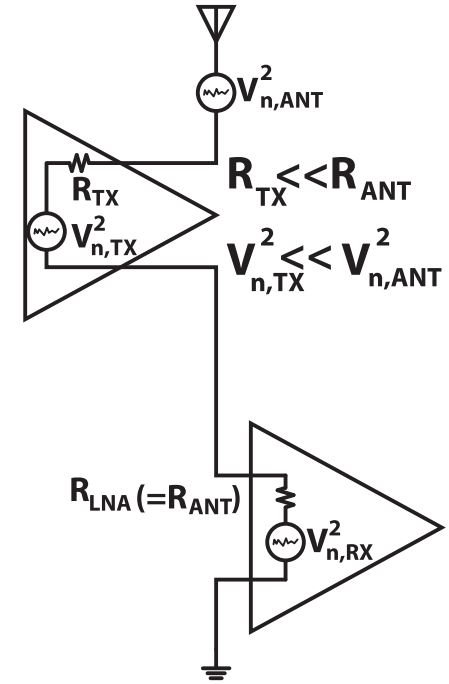


Fig. 9. Equivalent model for noise analysis of TX.

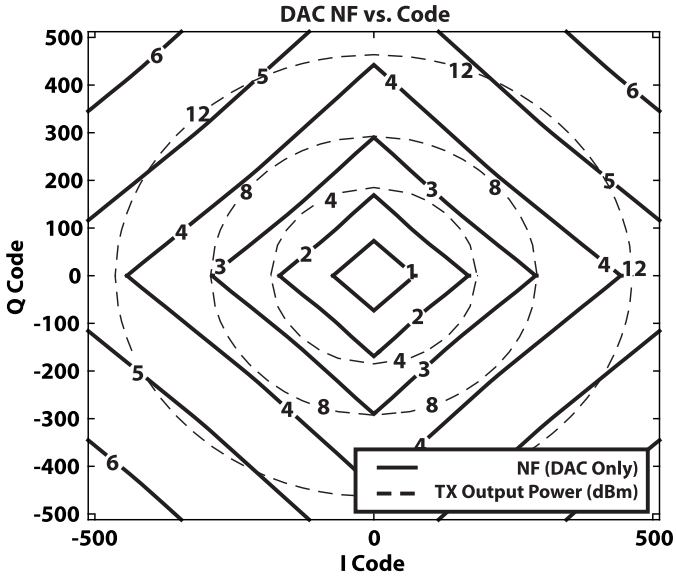


Fig. 10. Noise contribution of DAC versus TX output for both amplitude and phase.

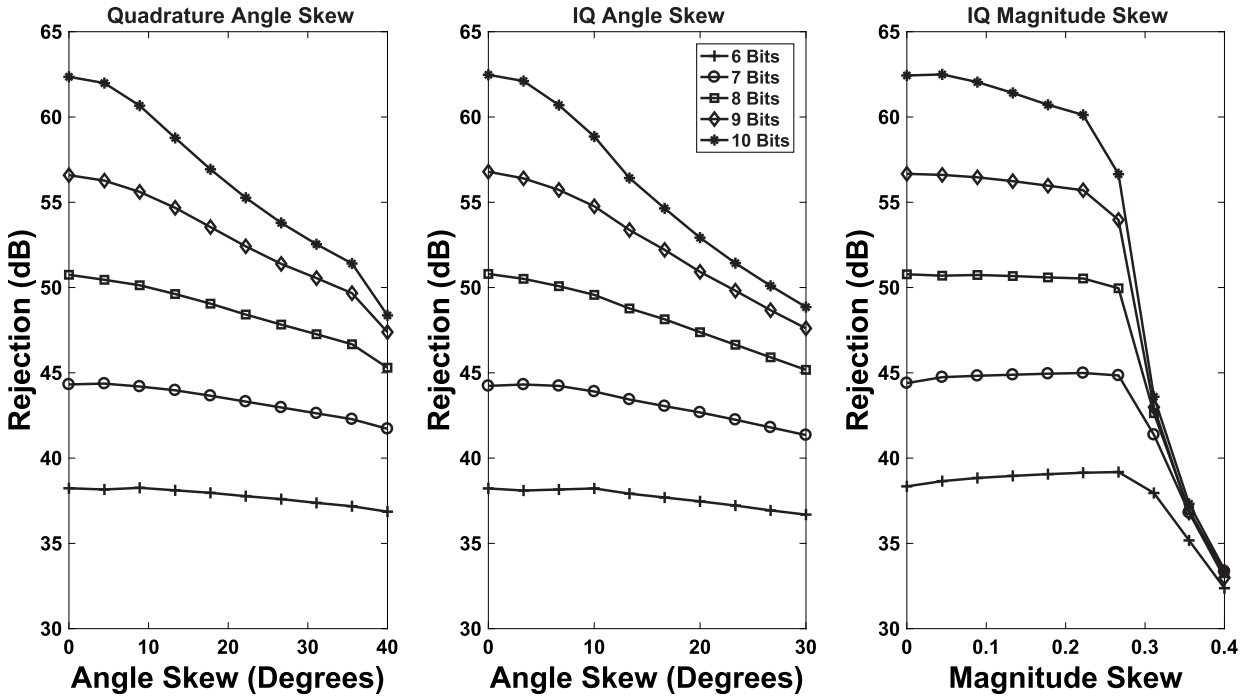
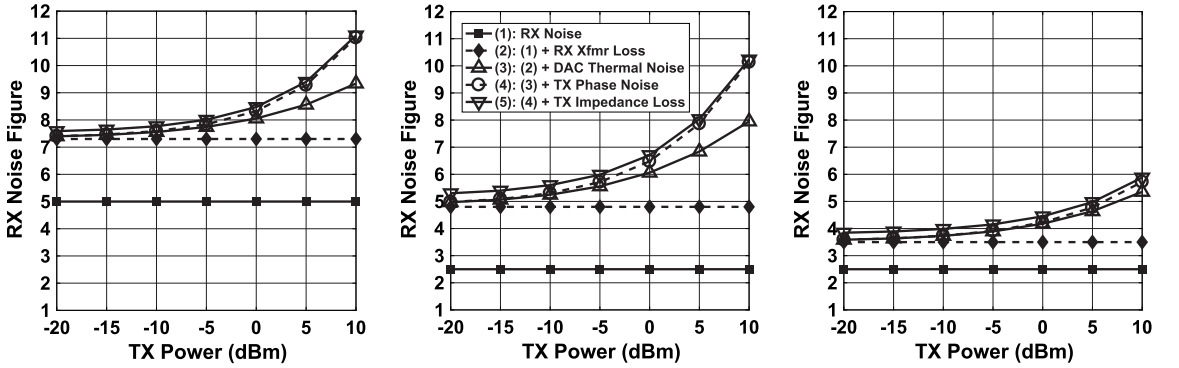


Fig. 11. Achievable rejection versus DAC nonlinearity mechanisms.



RX NF (dB)	5
RX Xfmr Loss (dB)	2.3
N_{Turns}	2
R_{TX} (Ω)	12
V_{OD} DAC (mV)	400
Uncorrelated Phase Noise (dBc/Hz)	-180

a)

RX NF (dB)	2.5
RX Xfmr Loss (dB)	2.3
N_{Turns}	2
R_{TX} (Ω)	12
V_{OD} DAC (mV)	400
Uncorrelated Phase Noise (dBc/Hz)	-180

b)

RX NF (dB)	2.5
RX Xfmr Loss (dB)	1
N_{Turns}	2
R_{TX} (Ω)	7
V_{OD} DAC (mV)	800
Uncorrelated Phase Noise (dBc/Hz)	-190

c)

Fig. 12. RX NF versus TX power (a) at the design point of this work (b) with a lower NF RX (c) with aggressive design conditions.

Because $R_{\mathrm{TX}} \ll R_{\mathrm{ANT}}$ this term is relatively small; concretely, if the RX nominally has a 2.5-dB NF and $R_{\mathrm{TX}} = 12\Omega$, the NF degradation is 0.5 dB.

D. Replica DAC Thermal Noise

The thermal noise injected by the DAC during cancellation is an important consideration, because it appears before any amplification. To derive the DAC thermal noise as a function of TX leakage power, it is useful to first consider the noise contribution of a single unit cell.

Given the DAC implementation in this paper, further described in Section III-B, a unit cell can be modeled as a noisy tail current source, cascaded with a noiseless mixer, as presented in Fig. 3(a). The mixer waveform's fundamental folds noise from around baseband and $2\mathrm{F_{TX}}$ to appear in the RX band. A 500-pH inductance with a Q of 5 at 4 GHz is synthesized by using a printed circuit board (PCB) via. This via inductance resonates with the 3 pF of tail parasitic capacitance to reject $2\mathrm{F_{TX}}$ noise by greater than 10 dB from 2.4–4 GHz, shown in Fig. 3(b). Higher harmonics have much lower conversion gain, and therefore add approximately 1.5 dB to the total noise. The analysis below focuses on the noise contribution of the fundamental. Representing the conversion gain of the mixer as A_{Conv}, the tail g_m noise which appears at the RX input is given by $i^2_{\mathrm{n,Unit}}/\Delta f = 8kT\gamma A^2_{\mathrm{Conv}} I_{\mathrm{Unit}}/\mathrm{V_{od}}$, where V_{od} is the transistor overdrive voltage and γ is the transistor noise factor. The tail currents of each unit cell

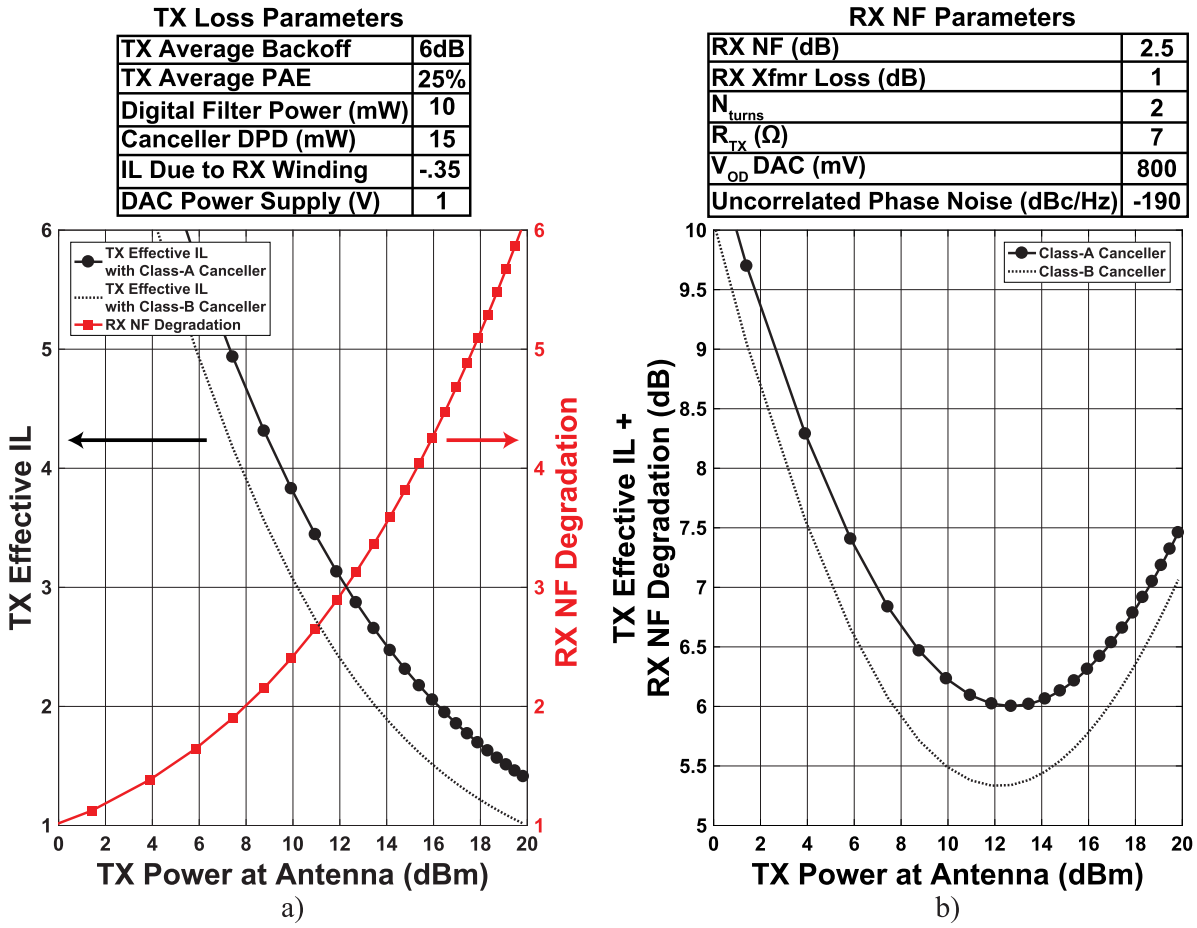


Fig. 13. TX IL summary (a) TX effective IL including canceller power vs. TX power at the antenna (b) sum of TX effective IL and RX NF under the assumptions of Fig. 12(c).

produce uncorrelated noise; the unit cell current noise sources add in power. For a 45° phase, (3) can be used with $I_{\mathrm{TX}} = (2P_{\mathrm{TX}}/R_{\mathrm{ANT}})^{1/2}$ to yield

$$I_{\mathrm{DAC}} = nI_{\mathrm{Unit}} = \sqrt{\frac{P_{\mathrm{TX}}}{2R_{\mathrm{ANT}}}}\frac{\pi}{N_{\mathrm{turns}}} \tag{7}$$

where n is the number of enabled unit cells and N_{turns} is the RX balun turns ratio. Therefore

$$\frac{i_{\mathrm{n}}^2}{\Delta f} = 4kT\gamma\sqrt{\frac{2P_{\mathrm{TX}}}{R_{\mathrm{ANT}}}}\frac{1}{N_{\mathrm{turns}}\pi}\frac{1}{\mathrm{V_{od}}}. \tag{8}$$

As detailed in Section III-B, the DAC in this work uses a 25% I/Q cell-sharing technique, where each unit cell outputs a 50% ($I = Q$) or 25% ($I = 0$ or $Q = 0$) square wave, causing the output noise to be dependent on the phase of the TX leakage. For example, the expression for output noise power for a phase of 0° is $2^{1/2}$ lower than for 45°. If the DAC is segmented as all thermometer bits, a reasonable simplification because thermometer cells are the largest and therefore dominate the noise, the total DAC noise can be rewritten as:

$$\frac{i_{\mathrm{n,total}}^2}{\Delta f} = 4kT\gamma\sqrt{\frac{P_{\mathrm{TX}}}{R_{\mathrm{ANT}}}}\frac{1}{V_{\mathrm{od}}}\frac{1}{N_{\mathrm{turns}}\pi}(|\cos(\varphi)| + |\sin(\varphi)|) \tag{9}$$

where φ is the phase of the TX leakage. The NF with both the RX and DAC follows:

$$F_{\mathrm{Total}} = F_{\mathrm{RX}} + \gamma\frac{N_{\mathrm{turns}}}{\pi}\frac{1}{V_{\mathrm{od}}}\sqrt{R_{\mathrm{ANT}}P_{\mathrm{TX}}}(|\cos(\varphi)| + |\sin(\varphi)|). \tag{10}$$

As DAC noise is proportional to (P_{TX}), the average noise power for a modulated sequence with XdB PAPR is approximately ($X/2$) dB lower than the noise of the maximum code in the sequence.

Fig. 10 shows the NF given thermal noise of the DAC, assuming a noiseless RX, a fully thermometer coded DAC, and accounting for noise folding from all harmonics. It is important to note that for every 1 dB the PA increases in power, the DAC output noise power increases by only 0.5 dB. There additionally exists a tradeoff between power consumption of the DAC and NF degradation through manipulation of the RX transformer turns ratio, as I_{DAC} is inversely proportional to N_{turns} and $(R_{\mathrm{ANT}})^{1/2}$.

E. DAC Linearity Requirements

Digital predistortion (DPD), namely, selecting the closest DAC constellation point for a given TX code, significantly relaxes the requirement for DAC linearity when compared

with a simple linear filter. As the number of DAC bits relative to TX bits increases, the constellation space becomes denser, reducing the average error between TX leakage and the replica DAC signal, even in the presence of significant nonlinearity. The dominant sources of constellation distortion are quadrature angle skew and I/Q summation nonlinearity. In an ideal complex DAC, the outputs of code I and code jQ are currents 90° out of phase. Quadrature angle skew is defined as the deviation from 90°, $\varphi_{\text{Skew}} = \angle I_{I=0} - \angle I_{Q=0} - \pi/2$. Similarly, summing the outputs of code I and code jQ separately should produce a result close to sending the complex code $I+jQ$. The deviation from this ideal has both a magnitude and phase component, defined as $A_{\text{Skew}}e^{j\varphi_{\text{Skew}}} = I_{I=Q}/(I_{Q=0} + I_{I=0})$. As seen in Fig. 11, >50 dB cancellation is achieved for even significant sources of constellation distortion, such as >30° quadrature and I/Q summation angle and 30% I/Q summation magnitude skew, by using 10 bits with DPD. Sources of DAC I/Q summation nonlinearity are examined in Section III.

F. RX/TX Loss and Noise Summary

The effects of Section II can be combined to determine total RX NF degradation versus TX output power. Summarized, the RX NF degradation is composed of: 1) loss through the RX transformer; 2) cancellation DAC thermal noise; 3) TX/DAC phase noise sources falling in the RX band which cannot be feed-forward cancelled; and 4) noise and loss from the series TX impedance, as translated through the TX transformer.

Fig. 12 plots these degradations for 2.5 and 5 dB nominal NF RX designs. The RX transformer loss, DAC thermal noise and un-cancelled phase noise are added at our design points of 2.3 dB, $V_{\text{od}} = 400\ mV$, $N_{\text{turns}} = 2$, and -180 dBc/Hz, respectively. Our implemented SCPA and lossy TX transformer present an effective 12 Ω series resistance from the antenna to RX input.

It is worth noting that the NF degradation is implementation dependent. The RX transformer loss can be improved in an ultra-thick metal process. DAC thermal noise and phase noise must be determined primarily by budgeted power. The TX impedance in the SCPA topology is reduced without incurring a TX efficiency penalty in scaled process nodes, due to lower switch resistance for the same capacitance. As a more aggressive baseline, RX NF under assumptions of a 2.5-dB NF RX, 1-dB RX transformer loss, DAC $V_{\text{od}} = 800\ mV$, $N_{\text{turns}} = 2$, -190 dBc/Hz, and 7Ω series TX impedance is also plotted in Fig. 12.

On the TX side, TX efficiency is effectively degraded by: 1) series loss in the RX winding, which results in imperfect reflection of the TX virtual ground on the RX side of the transformer to the antenna side and 2) canceller power consumption, including the digital filter required for wideband cancellation, and canceller DPD. At our design point, the TX incurs 0.35 dB of loss when connected in the series RX/antenna stack with chip to PCB interface parasitics, as compared with a TX connected directly to the antenna through the same parasitics. Eight taps of 200-Ms/s filtering on the 10 bit DAC data with 10 bit coefficients is estimated to consume 10 mW [23], while a canceller DPD reusing the existing RX chain to close the adaptation loop is estimated to consume 15 mW [24].

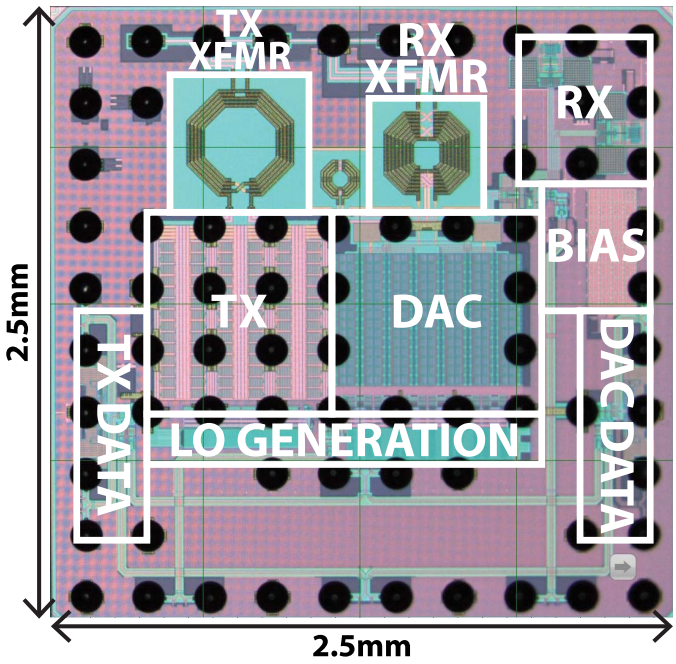


Fig. 14. Die photograph.

Fig. 13(a) plots the effective TX IL including canceller analog plus digital power for a system with 6-dB back-off and 25% average power added efficiency (PAE). At low TX powers, the assumed constant power of the digital filtering and DPD dominate the PA output power, reducing efficiency. While our system implements a class-A DAC, a class-B DAC would save significant power in systems operating under back-off. The sum of TX IL and RX NF degradation under the assumptions of Fig. 12(c) is plotted in Fig. 13(b). The scheme compares well with practical implementations of electrical balance duplexers at a range of power levels, while enabling cancellation over frequency selective antenna interfaces and wide operating frequency.

III. Circuit Implementation

A test chip for this system is implemented in a 65-nm CMOS process, shown in Fig. 14, and includes an on-chip CMOS PA, a measurement RX, cancellation current DAC, front-end transformer network, LO dividers, and 10-Gb/s baseband data inputs for the TX and DAC.

A. Switched-Capacitor Power Amplifier

The SCPA, shown in Fig. 15 and described in detail in [25] and [26], is used in this work primarily for its low code-independent output impedance, which is needed for the series TX/RX combination. As all capacitor bottom plates are connected to an ac ground independent of the amplitude code word, the full PA array capacitance always appears in shunt with the transformer inductance. Around its center frequency, the *LC* resonance thus provides a low impedance across all

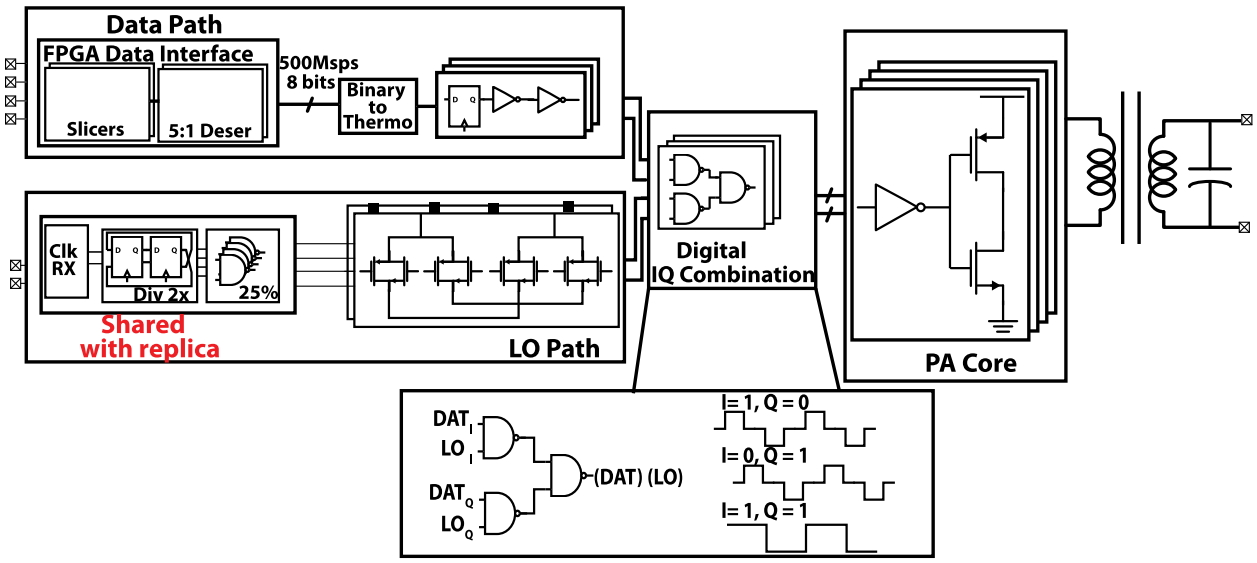


Fig. 15. TX chain top level schematic.

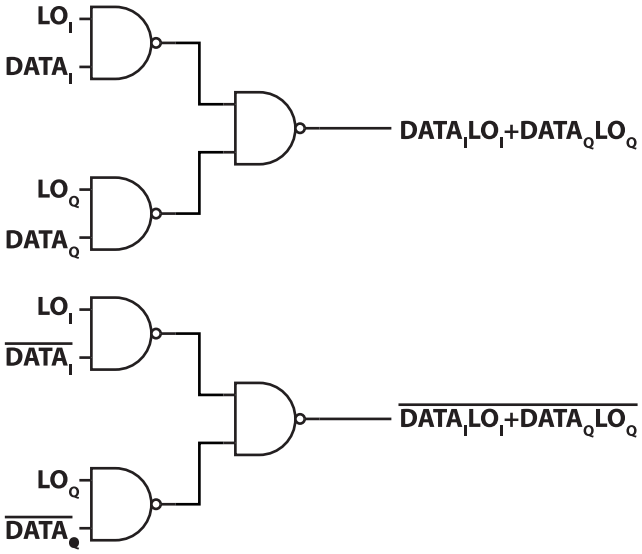


Fig. 16. Data and 25% LO combination driving TX and DAC unit cells.

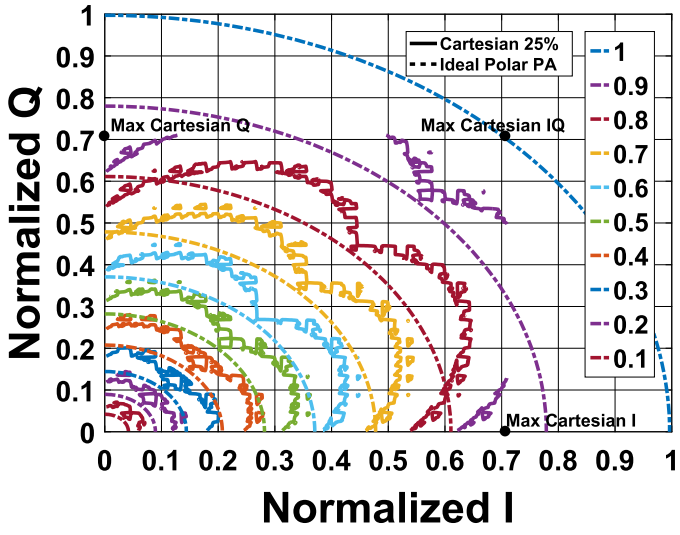


Fig. 17. Ideal 25% combination efficiency contour.

amplitude code words. The series switch resistance can be made code-independent by sizing the PMOS and NMOS transistors to have similar on-resistance. Because these devices are sized for low on-resistance to achieve high efficiency, any residual mismatch and code dependence is small compared to the resistance due to the Q of the transformer.

As described in Section II, the PA and cancellation DAC's LO paths should be shared as much as possible to mitigate TX's phase noise impact. A polar PA architecture is not appropriate, as it requires independent phase interpolators in the DAC and TX LO paths, adding significant uncorrelated phase noise. Accordingly, a Cartesian PA topology is implemented.

A noted problem with the Cartesian topology is that if an I PA and Q PA segment each consume half the dc power of an equivalent polar TX, the total efficiency is degraded by $\sqrt{2}$ due to out of phase summation. To overcome this efficiency penalty, a 25% duty cycle LO is used here, similar to [27], [28]. In this technique, the I and Q phases are time multiplexed on a single PA unit cell, by the use of 25% waveforms as shown in Fig. 15. The data and LO combination to each unit cell is implemented as NAND gates as shown in Fig. 16, noting that if the 25% duty cycle I and Q waveforms are provided as input, the unit cell should be switched if DATA_I AND LO_I are active, or DATA_Q AND LO_Q are active.

The ideal efficiency of the combination scheme can be derived as the contour plot in Fig. 17 by computing the total amount of capacitance switched per cycle. Note that at the 45° phase angle, the LO waveform matches the polar case, and the peak efficiency is the same. Similarly, when driven at peak I, or Q phase, the ideal peak efficiency is still 100%, as it would be in the polar case. A penalty is incurred at other phase angles, as shown in the plot.

The PA is implemented with 8 bits, segmented as 4 binary and 4 thermometers. In this implementation, non-stacked

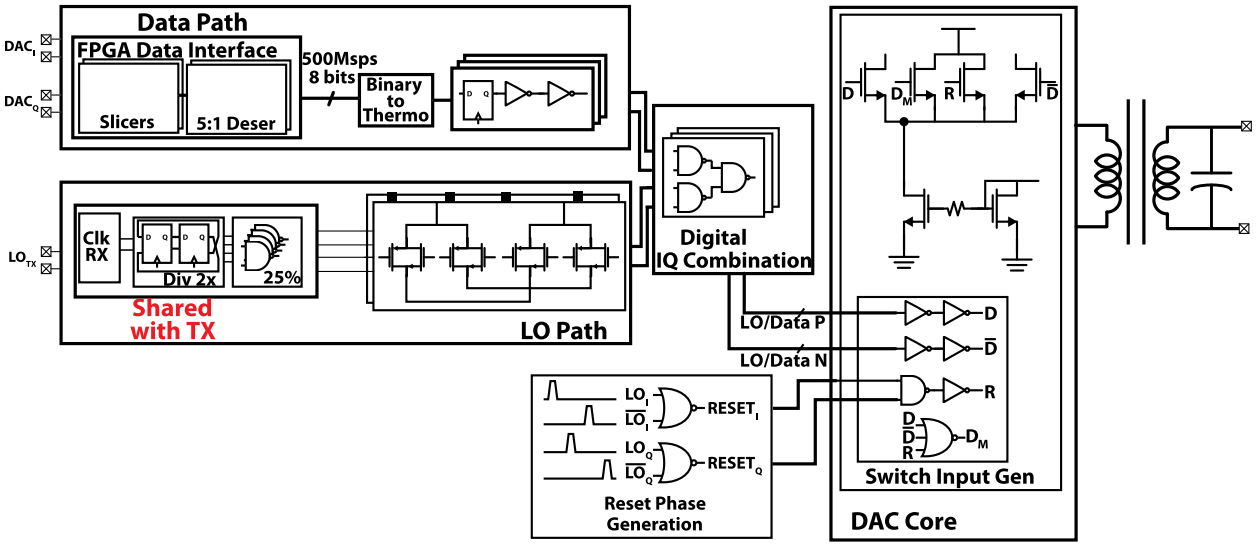


Fig. 18. Cancellation DAC chain top level schematic.

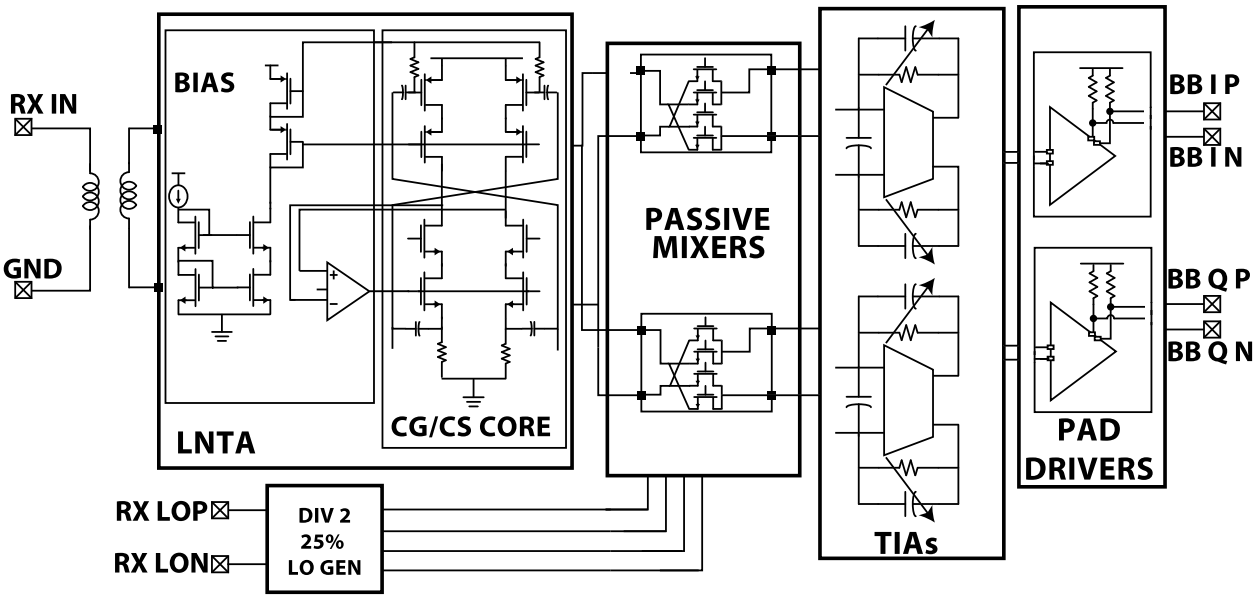


Fig. 19. RX chain top level schematic.

inverters are used, as the target output power can be achieved in a differential implementation with a 1:2 transformer turns ratio and a 1.2-V supply. A measured peak power of 18.8 dBm is achieved at 42% peak PAE including loss from the on-chip transformer.

B. Cancellation Current DAC

The DAC is constructed with static tail devices connected to hard-switched transistors which provide both mixing and data modulation, shown in Fig. 18. It is implemented with 10 bits, segmented as 5 binary and 5 thermometers. The DAC also uses an I/Q cell-sharing technique, allowing reuse of the TX LO generation to minimize the uncorrelated phase noise between the TX and DAC. When a cell is unused, its tail current is shunted to the center tap by turning on the MID switch, which provides for fast output current rise time, and therefore good dynamic linearity. High unit cell output impedance, provided by the hard-switched cascode devices, is important because the output impedance is inversely proportional to the magnitude of the DAC code.

Independent DAC and TX 10 Gb/s data links were implemented to interface with an FPGA in order to enable off-chip digital filtering of the DAC data relative to the TX data, to maximize cancellation. As stated in Section I-E, nonlinear predistortion allows the 10 bit DAC to reach 50 dB of cancellation despite I/Q nonlinearity. This nonlinearity stems from several sources. First, a 25% output requires four switch transitions, while the 50% requires only two, creating inherent differences in the waveforms. Skew in the MID signal versus the differential signals can also cause I/Q nonlinearity. Finally, any bandwidth limitations in the routing network will affect 25% waveforms more severely than 50% waveforms due to their reduced width.

To support the DAC noise model referenced in Section II, it is important to note that only one cascode switch is enabled at a given time. Therefore, the source impedance of the

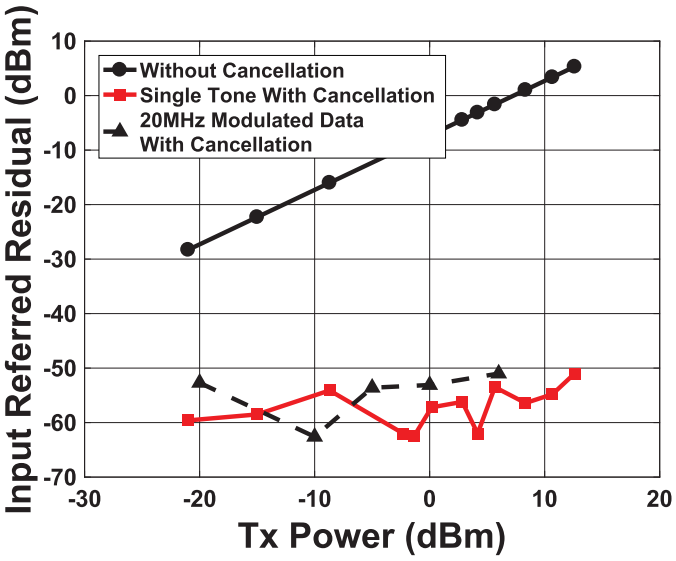


Fig. 20. TX fundamental referred at RX input versus TX power at antenna, 1.3-GHz TX signal at 40-MHz TX/RX spacing.

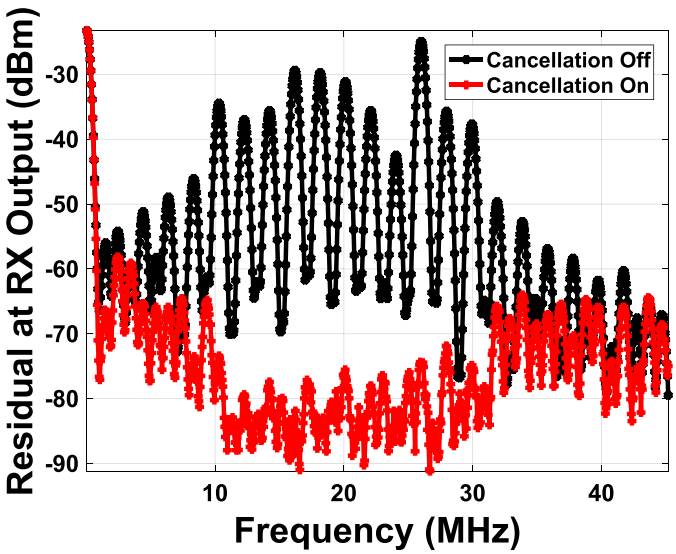


Fig. 21. Spectrum at RX output before and after cancellation enabled, 1.3-GHz TX signal at 20-MHz TX/RX spacing.

cascode switch is only due to the tail device and any routing capacitance. The unit cell is constructed in a compact manner so as to maximize the bandwidth of the tail drain. This causes the majority of switch noise to circulate, due to the high impedance provided by the tail current source. Noise from the biasing network is narrow-banded by a 1-MHz series *RC* filter.

C. Measurement Receiver

In order to measure the efficacy of the proposed cancellation scheme in a realistic environment, a RX powered from a 2.5-V supply is implemented on the same die. The RX prioritizes linearity and measurement flexibility over noise performance to enable various testing modes. The top level block diagram of the RX is shown in Fig. 19, consisting of a complementary common gate/common source low-noise transconductance amplifier driving current-mode passive mixers, followed by first order shunt feedback baseband transimpedance amplifiers (TIAs) with tunable gain and bandwidth settings. The RX's gain is 18 dB, to reduce the -160 dBm/Hz noise of the measurement equipment below the thermal noise floor. The RX has an Out-of-band IIP3 of +10.2 dBm at a nominal NF of 7.6 dB when measured from the antenna port with the TX at code 0. This is composed of 4.7-dB NF from the RX chain, and 2.9-dB loss from the RX transformer and the SCPA series impedance reflected through the TX transformer.

IV. Measurement Results

A. System Cancellation Measurements

First, single-tone cancellation is evaluated as shown in Fig. 20 by sweeping the TX power at the 45° phase angle ($I = Q$). The residual power referred to the RX input is plotted against the power at the antenna port. The plot first shows the TX signal that would be present at the RX input without any cancellation. This is measured at lower codes that do not damage the RX and linearly extrapolated. This power present at the RX input without cancellation is 3 dB lower than the TX power at the antenna with cancellation, the x-axis, because the PA power is equally divided between the antenna and the RX when cancellation is disabled. The measured residual at the input of the RX is independent of TX output power, as the residual is set simply by the LSB of the DAC once the appropriate cancellation code has been found. At the highest measured single-tone power of +12.6 dBm, $>$50 dB of digitally assisted analog cancellation is observed.

Cancellation with 20-MHz modulated data is also measured at over 50 dB in Fig. 21. Periodic TX and DAC sequences of length 128 were sent at a line rate of 2.5 Gb/s. Accordingly, this test setup limits the TX and DAC to produce sequences with Fourier series coefficients at 2-MHz spaced tones. This is suitable for testing purposes, corresponding to 10 random power tones spaced with a 20-MHz bandwidth. The sequences were designed to produce a peak-to-average power ratio of around 6 dB, to represent a realistic modulated signal. The DAC sequence is continuously closed-loop adapted, to minimize power in the 20-MHz cancellation bandwidth.

The residual is shown in Fig. 22 from 1 to 1.8 GHz by fixing the TX to produce a 0-dBm output as the TX LO is swept. Additionally, at a fixed 1.4-GHz center frequency, the antenna impedance is varied over impedance points via a tunable-length transmission line to create a VSWR up to 5:1, shown in Fig. 23. After digital adaptation of the DAC input sequence, the residual TX signal is still limited by the DAC LSB, demonstrating the flexibility of the cancellation system due to the wideband nature of the DAC, the low impedance of the summing junction, and the digital adaptation of the input data.

The RX band noise floor at a 40-MHz duplex offset is measured as the power of a single-tone TX output is swept with the cancellation enabled, shown in Fig. 24. At a +2 dBm TX output power the system incurs a moderate 1.7-dB noise penalty, with a 4.3-dB penalty at +10.6 dBm. This degradation of the baseline 7.6-dB NF closely matches the calculations

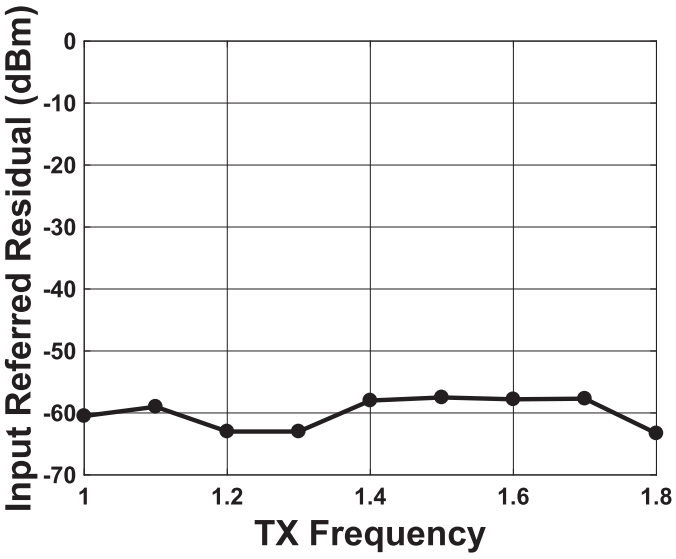


Fig. 22. TX fundamental referred to RX input for 0-dBm TX power at antenna versus TX center frequency.

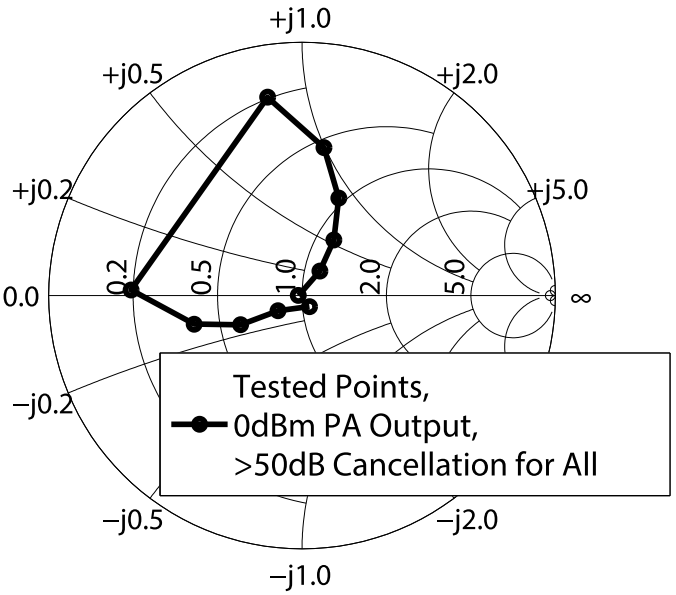


Fig. 23. Measured antenna impedance points with up to 5:1 VSWR, at TX frequency 1.4 GHz. The antenna load consists of a 60-cm SMA cable to a spectrum analyzer, in shunt with a 22-cm tunable transmission line terminated with a short. This is connected via SMA to an 18-mm 50-ohm transmission line to the chip.

of Fig. 12(a), and accounts for all the non-deterministic noise sources which cannot be further cancelled in the digital back end, primarily DAC thermal noise and TX phase noise. RX sensitivity with modulated data can be performed only after optimal back-end digital correction is applied to cancel the residual TX and DAC noise terms due to quantization and nonlinearity. For single-tone, such terms are periodic and outside the RX band, enabling this measurement.

RX linearity is measured as TX power at the antenna is swept through RX gain compression and triple beat. Note that the TX fundamental is always cancelled by >50 dB. Accordingly, the triple beat of an RX-band tone, and a two tone TX signal with the 50-dB cancellation of the fundamental exceeds a practical specification of 70 dB across the entire

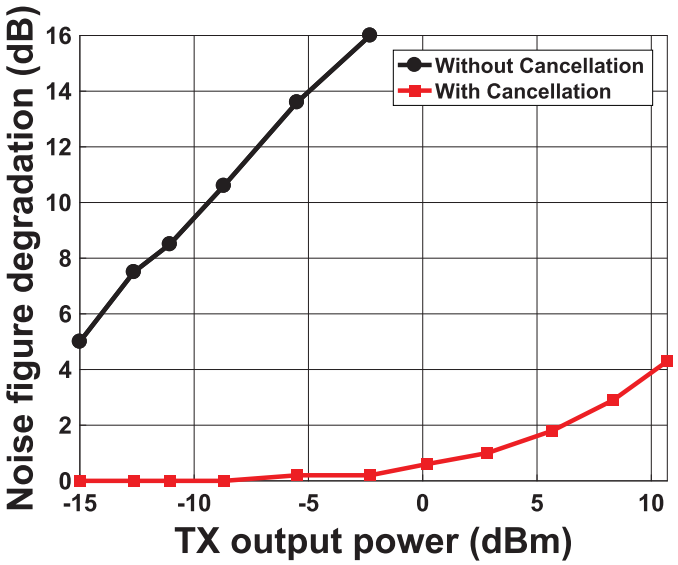


Fig. 24. RX NF degradation versus TX power at antenna, 1.3-GHz TX frequency, 40-MHz TX/RX spacing.

antenna power range. However, because the TX and DAC output weighted square wave LOs, the TX and DAC outputs contain strong harmonic content. As the DAC is filtered to match the TX only at the fundamental, the third harmonic is un-cancelled, and limits the max TX power for simultaneous operation in our implementation. The worst-case triple beat is thus due to the un-cancelled third harmonic of two 1-MHz spaced TX tones and an in-band RX tone measured in Fig. 25. As the third harmonic is un-cancelled, a 1-dB increase in TX output power results in a 2-dB decrease in triple beat. Harmonic rejection techniques and additional filtering at the third harmonic would thus allow operation at higher TX output power levels.

B. Phase Noise Cancellation

In the first test, spurs are injected at the input of the shared TX/DAC LO port to verify the folding relationships given by the Fourier series from Section II-B, as illustrated in Fig. 26. The resulting phase noise spurs on the I LO and the Q LO are measured separately through setting the PA to transmit in the I phase or the Q phase. The measured phase between these spurs is consistent with the Fourier series coefficients from Section II-B and Fig. 7.

Next, a single sideband spur at $2F_{\mathrm{TX}}+F_{\mathrm{Offset}}$ is injected into the shared LO port input. Consistent with the analysis, the spur is downconverted to $F_{\mathrm{TX}}+F_{\mathrm{Offset}}$, and measured with and without the cancellation DAC enabled. The result is plotted in Fig. 27—the close-in spur cancellation is >35 dB, while the cancellation of a spur in the RX band at 40-MHz spacing is >20 dB. This result confirms a conclusion of Section II-B: a wideband TX to RX network is desired for wideband phase noise cancellation.

White noise from a source generator filtered by a 100-MHz tunable bandpass filter is then injected into the LO port. As the noise is filtered to a narrow bandwidth around $2F_{\mathrm{TX}}$, no additional noise folding terms should contribute. The noise can simply be thought of as a sum of spurs, and results closely match spur cancellation.

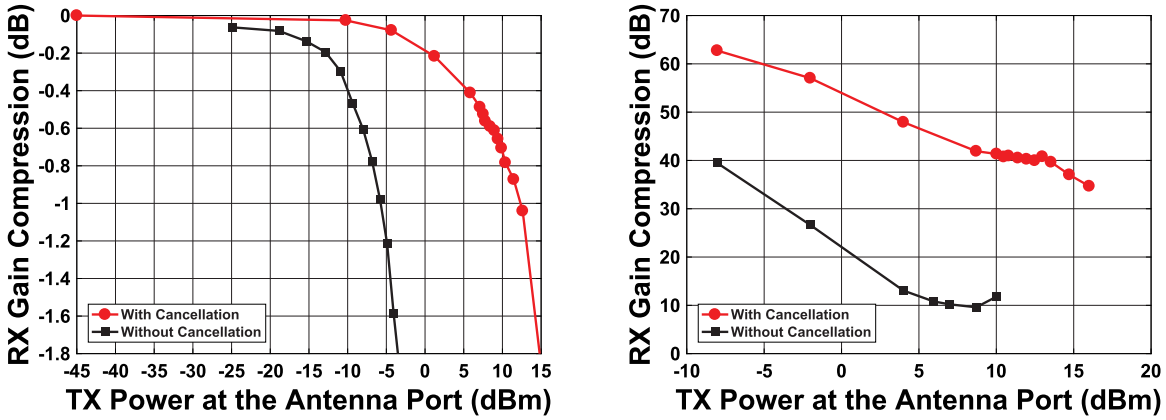


Fig. 25. RX linearity versus TX power in the form of (a) RX gain compression (b) Triple beat, both measured at 1.3-GHz TX frequency, 40-MHz TX/RX spacing.

TABLE I
COMPARISON TABLE

	[16]	[19]	[18]	[14]	[15]	[17]	This Work
Duplex Scheme	FD	FD	-	FDD	FDD	FDD	FDD
Architecture	BB Vector Modulator	N-Path Circulator	Feed-Forward Canceller	CG/CS LNA Canceller	RF Equalizer	Distributed Amp	Cancellation DAC
Frequency (GHz)	.15-3.5	.6-.8	2.3-2.5	.3-1.7	.8-1.4	.3-1.6	1.0-1.8
TX/RX Offset (MHz)	0[1]	0[1]	-	105	115	115	40
Max TX Power Leakage (dBm)	+1.5	-6	0	+2	-4	+14[2]	+12.6
Cancellation at Max TX Power (dB)	>27	42	90	>30	33	>40	>50
Cancellation Over 20MHz Modulated Bandwidth (dB)	27	42[3]	50	-	20	>25	>50
RX NF (dB)	6.3	5.0	4.7	4.2[4]	4.8[4]	8-12	7.6
NF Degradation at +2dBm TX Power	4	5.9	.25	.8[5]	.9[5]	4-5[6]	1.1
Effective IIP3 at -4dBm TX Power(dB)	-	+1[1]	-	-	+25-27	-	+25
Fully-Integrated TX+RX	Yes	No	No	No	No	Yes	Yes
Canceller Power (mW)	23-56	89	-	13-72	44-182	0[7]	60 (+25[8])
RX Power (mW)		70	-	74.6-83	63-69	<100	40
TX Insertion Loss (dB)	-	1.7	5	-	-	0	.35
Noise Cancellation in RX Band (dB)	-	-	-	13	-	15	19
Active Area (mm²)	2	1.44	1	1.2	4.8	7.2	3.9
Technology	65nm	65nm	130nm	65nm	65nm	65nm	65nm

1) Full-Duplex 2) With RX-band TX degeneration 3) 12MHz modulation bandwidth 4) Antenna interface loss not included 5) TX power for this measurement not reported 6) NF degradation reported here

Noise close-in is cancelled by around 35 to 40 dB, while noise at 20-MHz offset is cancelled by around 20 dB.

Wideband phase noise with 3-GHz 3-dB corner is injected into the LO port to emulate the case of wideband source noise. Noise around $4F_{TX} + F_{Offset}$ is folded by the -3 sideband with $-90°$ phase relationship between I and Q, and accordingly is not cancelled. From the spur folding measurement above, the strength of this folding term is -20 dB relative to the strength of the noise term folded from $2F_{TX} + F_{Offset}$. This term remains after cancellation, limiting total cancellation to 20 dB, even close-in, verified in the wideband measurement of Fig. 28. Near the main tone, source phase noise overcomes injected white noise, obscuring results at small offsets.

This work is benchmarked against prior active cancellation systems in Table I. The system provides the highest cancellation across a 20-MHz bandwidth with <1 dB RX gain

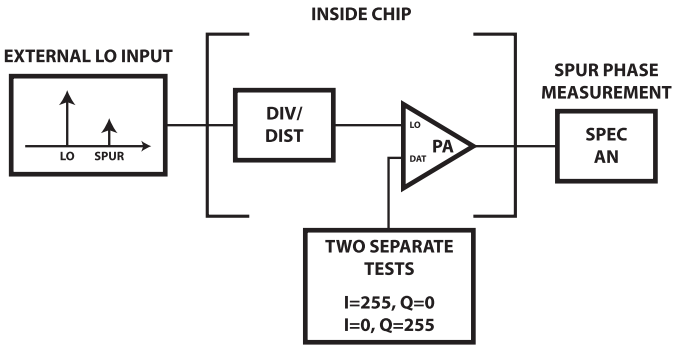


Fig. 26. Test setup for measuring I/Q folding phase relationship.

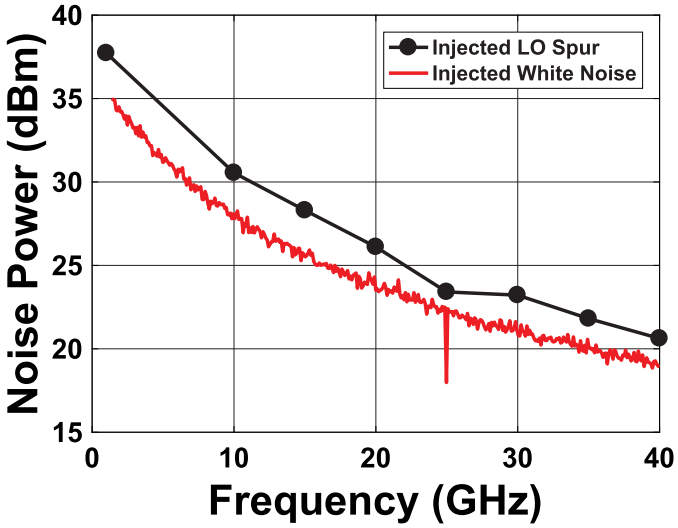


Fig. 27. Narrowband TX LO phase noise cancellation measured at RX output.

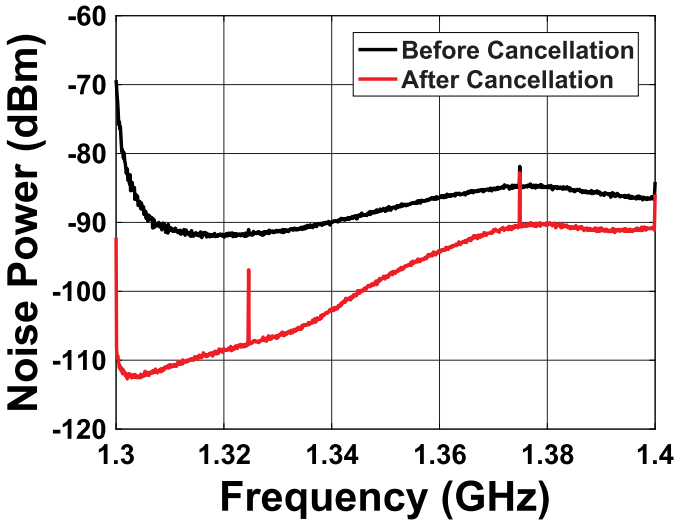


Fig. 28. Wideband TX LO phase noise cancellation measured at RX output.

compression at >10 dBm TX output power. Along with [17], this paper is among the first to fully integrate the TX, RX, and antenna interface. Triple beat linearity and maximum output power could be further improved through TX/DAC third harmonic cancellation techniques.

V. Conclusion

This paper demonstrates a frequency duplexed TX and RX with a single antenna interface and no external isolation elements integrated in a 65-nm CMOS chip. This is enabled by the series stacked combination with a low-impedance SCPA TX and high-impedance shunt cancellation replica. Digital adaptation of the input cancellation DAC data allows isolation to be maintained over a range of antenna impedances and operating frequency. Over 50-dB isolation is shown for 20-MHz modulated TX signals over an 800-MHz operating range, limited by the cancellation DAC resolution. TX phase noise falling in the RX band is analyzed and shown to be feed-forward rejected in the proposed architecture. Future extensions to this paper could include a digital back-end for TX residual cancellation, potential thermal noise reduction techniques in the cancellation DAC, and extension of the maximum TX output power to LTE-like specifications.

Acknowledgment

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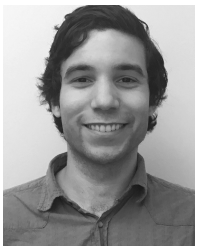

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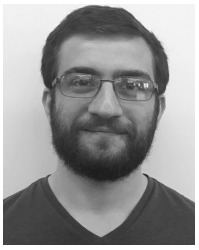

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