A Wideband 400 MHz-to-4 GHz Direct RF-to-Digital Multimode $\Delta\Sigma$ Receiver

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***Abstract*—A wide-tuning-range low-power sigma-delta-based direct-RF-to-digital receiver architecture is implemented in 65 nm CMOS. A flat signal transfer function is chosen to support wide-frequency-range radios. A multilevel (two-bit) nonreturn-to-zero DAC improves jitter immunity to enable a high dynamic range, and, with a class-AB low-noise transconductance amplifier, guarantees a highly linear front end. For a 4 MHz signal, the peak SNDR of the receiver exceeds 68 dB and is better than 60 dB across the 400 MHz to 4 GHz carrier frequency range. By virtue of utilizing a negative feedback digitizer close to the antenna, an IIP3 of +10 dBm is achieved while dissipating only 40 mW from 1.1 V/1.5 V supply voltages.**

***Index Terms*—ADC, bandpass ADC, CMOS, $\Delta\Sigma$ ADC, LNTA, receiver, software-defined radio.**

I. Introduction

CONTINUED evolution of wireless communications drives the need for flexible receivers capable of multimode, multistandard operation [1], [2]. A universal 4G-LTE device, for example, is anticipated to operate from 450 MHz to 3800 MHz with varying bandwidths. A downconverting $\Delta\Sigma$ analog-to-digital converter (ADC) is an architecture capable of such operation [3], [4]. By embedding the mixer inside the feedback loop, a highly linear design is achievable. By utilizing a low-noise transconductance amplifier (LNTA) in front of the $\Delta\Sigma$ ADC, this architecture can perform a low-noise direct RF-to-digital conversion. The center frequency is tuned by an external oscillator, and the bandwidth is set by the decimation filter. The high dynamic range of this architecture enables the ADC to migrate closer to the antenna, enabling many signal conditioning features to be implemented in the digital domain, thus benefiting from technology scaling.

While the direct-conversion architecture is still prevalent in commercial mobile handsets, significant research effort has shifted towards schemes that employ bandpass or downconverting $\Delta\Sigma$ ADCs. Previous implementations of downconverting $\Delta\Sigma$ receivers with switched-capacitor loop filters have demonstrated wide tuning range or high dynamic range, but not both [4], [5]. In general, the dynamic range has been limited by the clock jitter injected at high frequencies from the feedback digital-to-analog converter (DAC). Jitter directly degrades the SNDR of the receiver, since it cannot be distinguished from input noise. A nonreturn-to-zero (NRZ) signal waveform helps reduce the jitter sensitivity by reducing the transitions, while a multilevel DAC improves the jitter immunity by reducing the transition steps. However, both techniques are challenging to implement at high frequencies. This paper demonstrates a system that achieves a high dynamic range together with a wide tuning range, enabled by the implementation of a four-level NRZ DAC. The overall system linearity is further enhanced by a highly linear class-AB LNTA.

This paper is organized as follows. Section II discusses various architecture design tradeoffs in order to motivate the choices made in this design. Section III presents circuit implementation details, and Section IV presents measurement results. The paper is concluded in Section V.

II. $\Delta\Sigma$ Receiver Architecture

In the following discussion, various system architectures are evaluated and compared, and the impact of clock jitter is studied and analyzed. In addition, a behavioral model of a current-mode integration sampler (CMIS) mixer is derived. Finally, an architecture for such an implementation is proposed.

A. System-Level Design

To meet the requirements of software-defined radio (SDR) applications, an ADC has to overcome two major challenges. First, its dynamic range has to be sufficiently large to process the input signal together with blockers. It also needs to downconvert the input signal from the carrier frequency to baseband. A bandpass $\Delta\Sigma$ ADC (Fig. 1) is seemingly an ideal candidate for this application. However it requires resonators with high quality factors, which are difficult to realize in CMOS technology. Passive resonator designs offer higher Q, but come with a large area overhead and limited tuning range. Active resonators are tunable but suffer from limited quality factors. In addition, active designs incur a large power overhead and limit the system's linearity.

An alternative bandpass $\Delta\Sigma$ system is proposed in [6]. As diagrammed in Fig. 2(a), a bandpass feedback structure is formed by the summation of the feedback signals from the two interleaved channels. By using the idea of current mode integration sampling which would be elaborated later, the sampler in Fig. 2(a) can be transformed into a mixer and be moved inside of the $\Delta\Sigma$ loop, as shown in Fig. 2(b). The bandpass feedback suppresses signal swing at the RF nodes and enhances the linearity of both the LNTA as well as the baseband $\Delta\Sigma$ ADCs).

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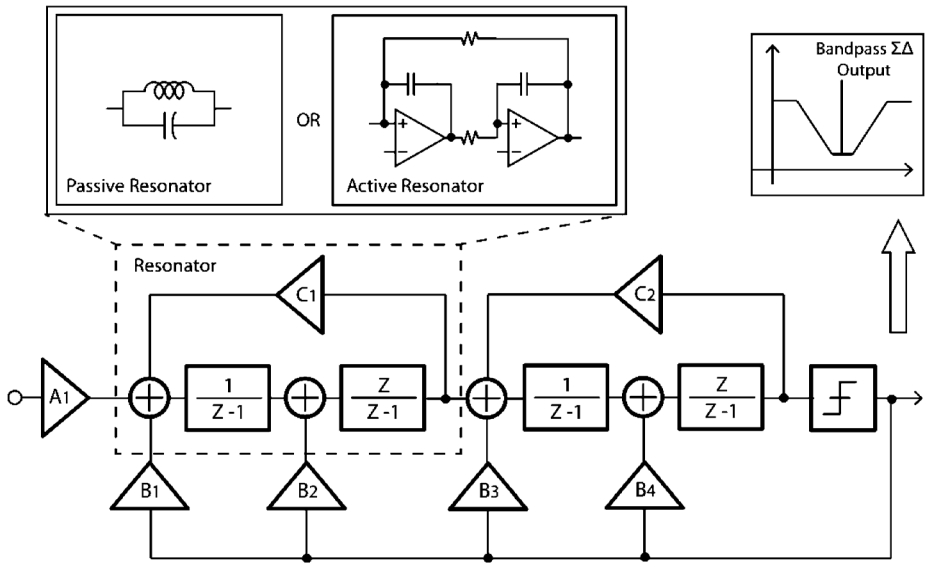

Fig. 1. Bandpass $\Delta\Sigma$ modulator loop filter in Z transform.

The two channels of the $\Delta\Sigma$ ADCs also serve to oversample the input data by a factor of two, thus providing a 3 dB SNR improvement.

B. Loop Filter Structure

There are numerous $\Delta\Sigma$ loop filter structures reported in literature [7]. As shown in Fig. 3, a second-order all-feedback cascaded integrators with distributed feedback (CIFB) structure is chosen for this design because of concerns for stability and peaking in the signal transfer function (STF). The STF and noise transfer function (NTF) of the chosen loop structure is shown in Fig. 4. The STF is ensured to be maximally flat for the entire band to maintain better wide-band blocker resilience. The NTF takes advantage of the large over-sampling ratio (OSR) between the baseband bandwidth specified by the wireless standards and the much higher carrier frequencies to provide the aforementioned large dynamic range.

1) Loop Stability: A major tradeoff in $\Delta\Sigma$ ADC design is between loop stability and the aggressiveness of the noise shaping. As demonstrated in [7], by optimizing complex poles and zeros, a more aggressive NTF can be achieved without raising the order of the loop filter or increasing the OSR. For ADC designs which are only targeted for a fixed sampling frequency, loop stability can be well compensated with additional tuning range in the feedback and feedforward factors [8], [9]. However, for SDR applications, the desired frequency of operation can spread over a decade, which results in complex loop structures such as CRFB (chain of resonators with weighted feedforward summation) or CIFF (chain of integrators with feedforward summation and local resonator feedback) that are far less appealing.

2) Peaking in the STF: Another challenge in the RF $\Delta\Sigma$ design is the flatness of the STF. As summarized in [7], common $\Delta\Sigma$ loop filter architectures are CIFB, CIFF, CRFB and CRFF (chain of resonators with weighted feedforward summation and local resonator feedback). CIFF and CRFF are popular choices in $\Delta\Sigma$ ADC design because a smaller number of feedback DACs is required; these DACs are often the design bottlenecks. However, a major drawback of the CIFF or CRFF design is ripple in the STF. Without a loss of generality, from the simple loop shown in Fig. 5, it can be shown that

$$NTF(z) = \frac{1}{1 + L(z)} \tag{1}$$

$$STF(z) = \frac{L(z)}{1 + L(z)} \tag{2}$$

$$L(z) = \frac{1}{NTF(z)} - 1 \tag{3}$$

$$STF(z) = NTF(z)L(z). \tag{4}$$

From (3) and (4), the poles in $NTF(z)$ become zero(es) in $L(z)$, and hence show up as zero(es) in $STF(z)$. This results in peaking in the STF. In some applications, such as audio CODEC, out-of-band (OOB) STF peaking can be tolerated due to the front-end anti-aliasing filters. However, for SDR, peaking in the STF degrades the receiver's OOB interference resilience. Due to the absence of front-end filtering, interference that coincides with the STF peaks would be "amplified" and hence desensitize the receiver. In the worst case scenario, it might exceed the ADC's full-scale range, causing the $\Delta\Sigma$ ADC to clip. Recent $\Delta\Sigma$ ADCs [5], [8], [10] have reported loop architectures with an FIR-feedback-DAC design. Embedding an FIR filter into the DAC is a low-power technique to alleviate the jitter sensitivity of a high-speed $\Delta\Sigma$ system, which is a major factor limiting its dynamic range. However, loop filters with an FIR DAC has large OOB STF peaking, making this technique unsuitable for SDR applications. For a FIR filter $F(z)$

$$\mathrm{NTF}(z) = \frac{1}{1 + F(z)G(z)} \tag{5}$$

$$STF(z) = \frac{G(z)}{1 + F(z)G(z)} \tag{6}$$

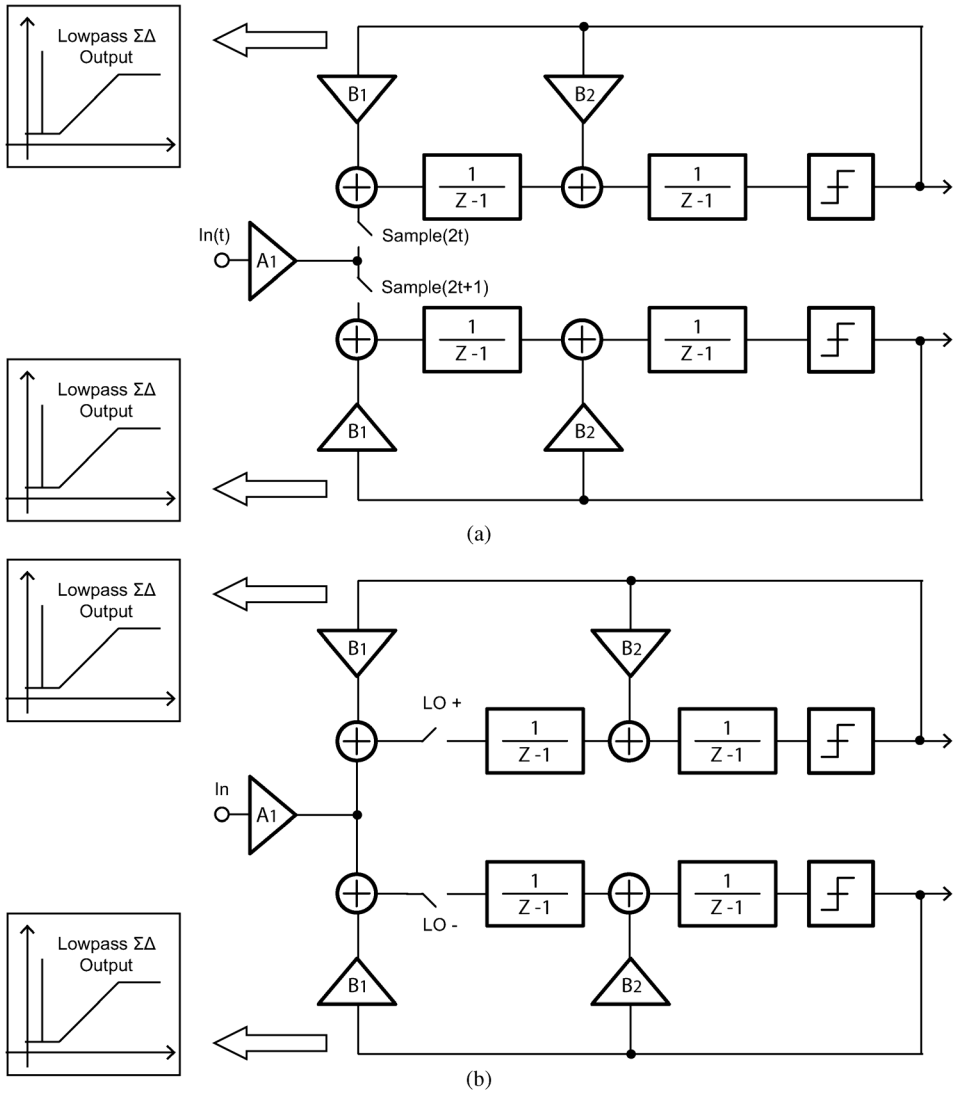

Fig. 2. Bandpass feedback created with two ΔΣ modulators. (a) Bandpass feedback created with out-of-loop interleaving sample. (b) Bandpass feedback created with inside-the-loop nonoverlapping mixture.

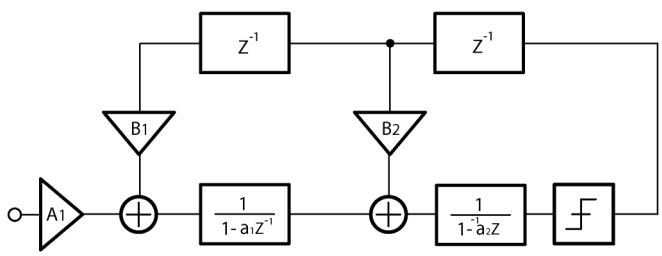

Fig. 3. Second-order CIFB ΔΣ loop filter.

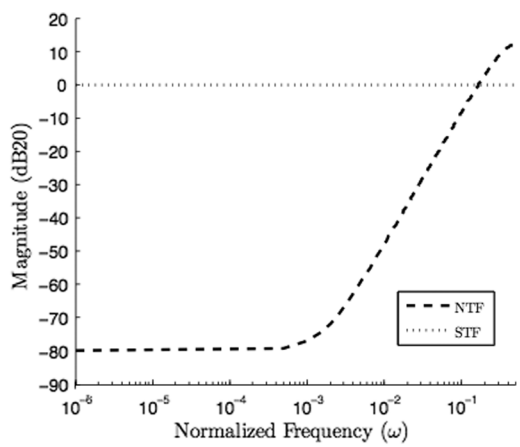

Fig. 4. Signal and noise transfer functions of a second-order modulator.

where $G(z)$ is the loop filter transfer function of the ΔΣ system as shown in Fig. 6. For the FIR filter in the DAC, we have

$$F(z) = \sum_{i=0}^{n} a z^{-i} = \frac{\sum_{i=0}^{n} a_i z^{n-i}}{z^n} \tag{7}$$

where a are the weighting factors for the taps in the FIR DAC. Most of the FIR DAC-based designs have a small number

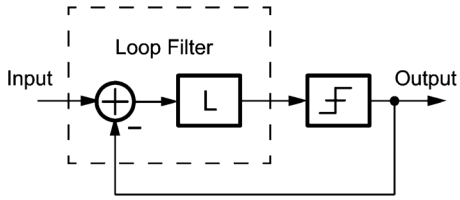

Fig. 5. Simplified $\Delta\Sigma$ block diagram.

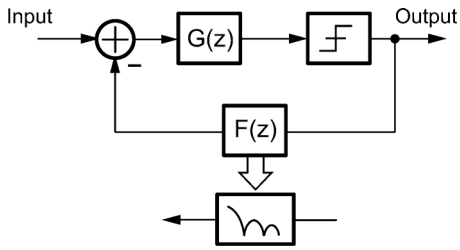

Fig. 6. Simplified loop filter model for FIR DAC.

of taps, usually from four to eight taps ([5], [8], [11]); therefore, (7) is quite manageable. In the frequency range where $F(z)G(z) \gg 1$, (5) reduces to $NTF(z) \approx 0$, and (6) yields

$$STF(z) \approx \frac{1}{F(z)}. \tag{8}$$

In general, $F(z)G(z) \gg 1$ at low frequency, since $NTF(z)$ should filter out most of the quantization noise at low frequencies. On the other hand, the STF would be flat if $F(z)$ is just a short, or, by (6), then

$$STF(z) \approx \frac{z^n}{\sum_{i=0}^{n} a_i z^{n-i}}. \tag{9}$$

Since $F(z)$ is an FIR function, it has nulls at different frequencies. By (6), these nulls result in STF peaking. The actual height of such peaks relates to the loop structure as well as the number of taps in the FIR filter. In [8] and [11], peaking levels higher than 10 dB have been reported with four-tap and eight-tap filters.

C. Jitter Sensitivity

Clock jitter is a major limiting factor in the performance of any high-speed $\Delta\Sigma$ ADC design. It has been reported in [12] that clock jitter perturbs the amount of feedback charge from the DAC and degrades the in-band SNR, but the actual mechanism by which clock jitter compromises the high-speed $\Delta\Sigma$ in-band performance has not been analyzed in detail.

The jitter sensitivity of high-speed $\Delta\Sigma$ systems is due to the nonlinear nature of the loop. A $\Delta\Sigma$ modulator can provide a dynamic range far exceeding the limit of its low-resolution quantizer. In the time domain, the $\Delta\Sigma$'s output is a pulse-density-modulated (PDM) bit sequence. The PDM nature of the bit sequence provides an additional dimension to encode data, so a $\Delta\Sigma$ ADC's dynamic range is not limited by its quantizer. When a low-resolution quantizer is used, the modulator has to modulate the output density more aggressively to maintain the same

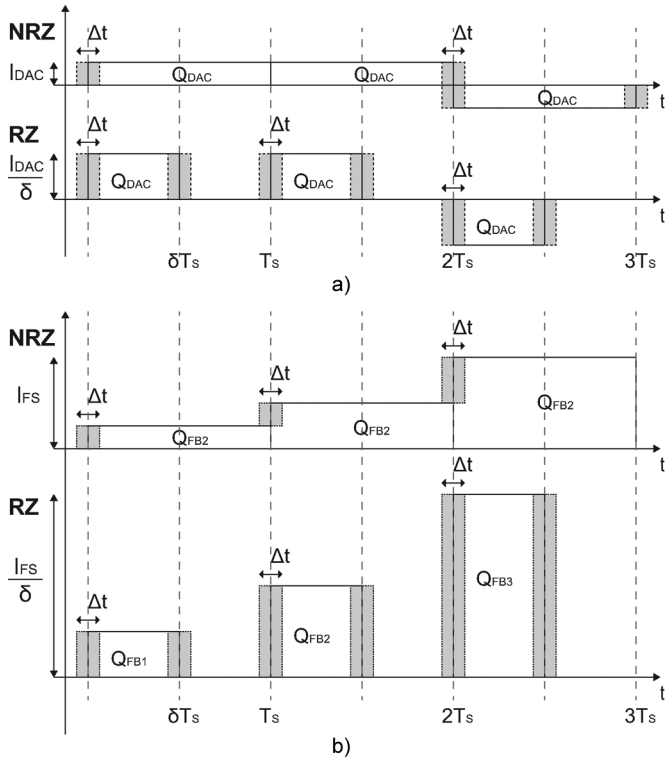

Fig. 7. Comparison of jitter impact on RZ and NRZ DACs. (a) Single-bit case. (b) Multibit case.

dynamic range as compared to the case of using a high resolution the quanziter. This results in more frequent switching between different levels in the output sequence. Clock jitter introduces noise every time there is a switching event in the output sequence. The more frequently the output switches, the more noise would be added, and then the in-band SNR suffers. Therefore, a quantizer with higher resolution is preferred for high-speed $\Delta\Sigma$ modulator designs.

1) Comparision of DAC Implementations: Common feedback DAC pulse shapes reported in literature can be summarized as nonreturn-to-zero (NRZ), return-to-zero (RZ), exponential, and half-sinusoid [13]. Even though raised-cosine DACs look promising [14], the complexity of these designs poses implementation challenges. A switched-capacitor DAC, which has an exponential pulse shape, is a popular choice for discrete-time $\Delta\Sigma$ ADC designs. To first order, the feedback charge is set by the reference voltage and the capacitor size, so it should not be affected by the clock jitter. In reality, due to slewing and settling, the system is still sensitive to clock jitter. Furthermore, since the SC DAC's feedback level is fixed by the reference voltage and capacitor sizes, the design lacks the flexibility to support a wide frequency range, making it less appealing for SDR. In comparison, the feedback charge of current DACs, such as RZ and NRZ DACs, can scale naturally with the clock frequency, thus enable a wide frequency range of operation. Therefore, RZ and NRZ DAC are the only suitable choice for such a design.

Reference [13] discusses how single-bit RZ and NRZ DACs are affected by timing uncertainties. Fig. 7 shows how clock jitter impacts the output pulses of RZ and NRZ DACs. Timing

uncertainties are modeled with a zero-mean random white noise process with a variance σ_j^2. As diagrammed in Fig. 7, clock jitter modulates the pulse width of the feedback signal, introducing a noise charge of a size of $I_{\mathrm{Feedback}}\Delta \mathrm{t}$. In the single-bit DAC case, the feedback current I_{Feedback} is the feedback DAC current I_{DAC}, while in the multi-bit case, I_{Feedback} is related to the feedback level resolved by the quantizer. One major difference between the RZ and NRZ designs is that the feedback current of the RZ DAC is larger than the NRZ DAC due to the fact that pulse width is narrower, as shown in Fig. 7. Therefore, RZ DACs are more sensitive to timing uncertainties, as more noise charge is injected than in the NRZ DAC case. Shown in Fig. 7(a), the noise charge in the RZ DAC has the same width as in the NRZ DAC case, but a factor of δ taller, therefore the noise charge is a factor of δ larger in the RZ DAC case. Also, the RZ DAC has worse jitter performance due to the extra transition edge in every cycle, thus reducing the dynamic range of the system by 3 dB [15].

Fig. 7(b) compares the effect of jitter on multibit RZ and NRZ DACs. Compared with single-bit DACs, the multi-bit DACs are less sensitive to jitter since, unlike single-bit DACs, they do not always operate at the full-scale range. The noise charge [Fig. 7(a) and (b)] still has the same width for the same amount of jitter. However, the height of the noise charge varies with the input signal statistics. As the number of DAC output levels is increased, it will operate with less likelihood, at the full-scale output, so the lower noise charge would be dumped into the integrators. In summary, more levels in the DAC reduce the jitter sensitivity.

2) Jitter Analysis and Simulation Models: The jitter sensitivity of ΔΣ ADCs with single-bit feedback DACs has been studied in the literature in the past. References [12] and [16] offer derivations of jitter sensitivity for ΔΣ systems with single-bit DACs for both the RZ and NRZ cases. With some modification on [16], the SNRs for a multi-bit NRZ and RZ DAC can be written as

$$\mathrm{SNR}_{\mathrm{NRZ}} \approx 10\log_{10}\left[\frac{\mathrm{OSR}}{\left(\frac{\sigma_j}{T}\right)^2}\left(\frac{A}{P_{yd}}\right)^2\right] \tag{10}$$

$$\mathrm{SNR}_{RZ} \approx 10\log_{10}\left[\frac{\mathrm{OSR}}{\left(\frac{\sigma_j}{T}\right)^2}\left(\frac{A}{P_{y}}\right)^2\right] \tag{11}$$

where A is the amplitude for a sinusoidal input and $Py = \sqrt{2}E[y[n]y[n+k]]$, which is the power in the modulator's output sequence. The P_y in the RZ case and P_{yd} in the NRZ case can be extracted from behavioral simulations. Fig. 8 lists different values of P_y and P_{yd} for a second-order ΔΣ modulator, assuming 1 ps rms jitter for a 2 GHz clock. The numbers from Fig. 8 are then substituted into (10) and (11) to calculate the effective SNR, as summarized in Fig. 9. Based on simulation and previous measurement results [18], 1 ps rms jitter roughly corresponds to 60 dB SNR.

From Fig. 9, one difference between the RZ DAC and the NRZ DAC is that, at a higher number of levels, the improvement of the RZ DAC saturates, while the NRZ DAC's SNR keeps increasing. As shown in Fig. 7, the NRZ DAC's output waveform smoothes out as more levels are introduced. In theory, when the NRZ DAC approaches infinite resolution, the output waveform approaches a sine wave for a sinusoidal input. The difference between DAC levels from adjacent cycles would be reduced, thus reducing the jitter induced noise charge as well. In reality, implementing a linear DAC with resolution beyond 3 bits comes with substantial design challenges as well as a large power and area penalty.

Number of Levels	P_y RZ DAC	P_{yd} NRZ DAC
2	0.5000	0.6584
3	0.3628	0.3574
4	0.3250	0.2429
8	0.2950	0.0983

Fig. 8. Comparison of P_y P_{yd} on different levels of DAC.

Number of Levels	RZ DAC	NRZ DAC
2	Ref.	0.6 dB
3	2.8 dB	5.9 dB
4	3.7 dB	9.3 dB
8	4.6 dB	17.1 dB

Fig. 9. SNR comparison between RZ and NRZ DACs with different DAC levels.

For the RZ DAC, the improvement in SNR saturates because the increasing the number of levels doesn't help reduce the step size. The RZ DAC has transitions as large as the output full-scale of the DAC, so the noise charge induced would not scale as nicely as in the NRZ DAC case. For this implementation, SNR saturates roughly at the 2 bit level, as summarized in Fig. 9.

D. Current-Mode-Integration Mixing/Sampling

This design, similar to [4], relies on current-mode integration sampling (CMIS) [17] to provide frequency translation within the loop. A graphical representation of sampling is shown in Fig. 10. In the time domain [Fig. 10(a)], the input signal is multiplied with an impulse train $s(t)$, which translates to a convolution between the input signal and the impulse train in the frequency domain, as shown in Fig. 10(b). The results are shown in Fig. 11. Because of aliasing, the signal, dc offset and blockers at harmonics of the carrier frequency fold down to baseband. In practical cases, the desired signal cannot be resolved properly.

Fig. 12 shows simplified models of the input signal mixed with a square-wave clock with a 50% duty cycle. The sinc filter in Fig. 12 is due to the square shape of the clock. For a clock with 50% duty cycle, this sinc filter nulls out the even-order harmonic contents of the clock frequency. Note that in Fig. 12(a) $a_0 = 0$. This is due to the fact that most of mixer circuit designs employ differential structures, that help to reject common-mode noise or DC offsets. The mixing process is illustrated in Fig. 13. The additional sinc filter rejects contents at the even-order harmonics, and attenuates the odd-order harmonics except for the one at DC. It can be shown that the attenuation at ω_s is $2/\pi$, which is commonly described as the conversion loss. Fig. 13 also exposes that the fact that the scheme is susceptible to higher

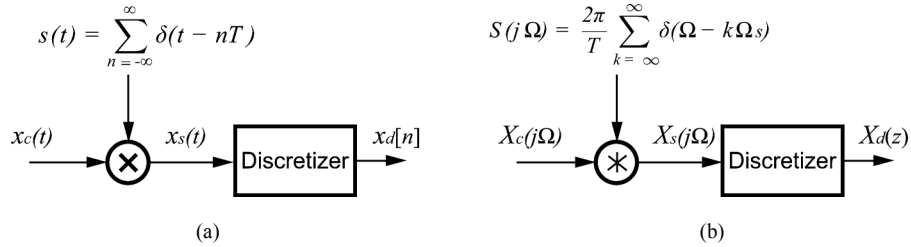

Fig. 10. Equivalent sampling model in the (a) time domain and (b) frequency domain.

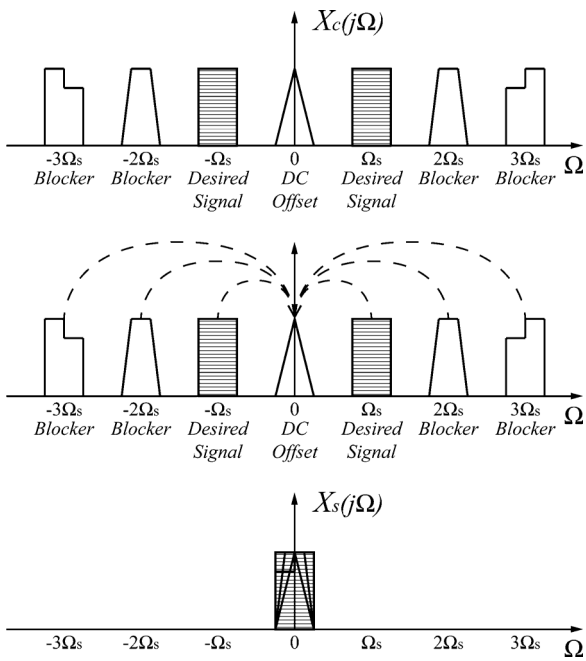

Fig. 11. Effect in the frequency domain of using sampling to downconvert the RF signal.

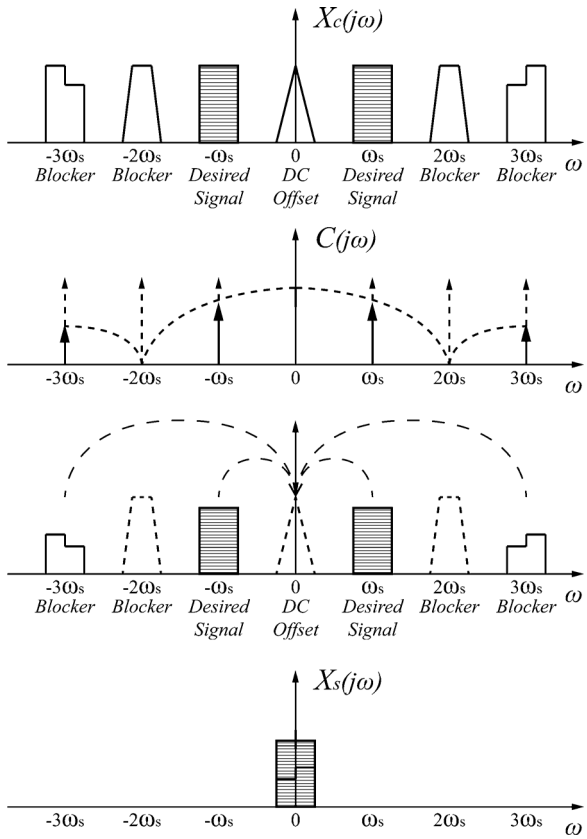

Fig. 13. Effect in the frequency domain of using mixing to downconvert the RF signal.

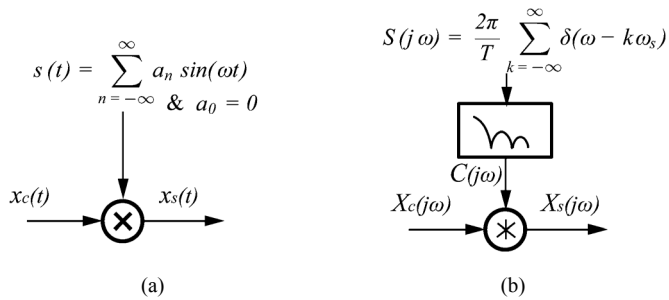

Fig. 12. Equivalent mixing model in the (a) time domain and (b) frequency domain.

order odd harmonics, such as the third-order harmonic shown here, when mixing with a 50% duty-cycle clock.

Current-mode integration sampling (CMIS) behaves like mixing [18]. Consider the CMI sampler shown in Fig. 14. Instead of capturing the instantaneous voltage at the moment that switch M1 turns off, capacitor C_H integrates the input current over a period of time set by the LO. It can then be shown [18] that

$$q_{\text{in}}[n] = \frac{T_{\text{LO}}}{2} \int_{\infty}^{nT_{\text{LO}}+\frac{T_{\text{LO}}}{2}} I_{\text{RF}}(\tau) p\left(\left(nT_{\text{LO}}+\frac{T_{LO}}{2}\right)-\tau\right) d\tau \tag{12}$$

where $p(x) = T_{\text{LO}}/2$ for $0 \le t \le 2/T_{\text{LO}}$ and $p(x) = 0$ elsewhere. T_{LO} is the integration period.

Fig. 15 gives a graphical representation of the above equation. While a sinc filter is in the clock path in the mixing case, as shown in Fig. 12(b), CMIS has a sinc filter in the signal path as shown in Fig. 15. Therefore, for an LO clock with the same 50% duty cycle, the final outputs from mixing and CMIS is identical for the reasoning shown in Fig. 13. Also, the dc offset in the case

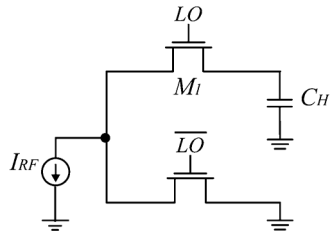

Fig. 14. Current-mode integration sampler with single-ended output.

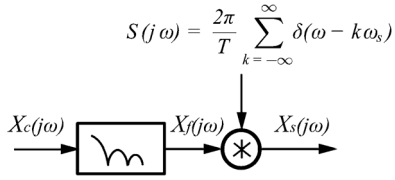

Fig. 15. Effect in the frequency domain of using mixing to downconvert the RF signal.

of CMIS can be rejected by a differential implementation. CMIS is also susceptible to high-order odd harmonics as a mixer.

E. System Summary

A four-channel second-order ΔΣ ADC with a CIFB all-feedback loop structure has been chosen for this work in order to achieve a maximally flat STF response and flexibility to support a wide frequency range. Also, a 2-bit NRZ DAC is selected for better jitter immunity and lower power consumption as compared to higher resolution options. Finally, discrete-time ΔΣ ADCs are implemented as in [4] employing CMIS mixers. The discrete-time design allows the CMIS mixers to be seamlessly integrated and helps to reduce the complexity for a system intended to operate over a wide range of frequency.

III. Implementation

The overall architecture of the receiver is shown in Fig. 16. For the sake of clarity, the system diagram is shown as single-ended, while the actual design is fully differential. The receiver includes both I and Q channels. A low-noise transconductance amplifier (LNTA) in each channel converts the input RF voltage into an output RF current. A programmable gain of 20 dB is implemented by changing the bias current in both the LNTA and the feedback DACs. As shown in Fig. 16, the output of the LNTA is then split into two interleaved paths for I and Q channels, each of which contains a pair of passive mixers implemented as a pair of CMIS switches. The signal is then processed by a second-order loop filter implemented using a passive switched-capacitor network. A two-bit quantizer digitizes the filtered signal, and its output is fed back to the RF summing node. With two channels of ADC's RF feedback signal, an effective bandpass feedback is created at the summing node. This multibit bandpass feedback suppresses the RF voltage swing; consequently, it improves linearity performance. Compared with [4], the two-bit network reduces the RF swing by a factor of three. However, due to the lack of front-end gain, the reduced swing poses challenges for the comparator design, which is discussed later in this section. The system requires a single external clock operating at twice the speed of the carrier frequency. All of the necessary clock phases are then generated internally.

A. Sub-Channel Design

A detailed schematic of the I channel is shown in Fig. 17. Two channels of interleaved ΔΣ ADCs create a bandpass ΔΣ feedback on the RF summing junction. The high output impedance of the LNTA forces the output current to flow through the mixer, switched with an externally supplied f_{LO}. When the LO signal is high, the output current from the LNTA charges a pair of capacitors $(C1a, C1b)$ in the top path. When the LO signal is low, these capacitors are isolated from the input, and the signal is held constant. This two-path scheme indirectly implements a sample-and-hold function for the subsequent switched-capacitor circuits. The sample-and-hold feature of the mixer limits the jitter sensitivity to the LOs rising edge only; however, the feedback DAC implementation does impact the SNDR of the receiver. $C1a$ and $C1b$ are chosen to be 5 pF to trade off linearity, noise, and power, as discussed in [18].

B. LNTA

Fig. 18 illustrates the design of the front-end LNTA. A class-AB dual common-gate (CG) amplifier provides both wideband input matching and good linearity. To improve both noise performance and power efficiency, the g_m of the four tail current sources are reused by ac-coupling the RF input signal to their respective gates. The input common-mode voltage is set by two replica biases that mimic the biasing conditions of the NMOS CG and the PMOS CG. The LNTA's differential outputs are ac-coupled to the mixer switches, and the output common-mode voltage is set by a common-mode feedback amplifier connected to the mixers. The LNTA provides a transconductance gain up to 20 dB from a 1.5 V supply with the CMIS circuits. The key feature is that the entire system is in current mode operation. All of the internal nodes are at low impedance (enforced by the cascode devices); however, the output nodes are not, but voltage swing at those nodes are suppressed by the low impedence from the global ΔΣ loop.

C. Feedback DAC Designs

A two-bit NRZ DAC is implemented to favorably trade off jitter immunity with power consumption. The NRZ DAC (Fig. 19) operates in two phases, LO_D and $\overline{LO\_D}$, derived from the LO. In the first phase, when the mixer switches are on, the feedback DAC is connected to the RF side of the mixer, suppressing the voltage swing at the LNTA and the mixer switches. During the second phase, the switches are off, and the DAC is connected to the baseband (BB) side of the switches, thus preserving the DACs NRZ feature. This scheme is sensitive to the clock jitter during the switching instances at RF side only (or the rising edge of the LO_D), since the timing uncertainties of the switching instance to the BB side does not change the duration of the feedback DAC pulse.

Intersample interference (ISI) is one major issue for the design of the NRZ DAC. As noted in [20], ISI is the result of asymmetry between the positive and negative feedback pulses of an

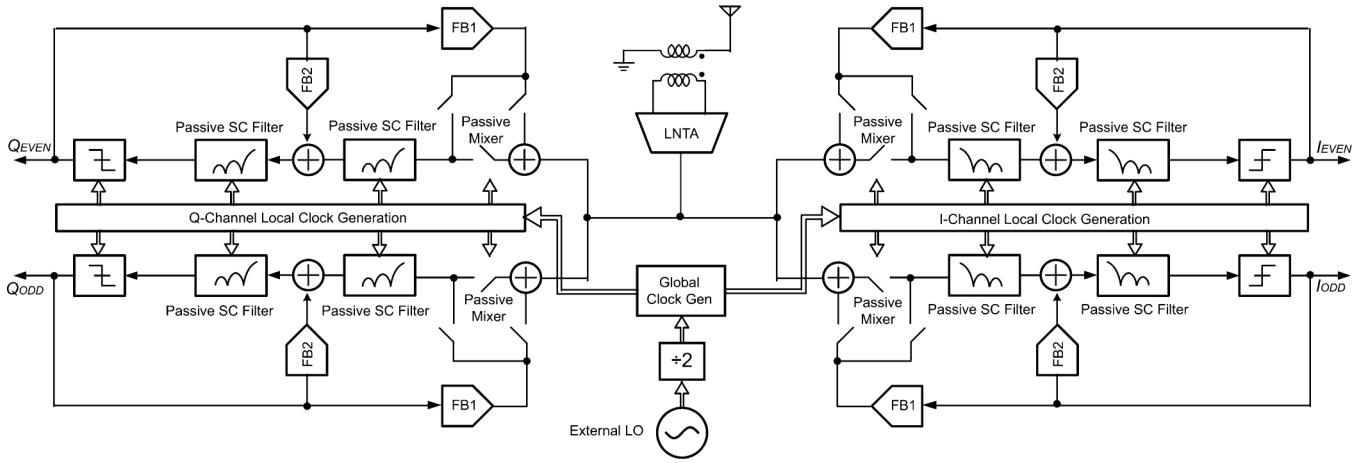

Fig. 16. Simplified block diagram of the receiver.

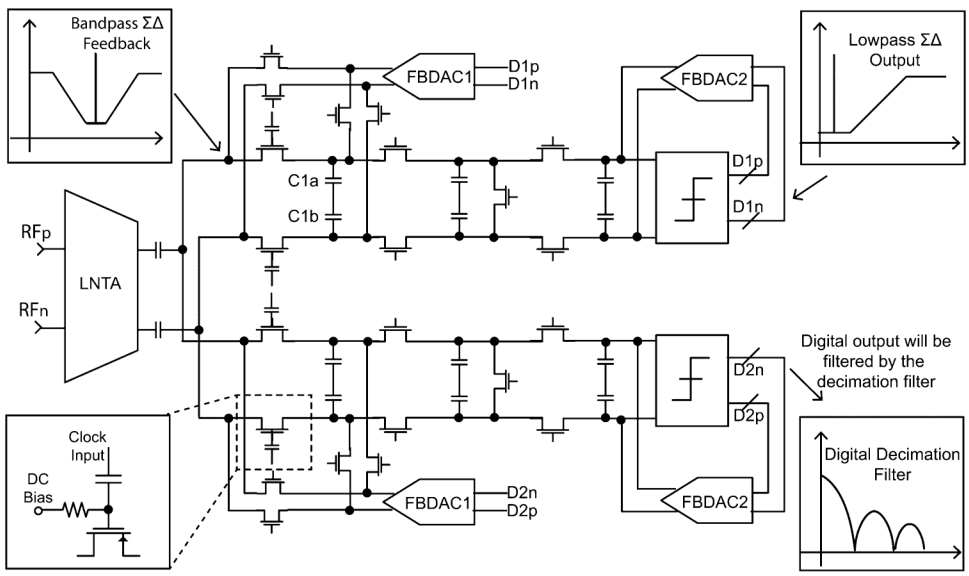

Fig. 17. Simplified schematic of the I channel.

NRZ DAC, which is caused by different transition times when switching from the positive to the negative reference and vice versa [20]. Waveform asymmetry can be reduced by sharper transitions and matching of the transition edges, or switching to an RZ DAC design. Due to the jitter sensitivity issue, an RZ DAC design is not a feasible choice. In this design, a pair of fast-switching complementary DFFs are applied within the DAC unit cell to retime the quantizer outputs as shown in Fig. 19. The DAC is switching with a slightly delayed clock, LO_D, to avoid leaking of the output into the wrong channels. The PMOS retiming DFF is precharged high when LO_D is low and transparent when LO_D is high, while the NMOS retiming DFF operates in the opposite way. For the switches connected to the RF terminal, the quantizer output is directly latched by the complementary DFFs. For the switches connected to the BB side, the digital output is first stored by another simple DFF, and then this stored value is supplied to a second pair of retiming DFFs which are ready to drive the DAC on the rising edge of $\overline{LO\_D}$.

Another issue associated with the DAC design, as suggested by [18], is the effect of limited output impedance. Finite output impedance in the feedback DAC would result in second order distortion since it creates a signal-dependent discharge path. In [18], a behavioral model including the effect of finite DAC output resistance is proposed and shown here as Fig. 20. β_{DAC} in Fig. 20 can be derived as [18]

$$\beta_{\mathrm{DAC}} = 1 - exp\left(\frac{-T_{ref}}{C_{H1}R_{\mathrm{DAC}}}\right). \tag{13}$$

Simulation suggests that the DAC impedance has to be larger than 10 kΩ to ensure the second-order tone induced is always below −80 dBc. The DAC unit cell is shown in Fig. 19. To ensure voltage headroom for all of the devices stacked in the unit cell and, hence, to maintain the desired high output impedance of the DAC, it is connected to the 1.5 V supply. All current source devices are sized appropriately for the required mismatch performance, and they are further source-degenerated for better matching and noise performance, as in [21]. The second feedback DAC design is less critical, since the jitter there is noise-shaped by the first integrator. Hence, it is implemented as an RZ DAC.

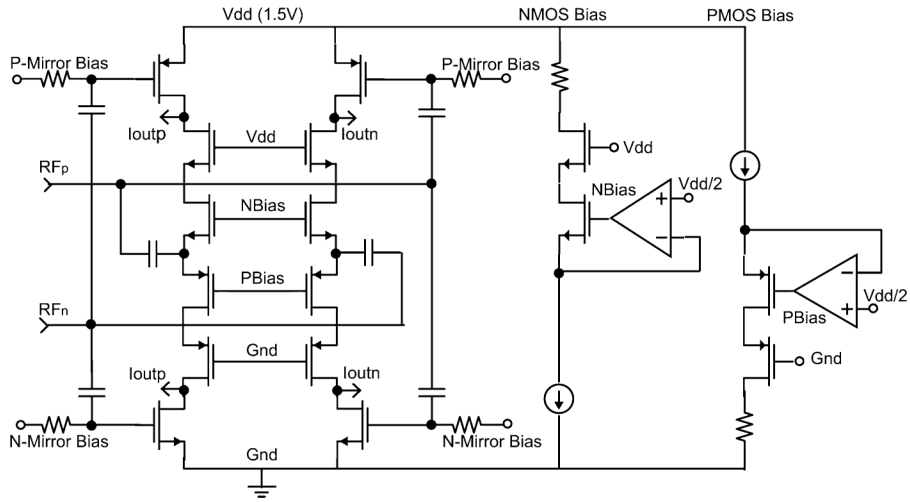

Fig. 18. Low-noise transconductance front-end with biasing.

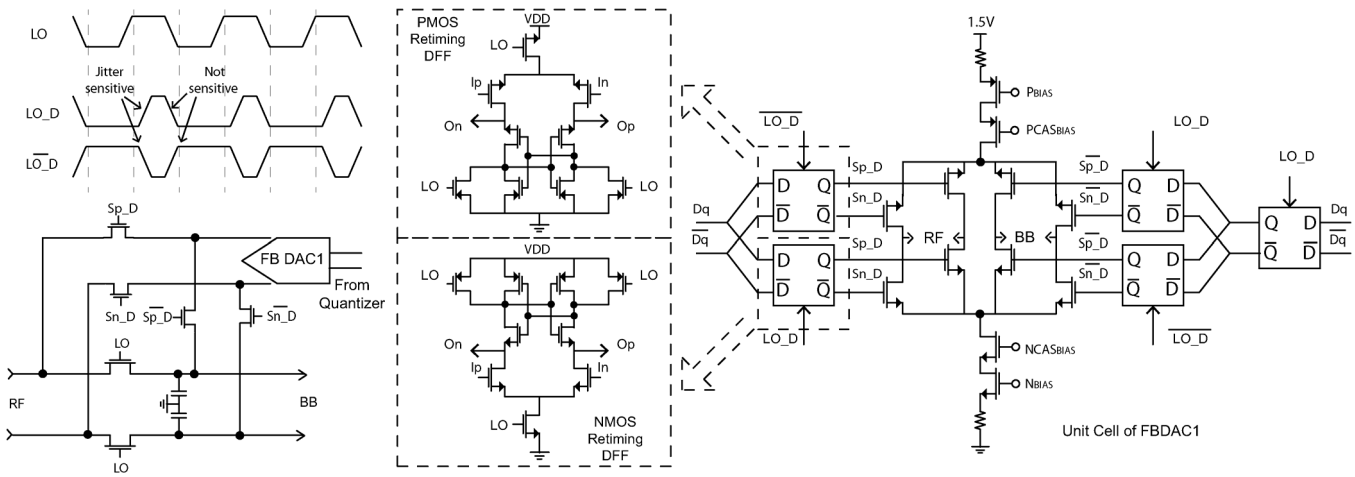

Fig. 19. Detail schematic and clocking scheme for FBDAC1.

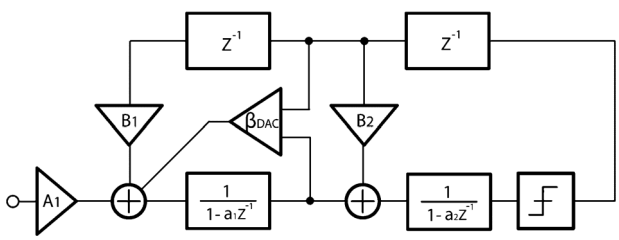

Fig. 20. System model including the effects of feedback DAC finite output resistance.

D. Comparators

The comparator design is challenging due to its speed and precision requirements. The comparator requires a short decision time (<200 ps), a small input-referred noise level (200 μV), and low power consumption. Shown in Fig. 21, the comparator core is implemented using a calibrated pre-amplifier followed by a sense-amplifier-based latch. The pre-amplifier helps to ease the stringent input-referred noise and mismatch requirements (0.5 mV) posed on the comparator due to the lack of front-end gain in the system. The mismatch of the core comparators is further suppressed through an integrated calibration DAC to avoid using excessively large devices. The calibration procedure begins by taking all comparators offline and connecting them to an on-chip reference ladder. Then, the optimum code for each comparator can be obtained by sweeping through its cal-DAC. Finally, the comparators are connected back to the loop. This is a one-time process and is robust over a wide range of frequency.

To reduce the jitter sensitivity, more feedback levels are preferable. However, this poses a more stringent requirement on the comparators' mismatch performance. Fig. 22(a) compares the quantizer area with respect to the resolution in the quantizer. To meet the mismatch requirement, the comparators need to be large in conventional design. With calibration, the quantizer can be four times smaller. The area breakdown of a calibrated quantizer is shown in Fig. 22(b). At the 1-bit level, the size of the decoder dominates. At higher resolutions, the area of the cal-DAC dominates. At the 2-bit level, the decoder and the cal-DAC are of comparable sizes. It is worth noting that a 3-bit quantizer has a size that is ten times larger than that of a 2-bit design. For the current design, the quantizer occupies around 10% of the overall area. If a 3-bit design is

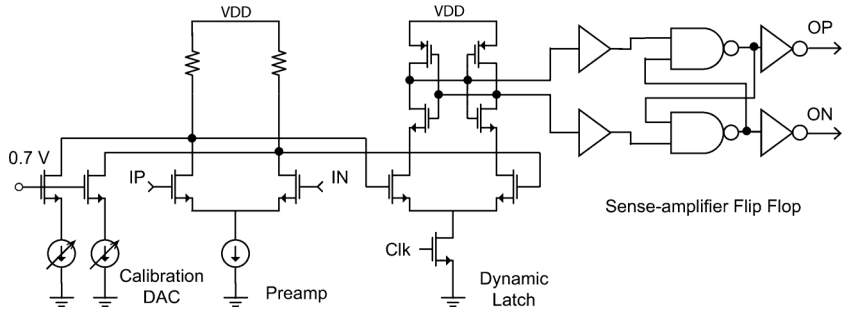

Fig. 21. Simplified schematic of the quantizer design.

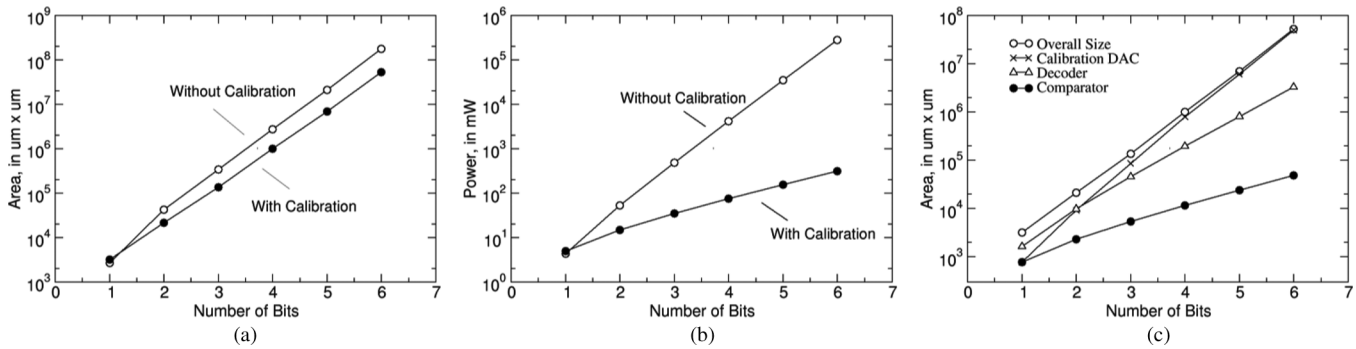

Fig. 22. Quantizer power and area comparision between calibration and no calibration.

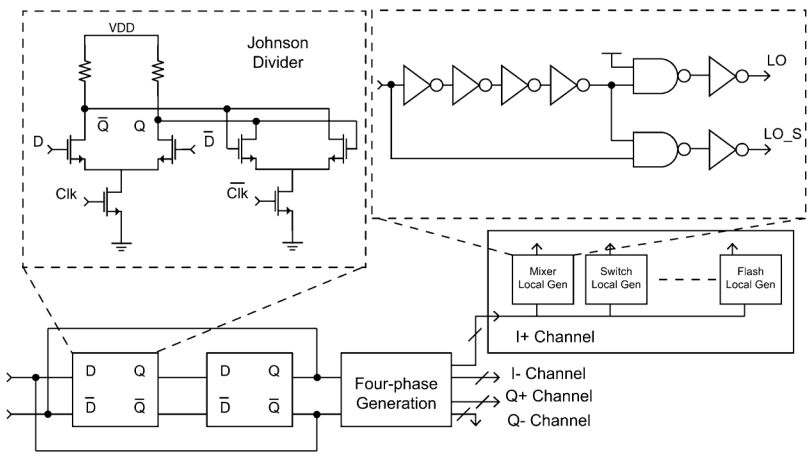

Fig. 23. Simplified clock generation and distribution scheme.

adopted, the quantizer would be similar in size to the current system. Another benefit of calibration is power savings as shown in Fig. 22(c). Without calibration, as the resolution is increased, each comparator scales up exponentially in size to meet the mismatch requirements. Meanwhile, more unit cells are needed. Hence, the switching power increases rapidly. With calibration, more cells are still needed, but each cell stays the same size; only the size of the cal-DAC increases. Therefore, the power overhead is less severe.

E. LO Generation and Distribution

As shown in Fig. 23, an external clock operating at twice the carrier frequency is fed to the chip. An on-chip global clock generation circuit brings down the clock speed to the carrier clock frequency and generates four phases of I/Q clocks. These I/Q clocks are then fed to the local clock generation circuit to generate all the needed clock phases, such as the mixer and DAC clock phases shown in the Fig. 23.

The LO network degrades the system noise floor through two mechanisms: its thermal noise and its flicker noise contributions. In [22], the jitter due to the thermal noise of a buffer is described as

$$\sigma_{dn}^2 = \left(\frac{4kT\gamma\tau_{\rm delay}}{I_{\rm discharge}V_{\rm overdrive}}\right). \tag{14}$$

Therefore, a larger $I_{\rm discharge}$ and a smaller $\tau_{\rm delay}$, which equate to having a faster edge rate, help to reduce thermal-induced jitter. The effect of flicker noise is discussed in Section IV. A larger device has faster edge rate and lower flicker noise, but It comes with large power penalty. For this

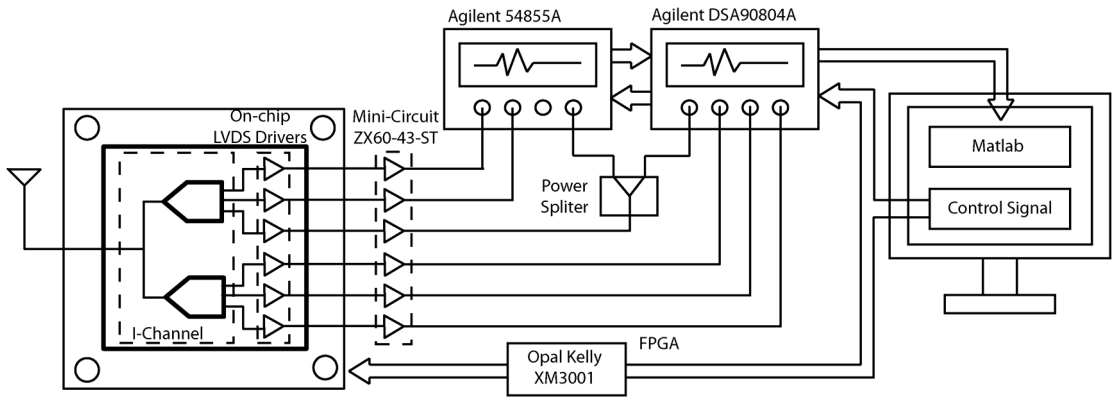

Fig. 25. Measurement setup for data capturing and system control.

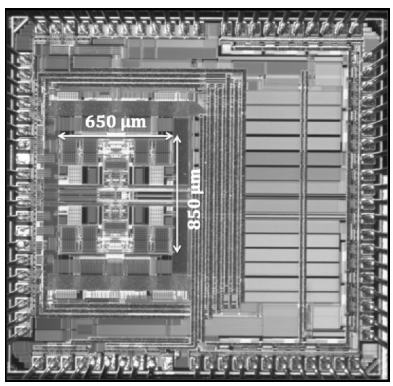

Fig. 24. Photomicrograph of the receiver.

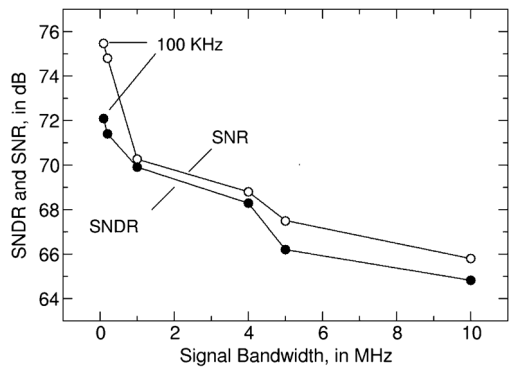

Fig. 27. Measured SNR and SNDR at 2 GHz carrier frequency.

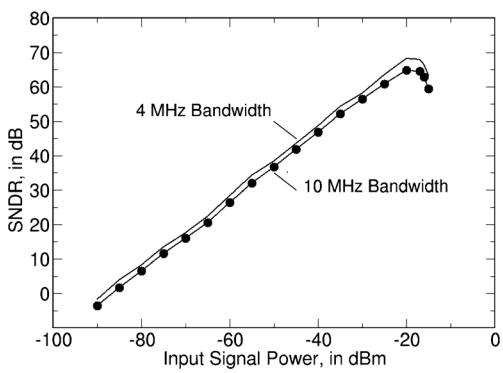

Fig. 26. Measured SNDR at 2 GHz carrier frequency.

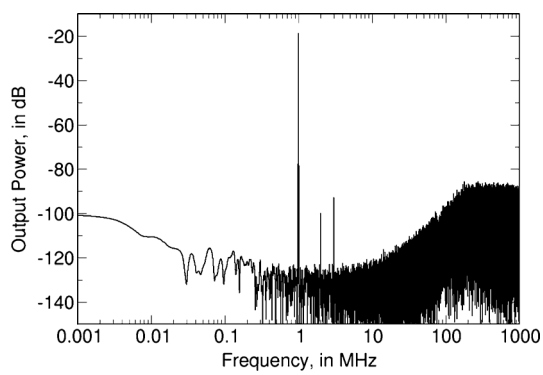

Fig. 28. Output spectrum at 2 GHz center frequency with input signal 1 MHz offset from the carrier.

design, the LO chain introduces 920 fs added jitter with 9 mW at 2 GHz operation.

IV. Measurement

The chip is implemented in TSMC's 65 nm GP technology. The chip microphotograph is shown in Fig. 24, highlighting that the receiver occupies an area of 850 μm $\times$ 650 μm, including the calibration DACs for the comparators as well as the local bypass capacitance. Fig. 25 shows the measurement setup for capturing data. Two real-time 20 GS/s oscilloscopes are used to capture the output digital waveforms, and post processing is performed on a computer. One channel is sent to two scopes to act as the trigger signal and synchronize the signals captured from the two scopes.

Fig. 26 shows the measured SNDR for 4 MHz and 10 MHz signal bandwidths at 2 GHz. The peak SNDR is 68.86 dB for 4 MHz and 64.83 dB for 10 MHz. The in-band P1 dB is at -15 dBm input level. The SNDR is higher than 60 dB over the 0.4 GHz to 4 GHz tuning range. Fig. 27 shows the SNR and SNDR for varying signal bandwidths at a 2 GHz center frequency. SNR and SNDR spectra are integrated from 10 kHz to the bandwidth mentioned. Fig. 28 shows the output spectrum for a 2 GHz frequency with an input signal at 2.001 GHz. The low frequency noise floor is elevated due to the reciprocal mixing of

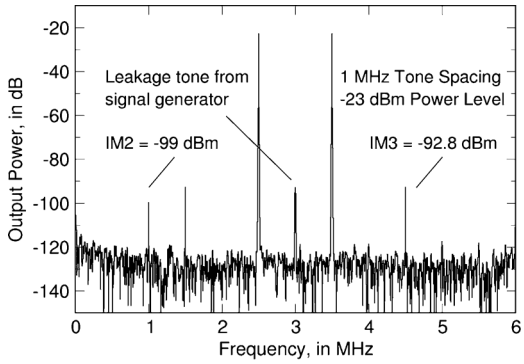

Fig. 29. Two tone tests with 1 MHz tone spacing around 2 GHz center frequency.

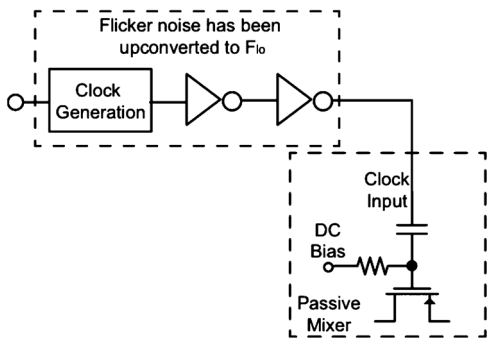

Fig. 30. Flicker noise from LO chain upconversion and downconversion.

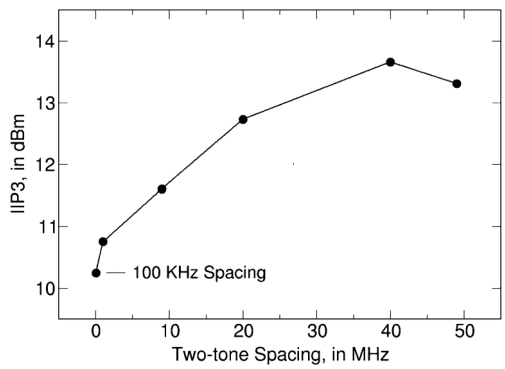

Fig. 31. IIP3 versus two-tone spacings at 2 GHz.

the LO phase noise by the mixer. A closer look at Fig. 28 reveals that there are two mechanisms that contribute to the noise floor in the above measurement. All of the transistors in the clock generation circuitry contribute flicker noise. As shown in Fig. 30, this low-frequency flicker noise is first up-converted to the LO frequency by the LO chain. Then, it is down-converted back to baseband by the CMIS mixers, which results in a rise in the noise floor at the low frequency. On the other hand, the noise floor at the higher frequencies is dominated by the jitter injected through the first feedback DAC. The clock jitter for this system is limited by its LO network: The clock source has a jitter of 290 fs, while the added jitter from the LO chain is around 900 fs. Therefore, this system would achieve (+10 dB) better SNR for narrow band standards, such as GSM, when operating in a low-IF mode.

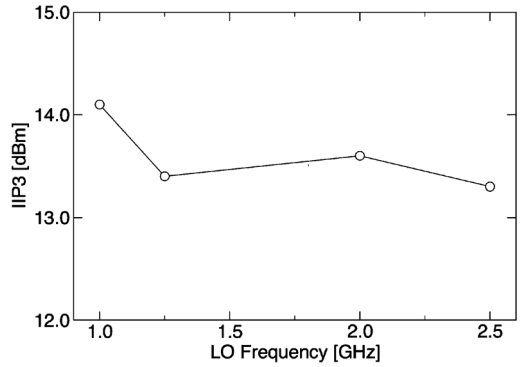

Fig. 32. IIP3 over different frequencies.

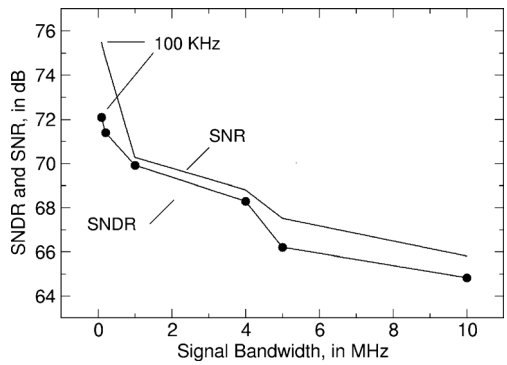

Fig. 33. SNR, SNDR vs. signal bandwidth.

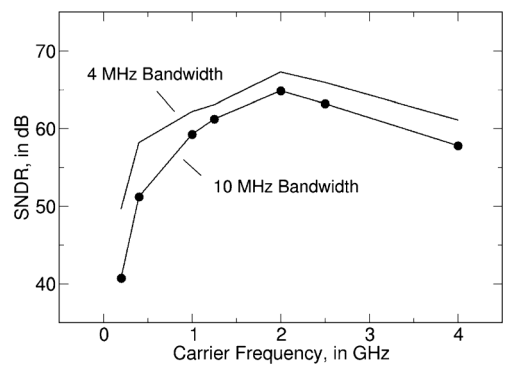

Fig. 34. SNDR versus carrier frequency.

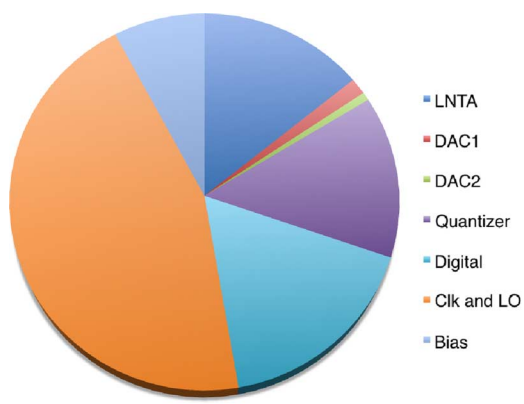

Fig. 35. Power breakdown.

Fig. 29 shows the two tone test result. One Agilent 4438C vector signal generator (VSG) is used to generate the two tones with different spacings. A leakage tone is generated by the VSG in the middle of the two desired signals. The measured IM2 and IM3 products are −99 dBm and −92.8 dBm respectively.

	[4]	[24]	[5]	[25]	[26]	[27]	[28]	[29]	This work
Architecture	ΔΣ Modulator	Bandpass ΔΣ	Lowpass ΔΣ	Bandpass ΔΣ	Bandpass ΔΣ	RX AFE	Bandpass ΔΣ RX	Downconvert ΔΣ RX	RF-Digital ΔΣ
RF Freq. [GHz]	0.4-1.7	0.8-2	0.9	0.95	2.4	0.4-6	0-1, 2-4	0.7-2.7	0.4-4
SNDR (dB)[1]	60	50-44[2]	56	59[2]	48	N/A	90 (SNR)	44	4 MHz: 68-60 10 MHz: 65-52
IB-IIP3 (dBm)	+19	-5 / -7	-12	N/A	-9	+6	+8	N/A	+10
OB-IIP3 (dBm)	+19	N/A	+4	N/A	N/A	+10	+8	-2	+13.5
Sentivity (dBm)[3]	N/A	-75[3]	6.2 dB NF	-77[3]	N/A	3 dB NF	-97 7 dB NF	5.9-8.8 dB NF	-88 16 dB NF[4]
Power (mW)	50.4	30	80	75	40	30-55	1000	90	40.3[5] (17-70.5)
Area (mm^2)	0.8	2.3	1.2	1.36	0.8	2	5.5	1.1	0.56
Supply (V)	1.2	1.2	1.2	1.25	1.0	1.2	1.1/2.5	1.0	1.1/1.5
Technology	90 nm CMOS	0.13 μm CMOS	65 nm CMOS	0.25 μm BiCMOS	90 nm CMOS	40 nm CMOS	65 nm CMOS	40 nm CMOS	65 nm CMOS

[1] SNDR is normalized for 10 MHz bandwidth.
[2] Reported SNDR is only for 1 MHz bandwidth.
[3] Sensitivity is measured and reported for 10 MHz bandwidth except for [24] and [25], which are measured at 1 MHz Bandwidth.
[4] Noise figure = Dynamic range + LNTA Gain – Thermal noise floor integrated over 10 MHz = 68 dB + 20 dB – (-174 dBm/Hz + 70) = 16 dB
[5] 40.3 mW is measured at 2 GHz, including the divider power. System consumes 17 mW at 400 MHz and 70.5 mW at 4 GHz of operation respectively.

Fig. 36. Comparison table.

Fig. 31 summarizes the IIP3 performance versus tone spacing. The IIP3 improves with farther spacing between the two tones, since the CMIS network functions in a similar manner to that of the N-path filter proposed in [23]. Fig. 32 shows IIP3 for a 40 MHz tone spacing over different frequencies. Overall, the system maintains its high linearity over a wide range of blocker frequencies.

Fig. 33 shows the SNR and SNDR for varying signal bandwidths at a 2 GHz center frequency. SNR and SNDR spectra are integrated from 10 kHz up. For narrow bandwidth standards, such as GSM, the SNR is severely impacted by the low-frequency noise increase. Therefore, it performs better in low-IF conversion. For wider bandwidth standards, the clock jitter noise sets the dynamic range of the system, which is why a multi-level feedback is used here. Overall, a large SNDR is maintained over a large range. Fig. 34 shows the SNDR performance as the carrier frequency varied from 200 MHz to 4 GHz. The frequency resolution of the plot is limited by the sampling rate of the oscilloscope. At low frequencies, the SNDR improves substantially with an increase in carrier frequency, as the in-band noise is dominated by the quantization noise. At higher frequencies, this improvement is offset by the increasing impact of the clock jitter. The clock jitter eventually dominates, so further oversampling only degrades the SNDR.

Finally, Fig. 35 shows the power breakdown of the system. Fig. 36 lists the performance summary and comparison other state-of-the-art designs. The proposed receiver is able to achieve the widest tuning range among all of the ΔΣ systems. Even compared to a more traditional design, its tuning range is comparable. The receiver's linearity performance (both in-band and out-of-band) is also in line with other state-of-art designs. The noise figure of the system is limited by the clock jitter injected from the first feedback DAC. Compared to [28], [29], this system consumes much less power since it avoids the use of active resonators. By avoiding bulky passives, this design achieves the smallest reported area among all.

V. Conclusion

This paper presents a novel ΔΣ ADC-based receiver design that supports a frequency of operation from 400 MHz to 4000 MHz, which covers all worldwide LTE bands. An NRZ feedback DAC design reduces the jitter sensitivity of the system and aids in achieving a high SNDR over the frequency range of interest. It provides a large dynamic range with a low power consumption. It meets the three major criteria of the SDR systems. Without any bulky passives, the design maintains its small footprint, while digitally oriented design methodology enables a truly flexible receiver that is able to adapt to different standards with change of a couple of control bits. Finally, the solution can scale naturally with technology.

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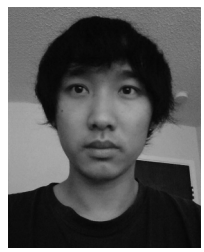

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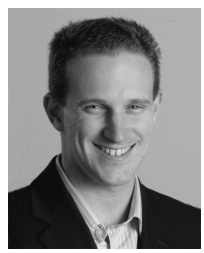

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