A 2.8 GS/s 44.6 mW Time-Interleaved ADC Achieving 50.9 dB SNDR and 3 dB Effective Resolution Bandwidth of 1.5 GHz in 65 nm CMOS

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***Abstract*—This paper presents a power- and area-efficient 24-way time-interleaved successive-approximation-register (SAR) analog-to-digital converter (ADC) that achieves 2.8 GS/s and 8.1 ENOB in 65 nm CMOS. To minimize the power and the area, the capacitors in the capacitive DAC are sized to meet the thermal noise requirements rather than the matching requirements, leading to the LSB capacitance of 50 aF. An on-chip digital background calibration is used to calibrate the capacitor mismatches in individual ADC channels, as well as the inter-channel offset, gain and timing mismatches. Measurement results at the 2.8 GS/s sampling rate show that the ADC chip prototype consumes 44.6 mW of power from a 1.2 V supply while achieving peak SNDR of 50.9 dB and retaining SNDR higher than 48.2 dB across the entire first Nyquist zone with a $1.8\mathrm{V_{pp\text{-}diff}}$ input signal. The prototype chip occupies an area of $1.03 \times 1.66\ \mathrm{mm^2}$, including the pads and the testing circuits. The figure of merit (FoM) of this ADC, calculated with the minimum SNDR in the first Nyquist zone, is 76 fJ/conversion-step.**

***Index Terms*—A/D, ADC, background, calibration, CMOS, converters, linearity, SAR, time-interleaved, timing.**

I. Introduction

ADVANCES in resolution, bandwidth and energy efficiency of analog-to-digital converters (ADCs) have enabled continued migration of signal processing and communications algorithms to the digital domain. Yet, new applications, with higher bandwidth and resolution requirements, require further advances in data conversion. An example of an application that brings the A/D conversion close to the front-end are the direct-sampling TV receivers, which implement the entire filtering in the digital domain [1]. Local- and personal-area communications in the 60 GHz band are receiving a lot of attention for their promise of delivering very high datarates [2]. Both of these example applications require ADCs with the sample rate greater than 2.5 GHz and a resolution of around 8 effective bits. However, the energy efficiencies of the ADCs that satisfy these specifications [1], [3] significantly lag behind those that sample in the 100 MHz range [4]–[8].

Time-interleaved converter arrays, first introduced in [9], have a long history in achieving extremely high sampling rates that cannot be achieved by any other ADC architecture [10]–[14]. More recently, the time-interleaved ADCs have been used to improve the energy efficiency at the speeds that have traditionally been dominated by the flash and folding-interpolating architectures, such as [3] and [15]. Time-interleaving of 16 two-step SAR ADCs was used in [16] to achieve 7.7 effective bits at 1.35 GS/s. This architecture requires a separate track-and-hold and buffer circuit in each channel, as well as the residue amplifier, which leads to non-optimal noise performance. In [1] interleaving 64 SAR ADC channels achieved more than 8 effective bits of resolution at 2.6 GS/s. Although more efficient than comparable flash converter implementations, resampling and buffering of the input signal in this design, coupled with the large area in this solution, lead to a large interleaving power overhead, for a total power of 480 mW.

In this work we present a 2.8 GS/s ADC that interleaves 24 charge redistribution SAR ADC channels and achieves the peak resolution of 8.1 effective bits. Aggressive downsizing of the capacitors, far beyond the matching requirements, is used to enable a compact design and a simple interleaving architecture, without buffering and resampling of the input signal. To support this capacitor downsizing, a digital background calibration algorithm with low power and area overhead has been developed to calibrate the capacitor mismatches in all individual ADC channels, as well as the inter-channel offset, gain and timing mismatches.

The energy efficiency of time-interleaved SAR ADCs and the reasoning behind the selection of the ADC architecture is discussed in Section II. The ADC architecture is presented in Section III. In Section IV the techniques for calibration of the capacitor mismatches are developed. Section V presents details of the timing calibration algorithm. Circuit implementation details of the chip prototype are described in Section VI, followed by the experimental results in Section VII. Section VIII concludes this paper.

II. Energy Efficiency of Time-Interleaved SAR ADCs

The energy per conversion of an ADC, defined as the ratio of the power and the sampling frequency, typically increases with the sampling frequency as shown in Fig. 1. By interleaving M

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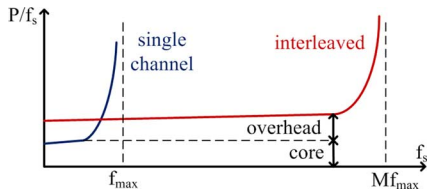

Fig. 1. Energy per conversion versus sampling frequency for a single-channel and a time-interleaved ADC.

ADC channels, the effective sampling frequency increases by a factor of M. The equivalent time-interleaved ADC will always be less energy-efficient than its constituent channels because of the overhead associated with interleaving. The overhead includes the generation and distribution of multiple clock phases, the distribution of the input and reference signals to all channels and correction of channel mismatches [17]. To achieve the best efficiency, the power of both the individual channels and the interleaving overhead should be minimized. Although there is no known exact answer to which architecture is the best choice for a given set of ADC specifications, the empirical data show that SAR ADCs built in sub-100 nm CMOS technologies can achieve excellent power efficiency in moderate sampling frequencies (less than 200 MHz) and resolutions (8–12 bits) [5]–[8]. The majority of modern SAR ADC implementations is based on switched-capacitor circuits, with a capacitive digital-to-analog converter (DAC) that is used to perform radix-based search. To get the maximum power and area savings, these capacitors need to be minimized to the point where the resolution becomes limited by the thermal noise. This minimization also reduces the overhead in distributing the sensitive analog signals common to all channels and increases the bandwidth of the analog front-end. For our target application, the resulting smallest capacitor in the capacitive DAC is much smaller than 1 fF. Matching of capacitors this small is limited by both random variations caused by process variability and systematic layout mismatches, and it can easily limit the overall linearity of the converter. Split capacitor and C-2C arrays [7], [18] have been proposed to solve the problems associated with using the small capacitor sizes. The linearity of the DACs built with these arrays depends on the parasitic capacitances, which creates problems similar to the mismatch of small capacitors in the radix-based arrays. Also, when designed for a thermal-noise-limited operation, these arrays need higher total capacitance. A careful layout technique was used in [19] to achieve 10 bits linearity with unit capacitance of 1.5 fF. This technique requires a careful layout and may be hard to apply to even smaller capacitors. In [20] a sub-radix-2 architecture is used to avoid missing decision levels in the transfer characteristics of the interleaved SAR ADCs and an accurate algorithmic reference converter was used to calibrate capacitor mismatches using a background calibration, based on the least-mean-square (LMS) algorithm. This approach requires the design of two different ADCs, which doubles the design effort. In this work, we eliminate the need for the accurate reference channel by replacing it with an identical copy of one of the time-interleaved channels and by using two modes of conversion for the calibration algorithm, as described in Section III.

Another major problem of the time-interleaved architecture is the timing mismatch of clocks in multiple channels. This problem can be solved by introducing a common front-end sampler, but this approach comes with a power and noise penalty in terms of buffering the sampled voltage and resampling it in the individual channels. A digital timing correction for a system without a common sampler has been proposed by Jamal, *et al.* in [21]. This technique uses fractional delay filters but has high complexity and high power. All analog approaches perform the tuning of the edges of the sampling clock. They differ largely by the method they use to infer the values of the timing mismatches that need to be tuned out. In [11] and [13] FFT processing and calibration DACs were used to infer the timing mismatches. These approaches require complex digital circuits, which may not fit area and power budgets in many systems. An additional single-bit ADC channel is used for timing calibration in [22], where a background calibration algorithm maximizes the correlation between the calibration channel and the time-interleaved channels, thus minimizing the timing errors. This approach is heavily reliant on the statistics of the input signal. In our work, a simple algorithm that uses an estimate of the input signal derivative has been developed and used to obtain the values of the timing mismatches. All calculations are performed in the digital domain and the output of the algorithm is used to fine-tune the edges of the sampling clocks. More details about the timing calibration and the clock generation and tuning are presented in Sections IV and V.

III. Architecture

A high-level block diagram of the proposed ADC architecture is shown in Fig. 2. It consists of $M = 24$ parallel channels, two additional channels that are used for calibration ($\mathrm{SAR0}$ and SARt) and an LMS-based calibration engine. The reference channels are identical to the time-interleaved channels, but they sample the input signal at a different rate. The time-interleaved channels sample the input signal at f_s/M, while the reference channels sample at $f_s/(M+1)$. Every 24 subsequent samples in the reference channel correspond to 24 calibration steps in 24 different time-interleaved channels. For each channel, two modes of conversion, described in Section IV, can be selected by a control signal, sw. A pseudo-random number generator randomly selects the conversion mode in the reference channels, while all time-interleaved channels always perform the same mode of conversion. A resistor, ΔR, is added in series with the channel SARt for the timing calibration purpose, as described in Section V.

Each SAR ADC channel consists of an analog and a digital part. A simplified schematic of the analog part of the ADC channel is shown in Fig. 3. A single-ended version is shown for simplicity, although the actual implementation is fully differential. It consists of an $N = 11$ bit capacitive DAC with nominal radix of 1.85, a comparator, a SAR logic and switches. In the actual implementation the switch S is connected to a bias voltage that defines the input common-mode voltage of the comparator. The outputs of the analog part of the channel are the raw output bits $d_{N-1}, \ldots, d_0$. The digital part of the ADC, $\mathrm{SAR}x\_\mathrm{D}$, is shown in Fig. 4. It takes the raw bit inputs from the analog part and creates the final conversion output as a weighted sum. Each

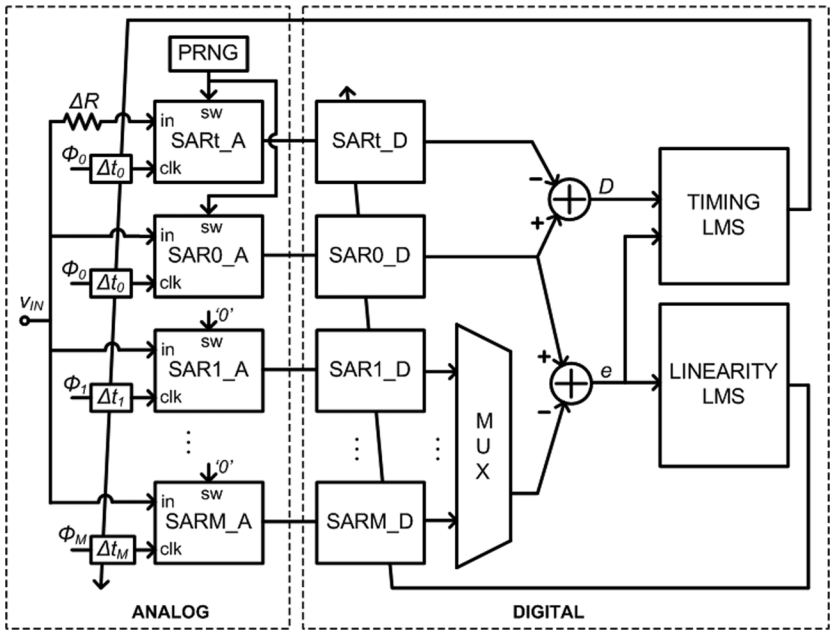

Fig. 2. High-level block diagram of the proposed time-interleaved ADC architecture, outlining analog and digital sections.

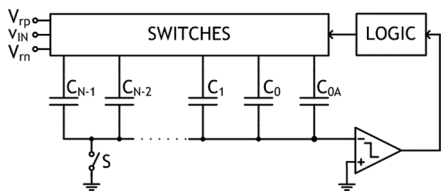

Fig. 3. Simplified schematic of the analog part of a SAR ADC channel.

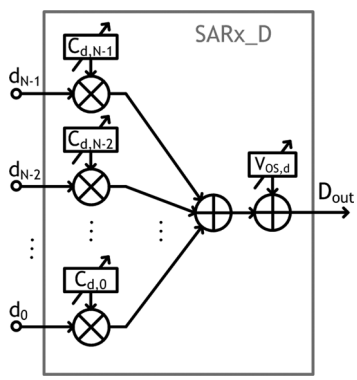

Fig. 4. Digital part of a SAR ADC channel.

bit is multiplied by its corresponding weight coefficient, $C_{d,i}$, and the products are summed up. The values of $C_{d,i}$ represent the capacitor values in the capacitive DAC. At the end, the offset coefficient, V_{osd}, is added to the sum to calibrate the channel offset mismatches, for the final expression

$$D_{out} = \sum_{i=0}^{N-1} C_{di} d_i + V_{osd}. \quad (1)$$

The calibration engine also has two parts: one for the linearity calibration and one for the timing calibration. The linearity calibration is performed completely in the digital domain by adjusting the digital coefficients $C_{d,i}$ and V_{osd} from Fig. 4. The timing calibration uses a mixed-signal feedback in order to tune the delay elements, $\Delta t_0 \ldots \Delta t_M$, shown in Fig. 2. The delay elements are implemented in the clock domain by fine-tuning the edges of the sampling clocks, $\Phi_0 \cdots \Phi_M$. The clock tuning in the SAR0 channel is not necessary, but by being there, it effectively doubles the tuning range of the calibration. The clock tuning in the SARt channel is optional. The details of the calibration algorithms are presented in the following two sections.

IV. Linearity Calibration

A. Direct and Reverse Switching

There are at least two ways to convert the input analog signal using the SAR ADC from Fig. 3. The two modes of conversion performed in this work are called direct and reverse switching in the remainder of this paper. After the input signal is sampled onto all capacitors in the array, the first most significant bit (MSB) needs to be resolved. In direct switching, which is usually considered a standard way of performing conversion, the top plate of the MSB capacitor C_{N-1} is connected to the positive reference V_{rp}, while the top plates of all other capacitors are connected to the negative reference V_{rn} as shown in Fig. 5(a). In the reverse switching, C_{N-1} is connected to V_{rn}, while all other capacitors are connected to V_{rp} as shown in Fig. 5(d). After the comparator input has settled, the comparison is triggered, and the first bit is resolved. If the resolved bit is '1', in the next bit-testing phase, C_{N-1} is connected to V_{rp}. If the resolved bit is '0', C_{N-1} is connected to V_{rn}. This is true for both direct and reverse switching. In the next bit-testing phase C_{N-2} is connected to V_{rp} in direct switching, and to V_{rn} in reverse switching as shown in Fig. 5(b) and (e). After the second bit is resolved, C_{N-2} is connected to V_{rp} if the second bit was '1', or to V_{rn} if the second bit was '0', in both direct- and reverse-switching schemes. This process continues until all N bits are resolved

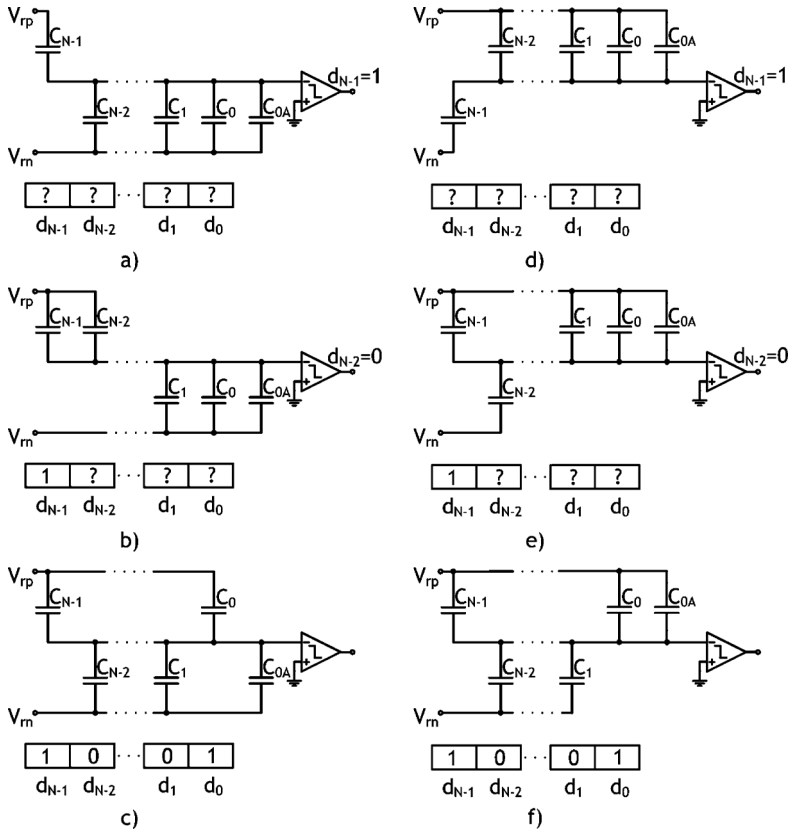

Fig. 5. Illustration of direct and reverse switching in a SAR ADC for (a)-(c) direct switching and (d)-(f) reverse switching.

as shown in Fig. 5(c) and (f). The transfer characteristics of the same 6-bit ADC with radix-1.8 DAC array with two types of switching are shown in Fig. 6. By careful examination of the plots, it can be seen that the transfer characteristics are 180° rotated with respect to each other around the center point. This effect can be explained by noticing that reverse switching conversion of the input signal V_{in} is equivalent to a direct switching conversion of the signal V_{rp}-V_{in}, but the output result is coded in the one's complement code, e.g., all bits are inverted. Due to inherent symmetries of the SAR ADC transfer characteristic, these two characteristics can overlap exactly only in the case of a perfect radix-2 array. If the weight coefficients from (1) are changed to the correct value (radix of 1.8), these two characteristics almost overlap, which shows the characteristics similar to the ones of a perfect radix-2 array. If the input signal is converted twice, once by using the direct switching and the second time by using the reverse switching, then the difference between the two conversion results can be used as an input error signal to the algorithm that will minimize the error by forcing the transfer characteristics to look like the ideal radix-2 curve. This can be achieved by adjusting the capacitor values in the analog domain or by adjusting the values of C_{di} coefficients from (1) in the digital domain. The prototype design in this work uses the digital approach.

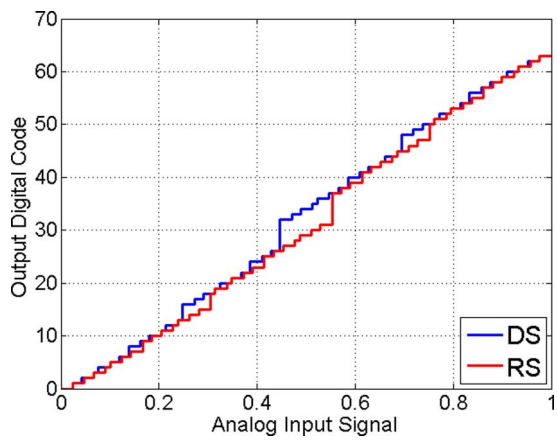

Fig. 6. Transfer characteristic of direct and reverse switching in a 6-bit radix-1.8 SAR ADC.

B. Algorithm

To obtain two conversion outputs for the same input signal sample, the reference channel SAR0, which samples the input signal together with one of the time-interleaved channels, is introduced. The goal of the calibration algorithm is to make the transfer characteristics of all interleaved channels equal to the transfer characteristic of the reference channel, and, at the same time, make the transfer characteristic of the reference channel linear. This can be achieved by randomly choosing the mode of conversion in the reference channel, effectively minimizing the difference between the direct and the reverse switching transfer characteristic of the reference channel. When the error is minimized, both transfer characteristics are equal and linear.

After the input signal sample is converted in the reference channel and one of the time-interleaved channels (k^{th} channel),

the error signal, e, is formed as a difference of the two conversion outputs:

$$e = D_{out}^{0} - D_{out}^{k} = \sum_{i=0}^{N-1} C_{di}^{0} d_i^{0} - \sum_{i=0}^{N-1} C_{di}^{k} d_i^{k} - V_{osd}^{k}, k = 1, 2, \ldots 24, \quad (2)$$

where the subscripts and superscripts indicate the bit number and the channel number, respectively. The offsets are calculated relative to the reference channel, so the interleaved ADC has a DC offset equal to the reference channel's offset. If DC accuracy is needed, the offset of the reference channel would need to be calibrated as well. By applying the LMS algorithm to (2), the update equations for the digital coefficients are obtained:

$$C_{di,j+1}^{0} = C_{di,j}^{0} - 2\mu e d_i^{0} \quad (3)$$

$$C_{di,j+1}^{k} = C_{di,j}^{k} + 2\mu e d_i^{k} \quad (4)$$

$$V_{osd,j+1}^{k} = V_{osd,j}^{k} + 2\mu e. \quad (5)$$

All digital coefficients are represented with four fractional bits in order to minimize the accumulation of the quantization error. The convergence speed can be traded for the accuracy of the converged results by adjusting the value of the LMS coefficient μ. To avoid costly multipliers, the value of μ is set to a power of two. The implementation of (3)–(5) requires only additions, subtractions and logic AND operations, leading to a low overhead per channel. Since the offsets are calibrated in digital domain, the input signal range is slightly reduced. This effect is, however, insignificant since the input signal range is much larger than the expected offset values.

C. Limitations of the Algorithm

Since the error signal can be zero for certain values of the input signal even with capacitor mismatches, the input signal has to be "busy" during calibration, e.g., the input signal samples need to take values that are diverse enough to contain the information about all the capacitors in the array. The expression on the right side of (2) contains $2N + 1$ unknown coefficients, so the necessary condition that the input signal samples need to satisfy is to contain at least $2N+1$ different values. A sufficient condition can be obtained if $2N+1$ subsequent expressions for the error signal (2) are set to zero and treated as a system of equations. If the rank of the corresponding matrix is $2N + 1$, the system has a solution and the calibration will converge to the right values of the digital coefficient.

V. Timing Calibration

A. Basic Idea

Timing mismatches can be corrected if sampling instances of all time-interleaved channels are aligned to the sampling instance of the same reference channel that is used for linearity correction. Fig. 7 illustrates the nature of the error signal due to a timing mismatch. A timing error Δt creates an error in the sampled signal that is approximately equal to $e = -D\Delta t$, where D is the derivative of the input signal at the nominal sampling time. By applying the LMS algorithm to the error expression, the update equation for the estimate of the Δt is obtained:

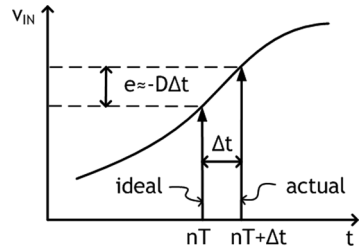

Fig. 7. Graphical illustration of the sampling error due to a timing mismatch, Δt.

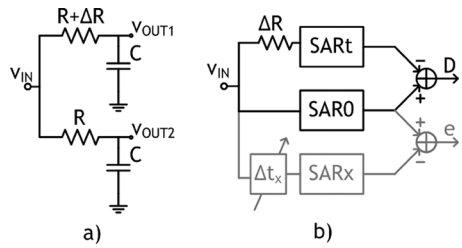

Fig. 8. Derivative estimation (a) concept (b) implementation block diagram.

$\Delta t_{i+1} = \Delta t_i + 2\mu e D$. The only remaining problem is how to obtain the signal D. It is important to note that, since Δt is tuned in the analog domain, it is not necessary to know the derivative exactly; it is sufficient to have an estimate that will drive the LMS algorithm on average in the right direction. Once the timing mismatch is corrected, the error is equal to zero and the value of the D signal is not of importance anymore.

B. Derivative Estimation

One of the simplest ways to obtain an estimate of the derivative is to pass the input signal through two RC circuits with different bandwidths and to subtract the capacitor voltages of the two RC circuits. This concept is illustrated in Fig. 8(a). In this figure, the bandwidth of the upper RC circuit is intentionally lowered by increasing the resistance R by ΔR. The transfer function from the input signal to the difference of the voltages V_{out2} and V_{out1} is given by $D(s) = sC\Delta R/((1 + sCR)(1 + sC(R + \Delta R)))$. The zero at zero creates the desired property of a derivative needed for the timing calibration. The two mismatched RC circuits are implemented by introducing another calibration channel, SARt, and intentionally placing a resistor ΔR in series with this channel, as shown in Fig. 8(b). The analog front-ends of the two calibration channels serve as two mismatched RC circuits. In our design, $\Delta R \approx 220\ \Omega$, which reduces the bandwidth of the SARt channel by approximately two times. ΔR is implemented as a poly resistor and its exact value does not need to be known precisely. Therefore, no programmability of ΔR is provided. SARt always samples together with $\mathrm{SAR0}$. After the conversion, the two outputs are subtracted in the digital domain to obtain the derivative estimate used in the LMS update equation for Δt.

C. Practical Implementation

The practical implementation of the algorithm is shown in Fig. 9. The multiplication by μ and digital integration perform

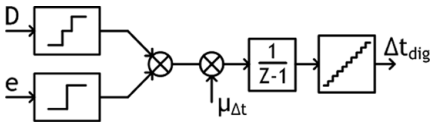

Fig. 9. Block diagram of a practical implementation of timing calibration.

the LMS updates. The quantizer at the output of the timing calibration limits the resolution of the circuit used to tune the sampling clock edges. Since all information necessary for phase mismatch calibration is contained in the phases of the signals e and D, the algorithm can be modified to use only signs of these two signals, as shown in Fig. 9. Additionally, a dead zone around zero is introduced for D signal. This solves three potential problems. First, the amplitude of the signal D varies a lot with input signal frequencies, causing non-smooth convergence of Δt estimates at the frequencies where the amplitude of D is high. The sign function eliminates the amplitude information from the control loop. Second, at low frequencies the amplitude of D is so small that its sign can be determined by the secondary effects, such as residual nonlinearities in the transfer functions of the ADCs, which can cause convergence problems. The dead zone around zero disables the calibration at low input frequencies, where the timing mismatches do not degrade the performance anyway. Finally, using signs of e and D significantly simplifies the implementation by avoiding the need for costly hardware multipliers.

A behavioral model of the system that includes timing, offset, gain and capacitor mismatches, as well as the effects of the thermal noise and jitter, has been implemented in software. As confirmed by extensive behavioral simulations, the timing calibration can be performed simultaneously with the linearity calibration.

D. Algorithm Limitations

The timing errors will be calibrated only if the amplitude of D is larger than the introduced dead zone around zero. This poses a restriction on the amplitude and frequency of the input signal. For a given input signal frequency, the amplitude of the input signal has to be higher than a certain threshold value that is determined by the input frequency. Assuming a single-pole approximation of the input sampling networks and a sinusoidal input signal with amplitude A and frequency ω, the following condition has to be met:

$$A > \delta \frac{\sqrt{(1+(\omega CR)^2)(1+(\omega C(R+\Delta R))^2)}}{\omega C \Delta R} \tag{6}$$

where δ is the size of the dead zone for signal D. This condition is typically met for the signals of interest. When the condition is not met, the calibration can be performed in the foreground, by using an appropriate training sequence.

VI. Circuit Implementation

A. Single SAR ADC Channel

A conventional switched-capacitor SAR ADC architecture, shown in Fig. 3, is used in this work. The comparator is a commonly used sense-amplifier based latch [23]. The comparator schematic is shown in Fig. 10. The $\mathrm{M_1}$ and $\mathrm{M_2}$ form an input differential pair whose outputs drive a cross-coupled inverter pair formed by $\mathrm{M_3}$-$\mathrm{M_6}$. The clocked tail device, $\mathrm{M_{clk}}$, ensures that no static current is consumed. The $\mathrm{M_{r1}}$-$\mathrm{M_{r6}}$ are the reset devices that eliminate the memory effect at the internal nodes of the comparator.

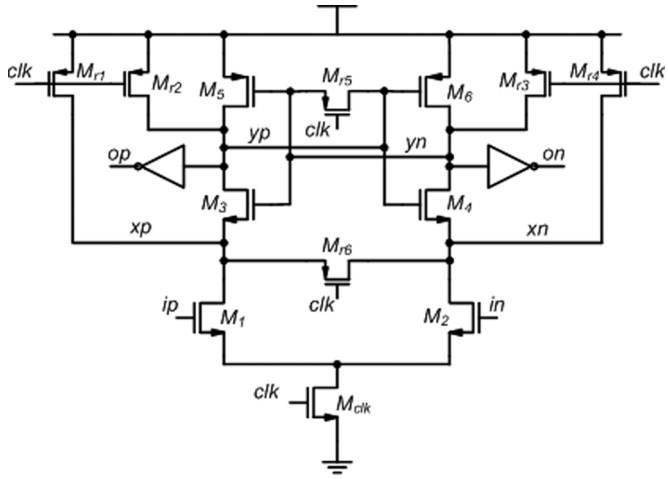

Fig. 10. Comparator schematic.

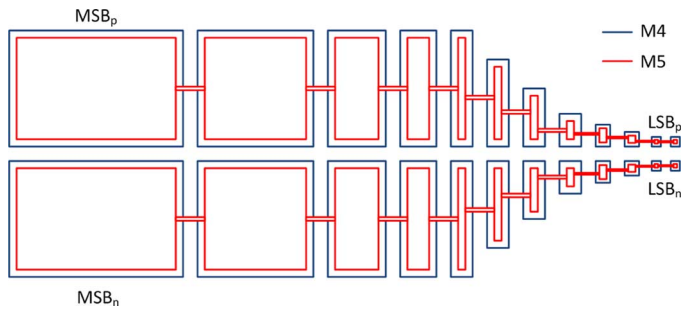

Fig. 11. Layout illustration of a differential capacitive DAC.

The DAC capacitors are realized as parallel-plate capacitors between regular metal-4 and metal-5 layers. The parallel-plate capacitors are selected so the wires connecting the capacitors to the top-plate switches and the wires connecting the DAC drivers to the SAR logic can be routed under the capacitors with minimum disturbance of the capacitor ratios in the DAC. Also, the parallel-plate capacitors with values as low as 50 aF were readily available in the design kit, so no 3D simulation and modeling were required. In this design, the total thermal noise level is set close to 9 effective bits (56 dB). Approximately one half of it is allocated to the sampling $\mathrm{kT/C}$ noise and one half to the comparator noise. The SNR due to thermal noise can be calculated as

$$SNR = \frac{P_{sig}}{2\gamma \frac{kT}{C_{DAC}}\left(1+\frac{C_\mathrm{p}}{C_{DAC}}\right) + v_{nc}^2\left(1+\frac{C_\mathrm{p}}{C_{DAC}}\right)^2} \tag{7}$$

where P_{sig} is the input signal power, γ is the device noise factor, v_{nc} is the rms inuput-referred comparator noise, and C_{DAC} and C_p are the total DAC capacitance and the total parasitic

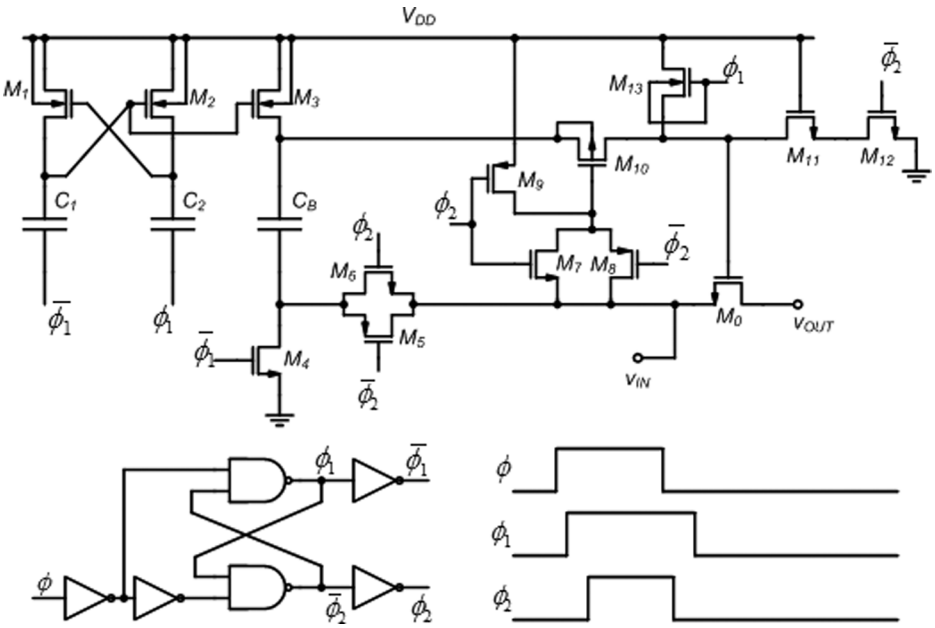

Fig. 12. Schematic of the top-plate bootstrapped switch.

capacitance at the comparator input node, respectively. $C_{\rm p}$ includes the input capacitance of the comparator, the parasitic capacitance of the bottom-plate switches and the parasitic capacitance between the metal-5 DAC capacitor plates and the metal-7 shield. With a $2\mathrm{V_{p\text{-}p,diff}}$ input sinusoidal signal, $v_{nc} \approx 0.4$ mV and $C_{\rm p} \approx C_{DAC} = 50$ fF, the sampling $\mathrm{kT/C}$ noise and the comparator noise correspond to the SNR of approximately 60 dB and 59 dB, respectively. The LSB capacitance of 50 aF is used for the quantization noise at the 10-bit level. Capacitors with calculated values are simply instantiated from the process design kit and placed in the layout, as illustrated in Fig. 11. No special matching techniques are used. DAC switches are sized to provide around seven time constants for settling. The positive reference voltage is generated using an on-board linear regulator. In order to reduce the disturbance of the reference voltage to much less than one LSB, two decoupling MOS capacitors with 0.8 nF capacitance are placed on the chip, one for even-numbered and the other for odd-numbered channels. The negative reference voltage is the shared ground.

To maintain low distortions with high input swing, bootstrapping of the top-plate switches is used. The schematic of the bootstrapped switch together with the non-overlapping clock generator is shown in Fig. 12. The switch is a slightly modified version of the bootstrapped switch proposed in [24]. The CMOS switches $\mathrm{M_5}$-$\mathrm{M_6}$ and $\mathrm{M_7}$-$\mathrm{M_8}$ are used for faster turn-on time. The body contacts of M_1, M_2 and M_3 are tied to V_{dd} to lower the threshold of these devices, making the use of minimum-sized transistors possible, and to reduce the required capacitances of C_1 and C_2. It also improves reliability of the circuit since no two terminals of M_1, M_2 and M_3 experience voltage difference larger than V_{dd}. M_{13} precharges the gate of M_0 to approximately V_{dd}-V_{th} right before the tracking phase. This reduces the effect of charge sharing and the required capacitance of C_B. It also keeps transient voltage between the source and the drain of M_{10} under V_{dd}. ϕ is one of the twenty-four phases obtained by division of the main clock. The non-overlapping clock generator is used to separate the precharging phase from the tracking phase in a robust way. The SAR logic and the DAC switch drivers are implemented using standard CMOS logic cells that were manually placed and connected. Additional power savings would be possible with custom-designed logic.

B. Clock Generation

A simplified schematic of the sampling network of the time-interleaved ADC is shown in Fig. 13, together with timing diagrams of the different clocks needed for the circuit operation. C_S, although shown as a single sampling capacitor, represents the whole bank of capacitors from the capacitive DAC. In addition to the $M = 24$ time-interleaved channels and the reference channel, two dummy channels sample the input signal while the reference channel is performing the conversion. This way the same impedance is present at the input of the ADC for every sample. Also, the second reference channel for timing calibration with its set of two dummy channels is implemented, but not shown in Fig. 13 since its clocks, while being physically separate signals, have the same timing diagrams as the ones for the first reference channel. Every channel needs two clocks, one for the top-plate switch, and the other for the bottom-plate switch. The falling edge of the bottom-plate clock occurs before the top-plate switch closes in order to get the benefits of the bottom-plate sampling. The top-plate clocks, $\phi_1 \ldots \phi_M$, are generated by a simple circular shift register, which is clocked by a buffered version of the master clock. Clock phases $\phi_{\rm r}$, ϕ_{d1}, and ϕ_{d2} are generated by flip-flops that are clocked by the same clock as the circular shift register to achieve the same delay from the master clock to multi-phase clocks. The circuit that generates the bottom-plate clocks is shown in Fig. 14. The input clock is a sinusoidal differential signal and it is AC-coupled to the chip using the big off-chip capacitors C_B. The first stage buffer is common for all channels, thus minimizing the timing skew

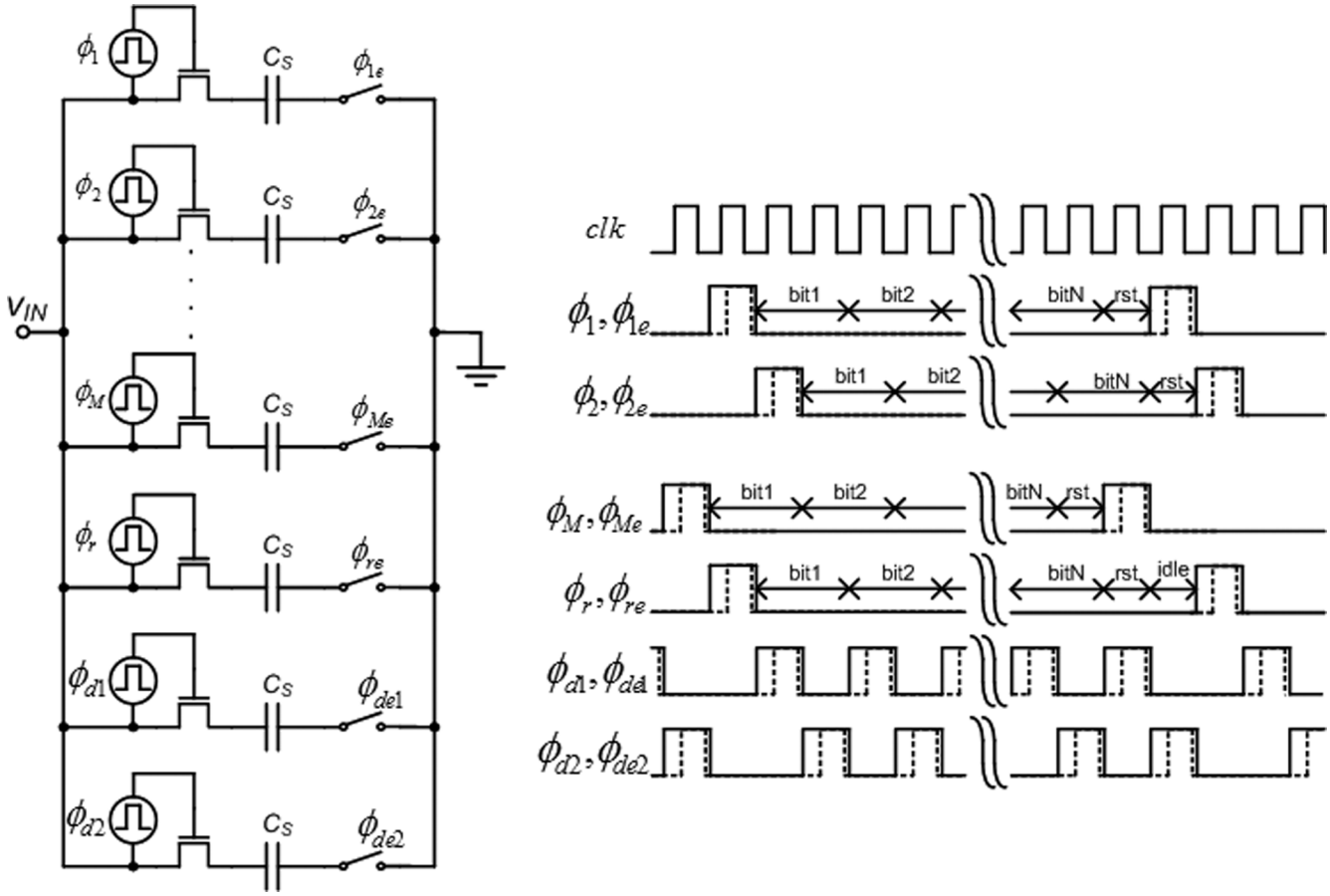

Fig. 13. Clock signals with timing diagrams.

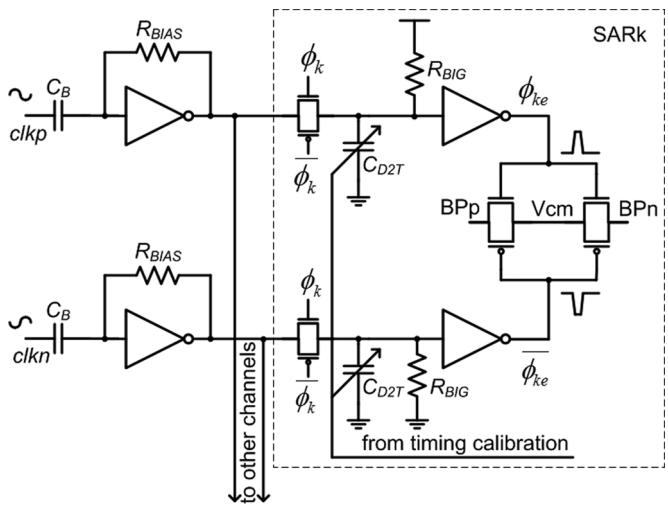

Fig. 14. Generation of bottom-plate sampling clocks.

between channels, and it is realized as a simple inverter with low-threshold transistors and a large bias resistor R_{BIAS} connected between the input and the output of the buffer. The output of the first stage buffer is distributed to all channels using thick low-resistance metal-7 wires. In each channel, the pseudo-differential clock is gated by two simple CMOS switches. These switches are controlled by the same clock signals used to drive the top-plate switches. The second (and last) stage of buffering is also realized as simple inverters with low-threshold devices. The bottom-plate switches are CMOS switches and are driven pseudo-differentially. Corner and mismatch simulations are used to verify that the delay mismatch between the two paths of the pseudo-differential clock is sufficiently small, including the phase and amplitude imbalance from the on-board balun. The big resistors R_{BIG} at the input of the second-stage buffers keep the bottom-plate switches closed during the conversion process. The variable capacitors C_{D2T} are used for fine-tuning of the edges of the sampling clocks, and their value is controlled by the timing calibration algorithm. The implementation of the clock tuning is shown in Fig. 15. The variable capacitors C_{D2T} are implemented as a bank of 31 small MOS capacitors that can be switched in or out of the clock path, thus enabling a 5-bit control of the capacitor value. To ensure monotonicity, the switching of the MOS capacitors is controlled by thermometer-coded outputs from the timing calibration algorithm. The minimum tuning step is $\Delta t_{step} = 300$ fs, for the total tuning range of approximately ± 4.8 ps. If the initial timing mismatch is Δt, after the calibration converges, the residual mismatch will toggle between $\Delta t_{res} = \Delta t \bmod \Delta t_{step}$ and Δt_{step}-Δt_{res}, where mod is the modulo operation. Assuming the probabilities of the residual mismatch being Δt_{res} and Δt_{step}-Δt_{res} are $1 - \Delta t_{res}/\Delta t_{step}$ and $\Delta t_{res}/\Delta t_{step}$, respectively, the expected rms value of the timing mismatch is $\Delta t_{step}/\sqrt{6}$. For a sinusoidal input at

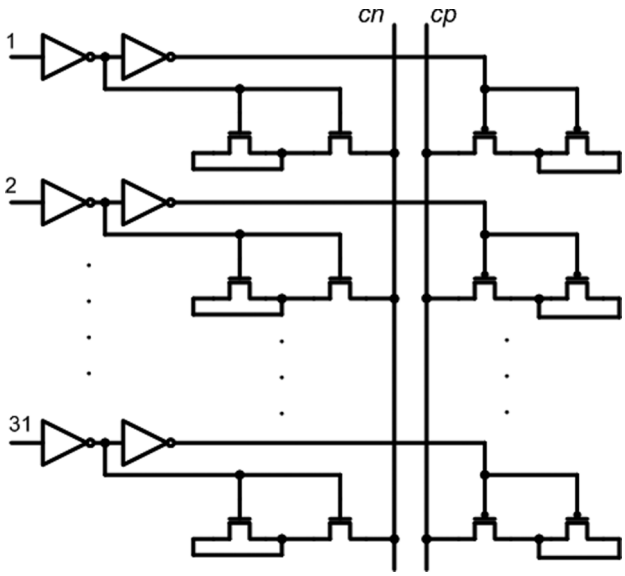

Fig. 15. Implementation of clock tuning.

1.4 GHz this level of residual timing mismatches will limit the SNDR to approximately 59 dB.

C. Calibration Logic

Calibration logic consists of two parts: the first one calculates the weighted sum of digital raw output bits from all ADC channels, and the second one implements the LMS algorithm and iteratively calculates the value of digital weight coefficients. The first one needs to be running all the time, while the second one can be shut down after the calibration converges, run periodically to track the environment changes, or run continuously if it can be guaranteed that the input signal is going to be 'busy'. The calibration logic has been described in the Verilog hardware description language. Synthesis from a register transfer level description and place-and-route have been performed to obtain the final physical design with the area of 0.23 mm × 0.76 mm and an estimated power of approximately 10 mW.

VII. Experimental Results

A chip prototype has been implemented in a seven-metal, single-poly 65 nm CMOS process. A die photo is shown in Fig. 16. A memory buffer with 14 k of 11-bit words for capturing the conversion outputs was placed on chip to facilitate testing. The chip area, including pads, is $1.03 \times 1.66\ \mathrm{mm}^2$. The analog core area, which includes all SAR ADC channels and the clock generation, is $0.4 \times 0.45\ \mathrm{mm}^2$. The calibration is performed with a sinusoidal input signal with $2.2\mathrm{V}_{\text{p-p,diff}}$ amplitude and frequency around 900 MHz. The calibration coefficients were frozen and used for all subsequent measurements in order to include the effect of the bandwidth mismatch in a single-tone testing. The ADC would need to be recalibrated if the supply voltage or temperature changes significantly, mostly because of the high sensitivity of the comparator offsets to these parameters. The delay cells, while being less sensitive than the comparator offsets, still can be a significant factor if the high-frequency performance needs to be maintained. Unless otherwise

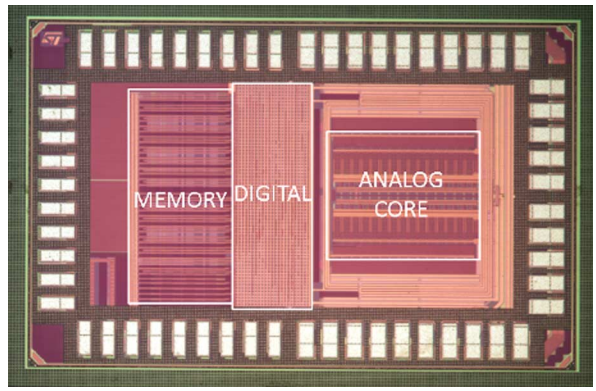

Fig. 16. Die photo.

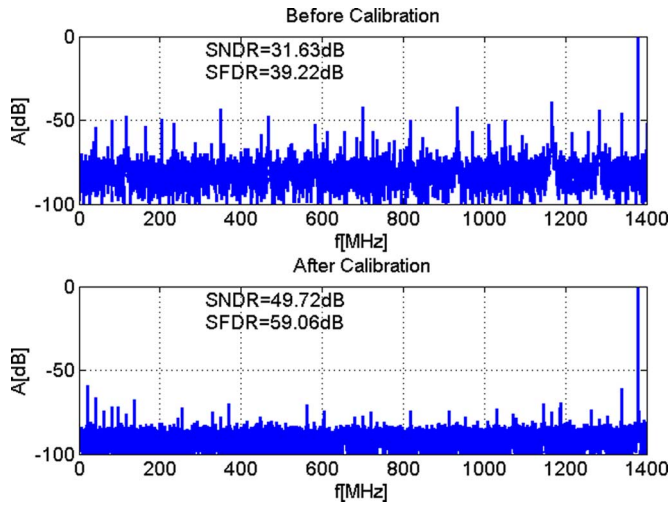

Fig. 17. Spectrum before and after calibration for $\mathrm{f}_{in} = 1379.56$ MHz (before calibration $\mathrm{SNDR} = 31.6$, $\mathrm{SFDR} = 39.2$ dB, after calibration $\mathrm{SNDR} = 49.7$, $\mathrm{SFDR} = 59$ dB).

noted, the measurements are performed at room temperature, 2.8 GS/s sampling speed, 1.2 V supply voltage and $1.8\mathrm{V}_{\text{p-p,diff}}$ input signal amplitude.

The effectiveness of the calibration algorithm is illustrated in Fig. 17, where the spectrum of the output signal is shown before and after the calibration. Before calibration, the SNDR and SFDR are 31.6 and 39.2 dB, respectively. After the calibration, both SNDR and SFDR are improved by more than 19 dB. The resulting SNDR and SFDR are 49.7 and 59 dB, respectively.

Contributions of different non-idealities to the performance of the uncalibrated converter can be estimated from the values of the calibration coefficients. Fig. 18 shows the values of the capacitor ratios for different bit positions in one of the channels on four measured chips. By reconstructing the transfer characteristic of the ADC from the capacitor ratios, it can be estimated that the capacitor mismatches limit the performance to approximately 6 effective bits. The systematic layout mismatches are much larger than the random variations. The values of the channel offsets in 24 channels on four different chips are shown in Fig. 19. The standard deviation of offsets is 14 mV, which would limit the converter performance to 5.2 bits. The timing mismatches in 24 channels on four different chips are shown in Fig. 20. The estimated standard deviation of 0.69 ps

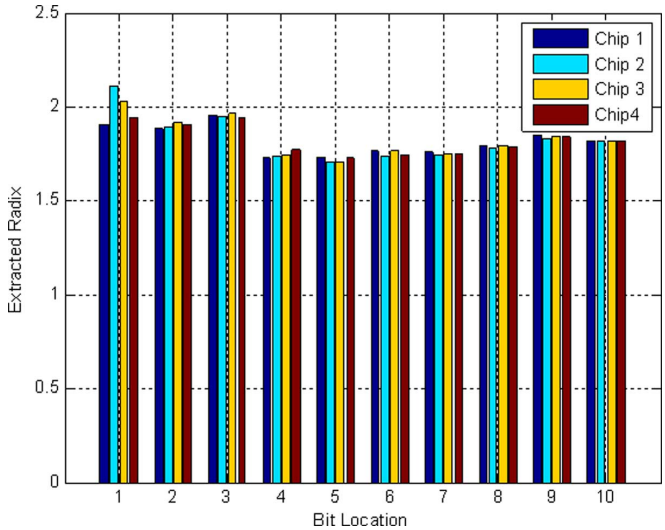

Fig. 18. Radix values on four different chips.

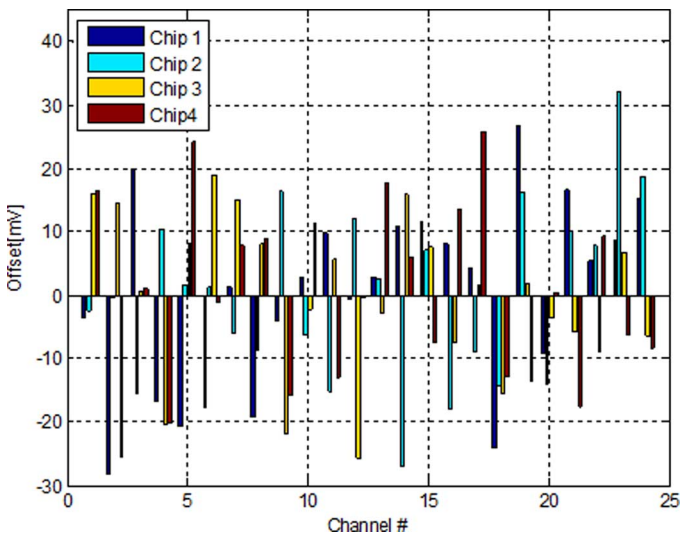

Fig. 19. Offset values on four different chips.

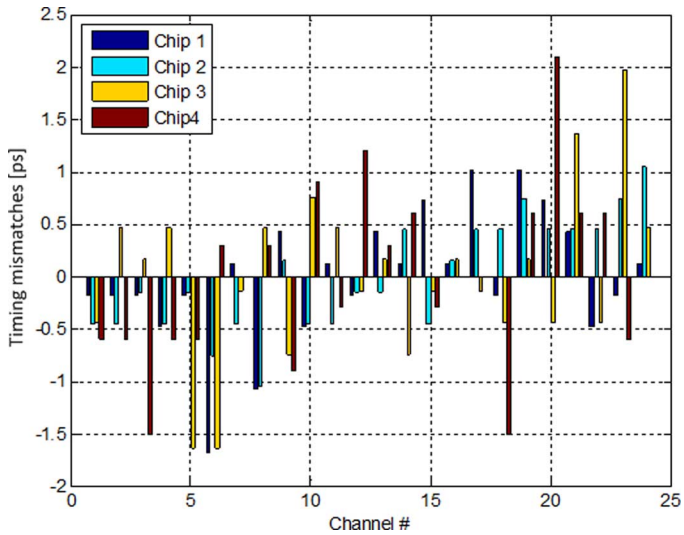

Fig. 20. Timing mismatches on four different chips.

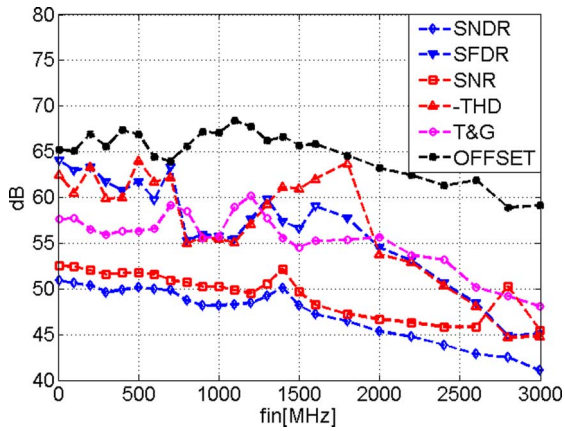

Fig. 21. Performance plots versus input frequency ($f_s = 2.8$ GHz, $V_{dd} = 1.2$ V).

would limit the performance to 7 effective bits without timing calibration.

To verify performance of the ADC across different input frequencies, the input signal frequency has been swept from 5 MHz to 3 GHz. The calibration was done at one input frequency (around 900 MHz), and the measurements were performed with frozen calibration coefficients. The performance plots are shown in Fig. 21. T&G and OFFSET represent the ratio of the signal power and the powers of the interleaved time/gain and offset tones, respectively. The SNR curve was obtained by nulling the first thirteen harmonics and all interleaved offset, timing and gain tones in software and by treating the remaining spectral content as noise. Visual inspection has been performed to ensure that no other visible tones were present. The rms jitter value of 320 fs explains the SNR shape at most frequencies, except in the vicinity of $kf_s/2$, where the rms jitter value is lowered to 110 fs. This can possibly be explained by the fact that the ADC is laid out as two ADCs sampling at the frequency $f_s/2$. When the input frequency is close to $kf_s/2$, the activity of digital circuits in each half of the ADC is lowered, creating less coupling to the clock buffers. The jitter contribution of the clock source used in the measurements is less than 40 fs rms.

The ADC achieves the SNDR of 50.9 dB at low input frequencies and maintains the SNDR higher than 48.2 dB up to the Nyquist frequency. The SFDR stays above 55 dB up to 2 GHz. The 3 dB effective resolution bandwidth is 1.5 GHz. The THD is limited mainly by the third harmonic, except at low frequencies where the second harmonic dominates due to a high phase and amplitude imbalance in the input balun.

The ADC has been tested with different sampling frequencies. Even though the ADC was recalibrated for each sampling frequency, less than 1 dB SNDR degradation is expected if a single set of calibration coefficients is used across different sampling frequencies, mostly stemming from the slightly different values of the timing coefficients. The SNDR plots versus the input frequency for the sampling frequencies of 1 GHz, 2 GHz, 2.8 GHz, and 3 GHz are shown in Fig. 22. The SNDR at low input signal frequencies is slightly higher for lower sampling frequencies, but it drops faster with increase of the input frequency due to more charge leakage in the bootstrapping circuit of the top-plate switches. The performance at 3 GHz and higher

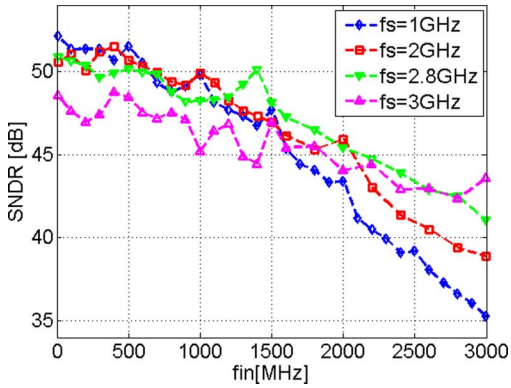

Fig. 22. SNDR versus input frequency for sampling frequencies of 1 GHz, 2 GHz, 2.8 GHz and 3 GHz.

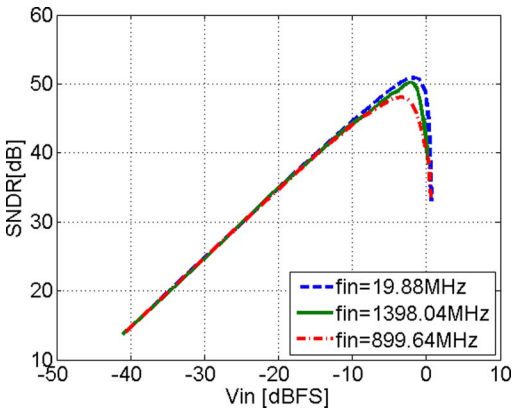

Fig. 23. SNDR versus input signal level for three input frequencies.

sampling frequencies is limited by the DAC settling errors and the speed of the bootstrapping circuits in the top-plate switches in the sampling network.

The SNDR versus the input signal amplitude is shown in Fig. 23 for three different input frequencies. The SNDR levels off at approximately 3/4 of the full scale because the distortion from the top-plate switches starts to increase at that level. When some of the channels begin to saturate, the SNDR falls off sharply.

The performance summary is shown in Table I. The total power consumed by the ADC at $f_s = 2.8$ GHz and $V_{dd} = 1.2$ V with ongoing calibration is 44.6 mW. The power consumption breakdown is shown in Fig. 24. The reference power represents the power drawn from the positive reference pin. The standard figure of merit (FoM) is 56 fJ/conversion-step calculated with low-frequency ENOB, or 78 fJ/conversion-step, if calculated with the minimum ENOB in the first Nyquist zone.

The energy per conversion $E_c = P/f_s$ for this ADC is 16 pJ. A comparison to the prior-art ADCs with sampling frequencies higher than 1 GHz published at the ISSCC and VLSI conferences from 1997 to 2012 [25] is shown in Fig. 25.

VIII. Conclusions

A low-power 2.8 GS/s time-interleaved ADC with peak ENOB of 8.1 bits and ERBW of 1.5 GHz is reported. The key technique for power and area efficiency is downsizing of the DAC capacitors to the point where the ADC operates in the thermal-noise-limited regime. The downsizing of the capacitors is supported by a low-overhead calibration of capacitor mismatches and channel offset, as well as the gain and timing mismatches. Together these techniques have enabled the power and area reduction of the ADC prototype to achieve a figure of merit lower than 78 fJ/conversion-step across the entire first Nyquist zone.

Efficient implementation of this ADC enables digital implementation of emerging applications. These include baseband signal processing for mm-wave wireless communications with higher constellation modulations, direct-sampling TV receivers and wide-bandwidth digital spectrometers. This architecture is expected to scale favorably with technology.

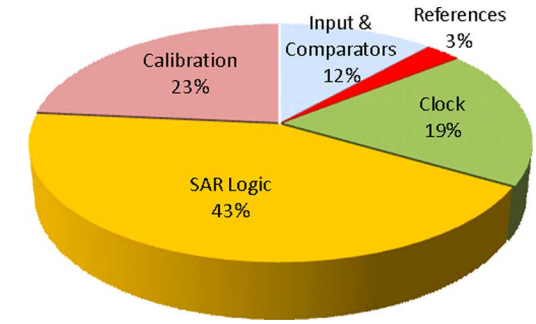

Fig. 24. Power consumption breakdown at $f_s = 2.8$ GHz, $V_{dd} = 1.2$ V.

TABLE I
Performance Summary

Sampling rate	2.8GS/s
Resolution	11b (10b with <0.5dB SNDR loss)
Peak SNDR	50.9dB
SNDR	>48dB (up to 1.5GHz)
SFDR	>55dB (up to 2GHz)
ERBW	1.5GHz
Input Bandwidth	>3GHz
Input	$1.8V_{pp\text{-}diff}$
Chip area	$1.7mm^2$
Analog core area	$0.18mm^2$
Technology	ST 65nm CMOS
Supply voltage	1.2V
Power	44.6mW

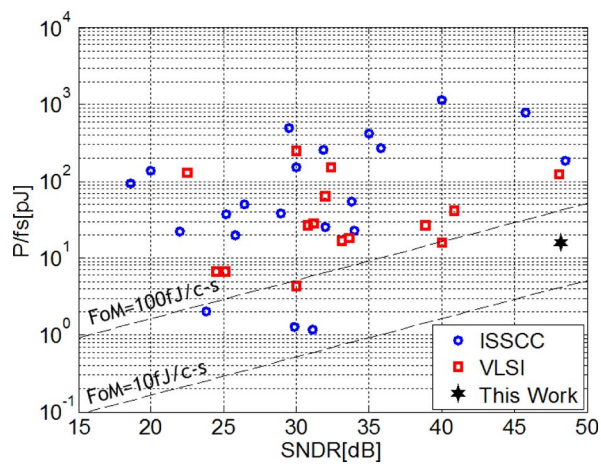

Fig. 25. Energy per conversion for all ADCs with $f_s > 1$ GHz published at ISSCC and VLSI conferences from 1997 to 2012.

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