Multiple-Input Relay Design for More Compact Implementation of Digital Logic Circuits

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***Abstract*—Multiple-input relays are proposed to enable more compact implementation of digital logic circuits, and the first functional prototypes are presented. A relay with three equally sized input electrodes is demonstrated to perform various three-input logic functions, with a delay that can be well predicted by a lumped-parameter model. Relays with differently sized input electrodes can be used to perform more complex functions. A flash-type analog-to-digital converter is presented as one example.**

***Index Terms*—MEMS, multiple inputs, NEMS, relay.**

I. Introduction

NANOELECTROMECHANICAL relay technology has been proposed as a potential solution to overcome the fundamental energy-efficiency limit of CMOS technology, because it offers the ideal characteristics of zero OFF-state leakage current and abrupt *on/off* switching behavior which provide for zero static power consumption and aggressive supply voltage ($V_{\rm DD}$) scaling [1], [2]. Various digital integrated circuit (IC) building blocks (logic, memory, and clocking structures) implemented purely with microelectromechanical relays have been demonstrated recently [3], [4]. Due to the large ratio between the mechanical (switching) delay and the electrical (capacitive charging) delay of a relay, an optimized relay-based IC design should comprise a single-stage complex logic gate between latches, so that the time required to perform any digital logic operation is essentially one mechanical delay [2]. Relay designs that incorporate multiple input (gate) electrodes and multiple pairs of output [source/drain (S/D)] electrodes enable more compact implementation of digital ICs at no incremental process cost. To illustrate this point, a generic n-input digital logic gate comprising only two relays is shown in Fig. 1. The "pull-up" relay connects the output to the power supply when it is turned on, whereas the "pull-down" relay connects the output to the ground when it is turned on. Each input signal is connected to one input electrode of the pull-up relay and also to one input electrode of the pull-down relay, and only one of these relays is on at any given time, i.e., they operate in a complementary manner. Note that each relay can comprise multiple pairs of S/D electrodes, to provide for greater functionality, e.g., output signals at various voltage levels (as indicated in the figure) or differential output signals. In this letter, the first functional prototype multiple-input relays are presented.

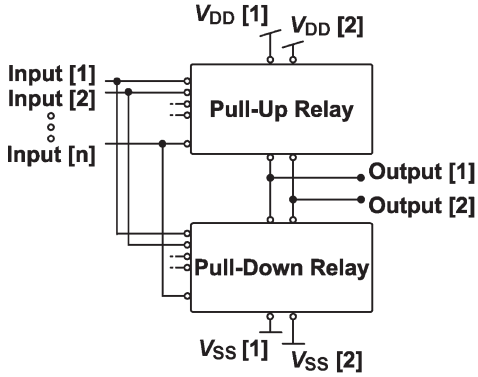

Fig. 1. Generic complementary-relay combinational logic circuit.

II. Multiple-Input Relay Design

Fig. 2(a) shows the structure and operation of a prototype three-input two-output relay design: In the OFF state, an immeasurably low leakage current flows because an air gap (of thickness $T_{\rm CONT}$) separates the channels from the pairs of S/D electrodes on each side. As the voltage applied to the gate electrode(s) increases beyond a threshold "pull-in" voltage ($V_{\rm PI}$), the relay turns on abruptly, because the attractive electrostatic force between the gate electrode(s) and the movable body electrode brings the channels (attached underneath the body electrode via an insulating oxide layer) into contact with the S/D electrodes

$$V_{\rm PI} \propto \sqrt{\frac{kT_{\rm ACT}^3}{\varepsilon_0 A}} \tag{1}$$

where k is the spring constant of the movable structure, $T_{\rm ACT}$ is the as-fabricated actuation gap thickness, ε_0 is the dielectric permittivity of air, and A is the gate-to-body overlap area.

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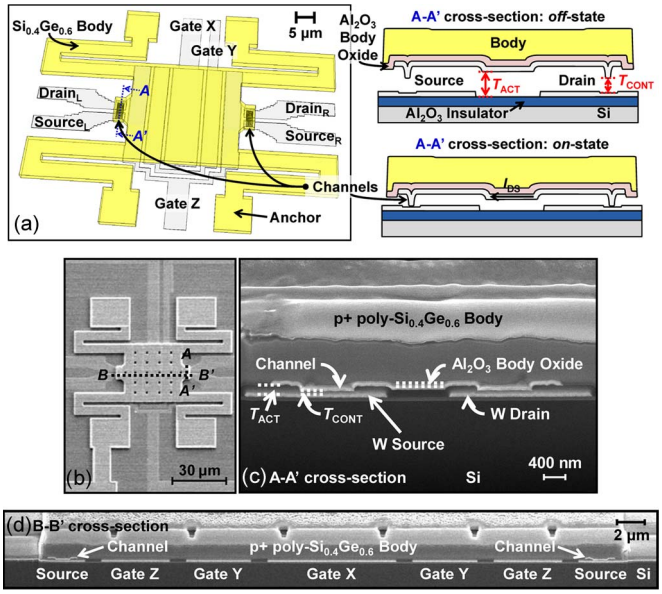

Fig. 2. Three-input two-output relay structure. (a) Three-dimensional schematic, (b) plan-view SEM of an unreleased device, (c) cross-sectional SEM (X-SEM) along $A-A'$ in (b), and (d) X-SEM along $B-B'$ in (b). $T_{\mathrm{BODY}} = 900$ nm, $T_{\mathrm{BODY.OXIDE}} = 45$ nm, $T_{\mathrm{CHANNEL}} = 50$ nm, T_{ACT} (as-designed) $= 180$ nm, T_{CONT} (as-designed) $= 90$ nm, $T_{\mathrm{GATE}} = T_{\mathrm{SOURCE}} = T_{\mathrm{DRAIN}} = 60$ nm, and $T_{\mathrm{SUBSTRATE.INSULATOR}} = 80$ nm. The gate electrodes—Gate X at the center, Gate Z at the edges, and Gate Y in-between Gates X and Z—are equally sized (each with an area of 288 μm^2 underneath the movable body electrode). Thin films of Pt and Ir were deposited over the poly-$Si_{0.4}Ge_{0.6}$ body electrode for protection during the focused ion beam cutting process for the X-SEMs.

A CMOS-compatible (peak substrate temperature $<$ 410 °C) surface-micromachining process [5] was used to fabricate the relays in this work. The scanning electron microscopy (SEM) images of a fabricated three-input two-output relay are shown in Fig. 2(b)–(d).

III. Results and Discussion

Finite-element method (FEM) simulations were performed to provide guidance for relay design, targeting ~5-V V_{DD} for AND operation [Fig. 3(a)]. Since the voltage level required to turn on the relay increases as the number of driven gate electrodes decreases (since the effective gate-to-body overlap area A increases) AND, MAJORITY ($\mathrm{X} \bullet \mathrm{Y} + \mathrm{Y} \bullet \mathrm{Z} + \mathrm{X} \bullet \mathrm{Z}$) and OR functions can be achieved with the same relay structure by adjusting the input voltage level (i.e., V_{DD}). Fig. 3(b) shows that the measured values of V_{PI} are much higher than the simulated values. Physical analysis [Fig. 3(c)] indicates that the actuation gap (T_{ACT}) is much larger than designed, due to the effect of a negative strain gradient within the structural (body) layer. The measured value of V_{PI} for the case where the input signals are applied to all three gates (input combination [1 1 1], where "1" $\equiv V_G$), i.e., "triple-gate" operation, is ~3× larger than the simulated V_{PI}. This is consistent with the interferometry-based measurements which indicate that T_{ACT} is larger than designed by ~2×, since $V_{\mathrm{PI}} \propto T_{\mathrm{ACT}}^{1.5}$.

The measured V_{PI} for the case where the input signal is applied only to Gate X (input combination [1 0 0]) is larger than those for the cases where the input signal is applied only to Gate Y or Gate Z (input combination [0 1 0] or [0 0 1], respectively)

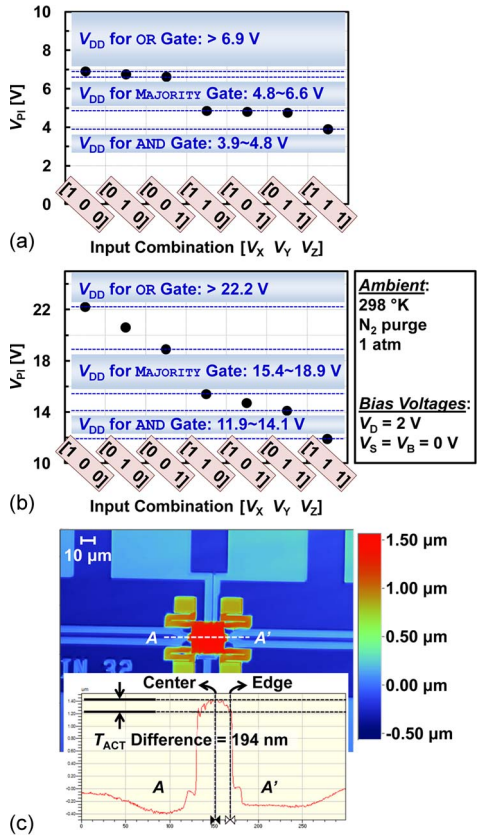

Fig. 3. Comparison of simulation and measurement results for a three-input relay. (a) FEM simulations [6] of V_{PI}, for various combinations of input signals, for the three-input relay. "1" $\equiv V_G$. (b) Measured V_{PI} values. "1" $\equiv V_G$. (c) White-light interferometry topograph of the fabricated relay. T_{ACT} at the body center is 374 nm, which is roughly twice as large as designed.

because T_{ACT} is larger at the center than at the edge of the body due to the convex shape of the body electrode.

The versatility of the three-input relay design is demonstrated in Fig. 4, which shows the measured waveforms for a three-input relay with drain electrodes connected to a 6-V power supply and source electrodes connected to an oscilloscope with 1-MΩ internal resistance: When the input voltage range (corresponding to V_{DD}) is 10 V, the relay performs the AND function; when it is increased to 13 V, the relay performs the MAJORITY function; and when it is increased to 18 V, the relay performs the OR function.

Fig. 5 shows the measured three-input-relay turn-on delay (t_{DELAY}) as a function of the driving gate voltage (V_G), for double- and triple-gate operations. t_{DELAY} decreases with increasing gate overdrive, and triple-gate operation is faster, due to larger electrostatic force between the gates and the body. A negative body bias also improves t_{DELAY} because it serves to reduce T_{ACT} and T_{CONT} in the OFF state, so that the body moves a shorter distance to switch the relay on. A first-order lumped-parameter model predicts t_{DELAY} to be inversely proportional to V_G^2 [7]

$$t_{\mathrm{DELAY}} = \frac{27 V_{\mathrm{PI}}}{4\omega_O \cdot Q \cdot V_G^2}. \tag{2}$$

A reasonable fit to the measured data is achieved with the following parameter values: quality factor $Q = 0.5$,

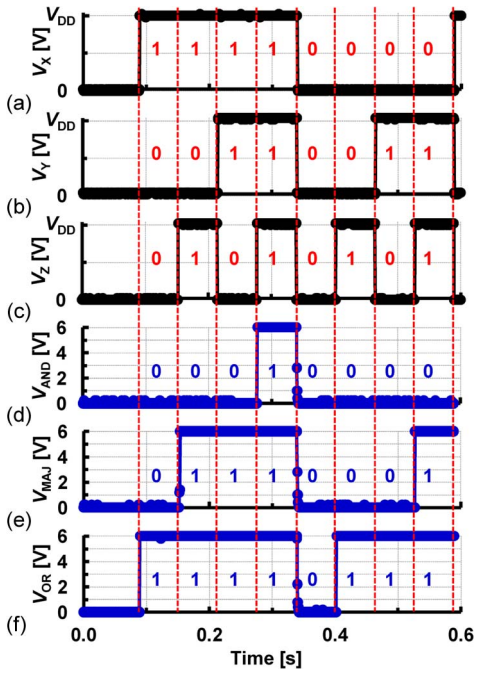

Fig. 4. Measured waveforms obtained using a single three-input relay with drain electrodes connected to a 6-V power supply and source electrodes tied together to form the logic gate output node connected to the oscilloscope (1-MΩ resistance to ground). The body is biased at −2 V. The measurements were made at room temperature and atmospheric pressure, under N_2 purge. (a) INPUT X signal (to "Gate X"). (b) INPUT Y signal (to "Gate Y"). (c) INPUT Z signal (to "Gate Z"). (d) AND output waveform for $V_{DD} = 10$ V. (e) MAJORITY gate (X • Y + Y • Z + X • Z) output waveform for $V_{DD} = 18$ V.

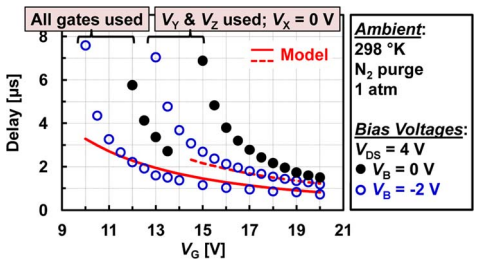

Fig. 5. Measured turn-on delay of a three-input relay as a function of the input voltage, for various values of body bias. A lumped-parameter model (lines) can be reasonably fit to the experimental data.

resonance frequency $\omega_O = 5.4$ MHz, and $V_{PI} = 14.1$ or 11.9 V for double- or triple-gate operation [refer to Fig. 3(c)]. The supply voltage $(V_{DD} > V_{PI})$ must be chosen properly to meet a specific switching delay requirement and to mitigate variations in V_{PI} (refer to Fig. 3).

More complex logic functions can be achieved by adjusting the areas of the input electrodes to give them different weights. (The relative weight of an input gate is determined by its relative gate-to-body overlap area, as compared with the other input electrodes.) For example, by sizing the gate electrodes appropriately, three 3-input relays can be used to implement a flash-type analog-to-digital converter (ADC), as shown in Fig. 6: The switching voltages for single-gate (most significant bit), double-gate, and triple-gate [least significant bit (LSB)] operations decrease linearly to properly decode an analog input signal level (v_{ac}). For instance, if v_{ac} is between 11.7 and 13.3 V, only the LSB relay (with v_{ac} driving all three gates)

	ΔV_{PI} = 0.9 V	ΔV_{PI} = 1.6 V
Electrode Area	Value	Value
$T_{GATE.X}$	192 µm²	96 µm²
$T_{GATE.Y}$	136 µm²	88 µm²
$T_{GATE.Z}$	536 µm²	680 µm²
T_{BODY}	1024 µm²	1024 µm²

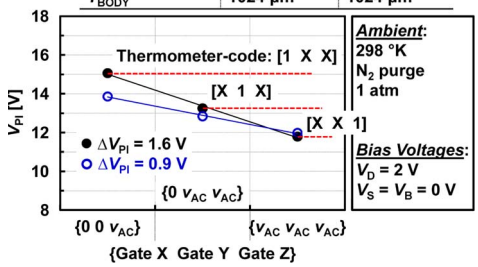

Fig. 6. Measured linearly increasing V_{PI} of a three-input relay with differently sized gates for ADC application.

turns on; the other two relays (with v_{ac} driving only the two smallest gates or with v_{ac} driving only the smallest gate) do not turn on, so that the thermometer code [0 0 1] is generated.

IV. Conclusion

Multiple-input relays have been proposed to implement digital logic more compactly than single-input relays. (Although a multiple-input relay has a larger footprint than a single-input relay for the same input voltage range, the reduction in device count is advantageous because of the significant area required for the suspension beams and anchors and for routing of the S/D electrodes.) A relay with three equally sized input electrodes can perform various three-input logic functions, depending on the input voltage level, with a delay that can be well predicted by a lumped-parameter model. Relays with differently sized input electrodes can be used to perform more complex functions, such as a flash-type ADC.

Acknowledgment

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