Performance and Yield Benefits of Quasi-Planar Bulk CMOS Technology for 6-T SRAM at the 22-nm Node

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***Abstract*—The performance and threshold voltage variability of quasi-planar bulk MOSFETs are compared against those of conventional bulk MOSFETs, via three-dimensional (3-D) device simulations with gate line-edge roughness and atomistic doping profiles, at 25 nm gate length. The nominal performance of six-transistor (6-T) SRAM cells is studied via 3-D simulation of full cell structures. Compact (analytical) modeling is used to estimate SRAM cell yields. As compared to conventional bulk CMOS technology, quasi-planar bulk CMOS technology provides for enhanced SRAM cell performance and yield, and hence facilitates reductions in cell area and operating voltage. It also enables a notchless 6-T SRAM cell design which is advantageous for improved lithographic printability and either smaller area or lower standby power, and is projected to achieve 6-sigma cell yields at operating voltages down to ∼0.8 V.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS), metal–oxide–semiconductor field-effect transistor (MOSFET), static random-access memory (SRAM), variability.**

I. Introduction

Efforts to reduce six-transistor (6-T) static random-access memory (SRAM) cell area [1]–[5] by a factor of two with each new technology generation are the *de facto* driving force for cutting-edge complementary metal–oxide–semiconductor (CMOS) technology development. Continued SRAM cell area scaling is essential to sustaining Moore's Law. However, it is challenged by both increased process-induced variability with transistor scaling and the need to integrate more cells on a die at each successive technology node. Specifically, a growing issue is transistor threshold voltage $V_{\rm TH}$ mismatch due to systematic and random variations [6], [7], which sets a lower limit for the operating voltage of the SRAM array [8]. Variations in $V_{\rm TH}$ caused by random dopant fluctuations (RDFs) and gate line-edge roughness (LER) will become dominant as the gate length L_G is scaled down below 30 nm [9].

Various circuit- and transistor-design approaches have been proposed to address the issue of increasing $V_{\rm TH}$ variation. These include the use of read-assist and write-assist techniques to enhance SRAM read and write margins, e.g., read/write-assist column circuitry, word-line bias, pulsed bit lines, and lower column supply voltages during write [10], [11], which results in lower array efficiency (i.e., larger array layout area). Transistor-design approaches include the use of a super-steep retrograde or delta-shaped body doping profile [12], or the adoption of a transistor structure that provides for improved electrostatic integrity, such as fully depleted ultra-thin-body or multigate structures [13]–[15], to reduce $V_{\rm TH}$ sensitivity to variations. To avoid the need for costly silicon-on-insulator substrates or complex fabrication processes [16], [17], the quasi-planar bulk MOSFET design (Fig. 1) was recently proposed [18]. A simple approach for manufacturing this structure using a conventional CMOS process flow was recently demonstrated to provide for improved yield in an early 28-nm-generation SRAM technology [19], [20]: a timed dilute-hydrofluoric etch is used to slightly recess the shallow trench isolation (STI) oxide just prior to gate-stack formation, resulting in gate electrodes that each wrap around the top portion of their respective MOSFET channel region. In this paper, the potential benefits of quasi-planar bulk CMOS technology versus planar bulk CMOS technology with regard to 6-T SRAM cell performance and yield are assessed, for the 22-nm technology node.

II. Quasi-Planar Bulk CMOS Technology

A. Optimized MOSFET Performance

Quasi-planar bulk CMOSFET designs were optimized for gate length $L_G = 25$ nm and transistor width $W_{\rm STRIPE} = 30$ nm, using 3-D device simulations, to achieve the highest on-state drive current $(I_{\rm ON})$ for an OFF-state leakage current $(I_{\rm OFF})$ no greater than 3 nA/μm, effective oxide thickness (EOT) $T_{\rm ox} = 9$ Å and $V_{DD} = 1$ V; electrical channel length (which is defined as the distance between the points where the source/drain extension (SDE) doping profiles fall to 2×10^{19} cm^{-3}) $L_{\rm eff} = 27$ nm for NMOS and 28 nm for PMOS; SDE junction depth $X_{J,\rm EXT} = 10$ nm; deep source/drain junction depth $X_{J,S/D} = 28$ nm; STI oxide recess depth

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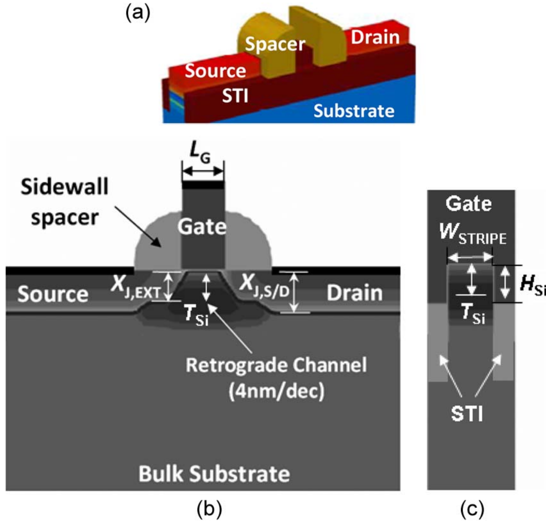

Fig. 1. (a) Bird's eye view of a quasi-planar bulk MOSFET (gate electrode not shown to allow channel region to be seen) and its cross-sectional views (b) along and (c) across the channel.

$(H_{\mathrm{si}}) = 10$ nm; and near-band-edge gate work-functions (WFs) $\Phi_M = 4.2$ eV for NMOS and 5.1 eV for PMOS. The retrograde channel doping profile is assumed to have a gradient of 4 nm/dec and peak doping concentration $(N_{\mathrm{peak}}) = 10^{19}$ cm^{-3} at a depth T_{si} below the top channel surface; the SDE doping profile is assumed to have a steep lateral gradient of 2 nm/dec. Steep retrograde doping profiles have been achieved in practice via selective epitaxial growth of the lightly doped (or undoped) channel region [21]–[26] or by utilizing diffusion-barrier layers [27]. The same design parameter values are assumed for the planar bulk MOSFET design, except that $\Phi_M = 4.08$ eV for NMOS and 5.2 eV for PMOS to yield similar nominal values of saturation threshold voltage as their quasi-planar counterparts.

Fig. 2 shows the transfer characteristics (I_{DS} versus V_{GS}) for the optimized quasi-planar bulk and planar bulk MOSFET structures, with $H_{\mathrm{si}} = 10$ nm. The quasi-planar bulk devices exhibit steeper subthreshold slopes due to better capacitive coupling between the gate and the channel region. A summary comparison of device performance parameters is given in Table I. These simulation results are consistent with recently reported experimental results [20] for devices that have worse electrostatic integrity (e.g., DIBL > 100 mV/dec), which have shown that quasi-planar bulk MOSFETs achieve higher I_{ON} at comparable I_{OFF} (and have lower V_{TH} variation), compared with conventional planar bulk MOSFETs, so that they provide for improved SRAM yield. In this paper, the planar bulk MOSFET design is optimized with very shallow SDE junction depths [28] to achieve very good electrostatic integrity, i.e., DIBL < 50 mV/V, to present the best-case scenario against which to compare the quasi-planar bulk MOSFET design.

An analytical I–V model for the short-channel MOSFET [15] was fit to the simulated current-versus-voltage characteristics. This model can be used to estimate SRAM performance metrics such as read static noise margin (SNM) [29], [31], static write margin expressed through the write-ability current (I_w) [30], [31], and read current. It is used in this work to estimate SRAM cell yield following the methodology described in [32].

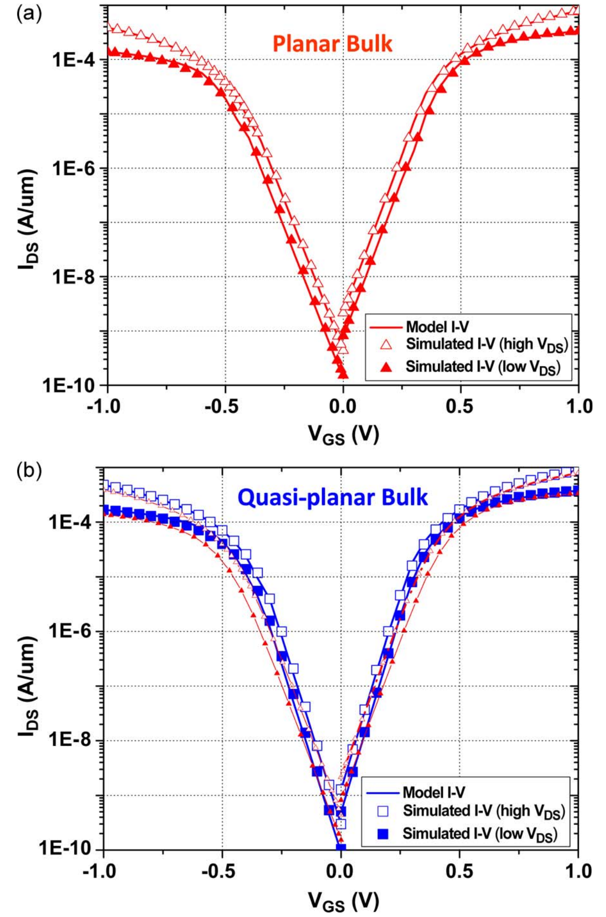

Fig. 2. Simulated transfer characteristics for (a) planar bulk and (b) quasi-planar bulk MOSFETs. To facilitate a direct comparison, the curves from (a) are overlaid in (b). The current is normalized to $W_{\mathrm{STRIPE}} + 2 \times H_{\mathrm{si}}$.

TABLE I
SUMMARY OF TRANSISTOR PERFORMANCE PARAMETERS. THE ON/OFF CURRENTS ARE NORMALIZED TO $W_{\mathrm{STRIPE}} + 2 \times H_{\mathrm{si}}$.

V_{DD} = 1.0V	Quasi-planar bulk		Planar bulk	
	N-type	P-type	N-type	P-type
I_{ON} [µA/µm]	884	476	786	386
I_{OFF} [nA/µm]	1.3	0.30	2.2	0.44
SS [mV/dec]	69	71	85	88
$\|V_{TH,LIN}\|$ [V]	0.16	0.21	0.17	0.25
$\|V_{TH,SAT}\|$ [V]	0.13	0.18	0.13	0.21
DIBL [mV/V]	33	37	44	46
L_{eff} [nm]	27	28	27	28

B. Impact of Variations

The impact of variations on transistor performance was studied via 3-D device simulations using realistic gate-electrode profiles and atomistic doping. Gate LER was simulated by

sampling line-edge profiles from a scanning electron microscopy image of photoresist lines printed for the 22-nm node. This represents the worst-case scenario since the LER of a patterned gate electrode generally is less severe than that of the resist line used to define it. In addition, the SDE junction lateral profiles are assumed to have the same LER as the gate electrode, so that L_{eff} will have the same roughness profile as L_G. In this manner, gate-LER-induced variations in V_{TH} (i.e., $\sigma(V_{\text{TH}})|_{\text{gate-LER}}$) were found to be $= 31$ mV for the planar bulk MOSFET and 16 mV for the quasi-planar bulk MOSFET with $W_{\text{STRIPE}}/L_G = 30$ nm/25 nm.

Since the quasi-planar bulk MOSFET structure is an evolutionary form of the conventional planar bulk MOSFET structure [18]—in contrast to the vertical FinFET/MuGFET structure—it can be reasonably expected that gate-LER-induced variation for a quasi-planar bulk MOSFET would be very similar to that for a conventional planar bulk MOSFET. To verify this, LER-induced V_{TH} variation for the various device architectures was compared: it was found that, for the high-aspect-ratio FinFET/MuGFET, LER-induced V_{TH} variation increases with decreasing correlation length due to increased misalignment between the front and back gates [33]; in contrast, for the low-aspect-ratio quasi-planar MOSFET and conventional planar MOSFET, LER-induced V_{TH} variation decreases with decreasing correlation length due to an averaging effect.

The methodology proposed by Sano [34], wherein only the long-range Coulomb potential for an ionized dopant atom is considered to avoid unrealistic singularities in potential profile, was used to simulate the effect of RDF for each of the gate-electrode profile cases. Details are described in [35], and only the results are summarized here: $\sigma(V_{\text{TH}})|_{\text{RDF}} = 54$ mV for the planar bulk MOSFET and 30 mV for the quasi-planar bulk MOSFET with $W_{\text{STRIPE}}/L_G = 30$ nm/25 nm.

Fig. 3(a) shows the distributions of saturation V_{TH} (i.e., the value of V_{GS} corresponding to 100 nA/μm for $V_{DS} = 1$ V) obtained from the simulated I_{DS}–V_{GS} curves (200 cases) for each device structure. The standard deviation of V_{TH} variation ($\sigma(V_{\text{TH}})$) for the quasi-planar device is smaller than that for the planar device. This is due to reduced short-channel effects (SCEs) in the quasi-planar device and the fact that it has $\sim 1.6\times$ larger effective channel width W_{eff} (based on linear I_{DS} values) but only slightly greater depletion charge [35].

Fig. 3(b) compares the V_{TH} mismatch, which is gauged by the Pelgrom coefficient (A_{VT}) [36], for the simulated devices in this work against that of experimental devices reported in the literature. It can be seen that A_{VT} for the planar bulk device design in this work follows the trend for planar bulk technologies. A_{VT} of the quasi-planar bulk device design is improved to be slightly worse than A_{VT} for reported ultra-thin-body MOSFET technologies.

The impact of gate WF variations (WFVs) cannot be neglected for nanometer-scale MOSFETs with metal/high-k gate stacks. In this paper, WFV-induced $\sigma(V_{\text{TH}})$ is estimated based on [37]. It is well known that the WF of the gate material close to (within a few monolayers of) the gate–dielectric interface affects V_{TH}. The composition, average grain size, and crystalline orientation ("texture") of this material each can affect the WF value and may depend on the gate dielectric material. For a

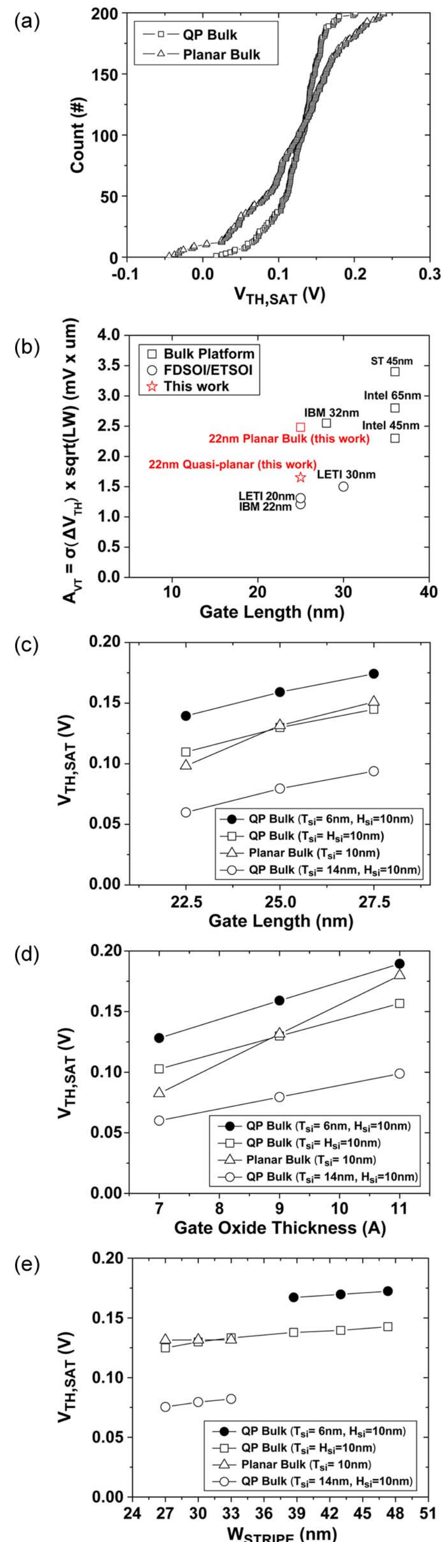

Fig. 3. Simulated saturation threshold voltage ($V_{\text{TH,SAT}}$) for planar bulk versus quasi-planar bulk MOSFETs. (a) Distribution of $V_{\text{TH,SAT}}$ caused by gate-LER and RDF (for $W_{\text{STRIPE}}/L_G = 30$ nm/25 nm), from which $\sigma(V_{\text{TH,SAT}}|_{\text{PlanarBulk}}) = 61.6$ mV and $\sigma(V_{\text{TH,SAT}}|_{\text{QPBulk}}) = 33.1$ mV. (b) Comparison of Pelgrom coefficients for simulated versus experimental reported devices. (c) $V_{\text{TH,SAT}}$ versus L_G. (d) $V_{\text{TH,SAT}}$ versus T_{ox}. (e) $V_{\text{TH,SAT}}$ versus W_{STRIPE}. Note that the quasi-planar bulk MOSFET shows less sensitivity to variations in gate length (L_G) and gate-oxide thickness (T_{ox}) and that the depth of the retrograde channel doping profile (T_{si}) can be used to tune the threshold voltage without impacting short-channel control. The quasi-planar bulk MOSFET shows more sensitivity to variations in transistor width if W_{STRIPE} is small (30 nm).

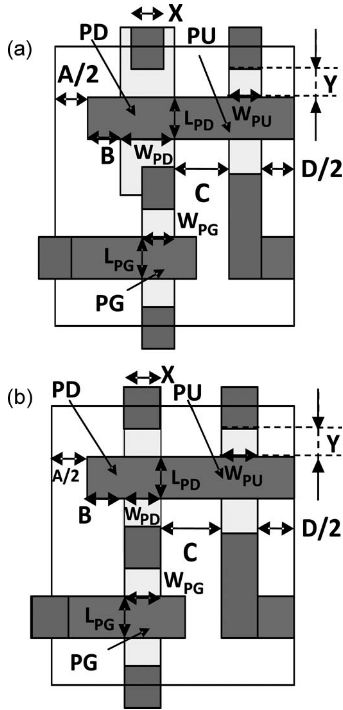

Fig. 4. Half-bit cell layouts for (a) notched and (b) notchless SRAM cell designs.

TABLE II
22-nm-NODE 6-T SRAM CELL LAYOUT PARAMETERS FOR PLANAR BULK AND QUASI-PLANAR BULK CMOS TECHNOLOGIES

Design rules		Symbol	Size [nm]
Cell Height	PG CH length	L_{PG}	25
	PD CH length	L_{PD}	25
	CONT size	X	30
	Gate-to-CONT	Y	20
	Total	190	
Cell Width	POLY-to-POLY	A	30
	POLY-to-DIF ext	B	20
	PD Width	W_{PD}	55 / 30 / 43
	PG width	W_{PG}	30 / 30 / 43
	PU width	W_{PU}	30 / 30 / 43
	N/P isolation	C	50
	DIF-DIF (min)	D	50
	H_{si} for quasi-planar	H_{si}	10
	Total	390 / 340 / 392	
A SRAM cell area		0.0741 / 0.0646 / 0.0745 μm^2	

conformal chemical vapor deposition process (used to deposit the metal gate layer that affects V_{TH}), the properties of these materials are substantially the same for a horizontal surface as for a vertical surface. Thus, metal–gate WFV observed for nonplanar transistor structures as in [37] can be reasonably expected to be observed in more planar transistor structures. In this paper, $\sigma(V_{\mathrm{TH}})|_{\mathrm{WFV}}$ is assumed to be negligible for the planar bulk MOSFET (poly-Si gate: Fermi-level pinned

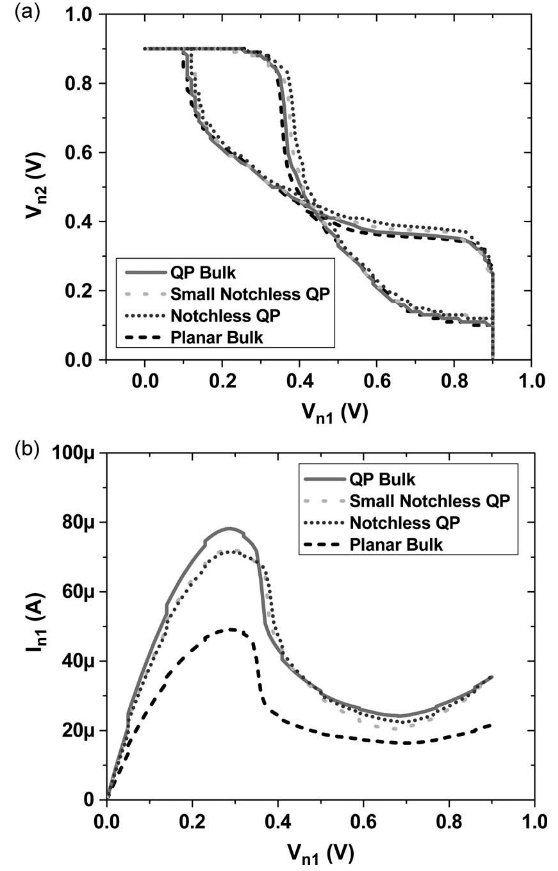

Fig. 5. Three-dimensional 6-T SRAM cell simulation results for the planar bulk, quasi-planar bulk, and notchless quasi-planar bulk SRAM cells. (a) Butterfly curves. (b) Write-N-curves.

near to the band edge [38]) and 12.4 mV for the quasi-planar bulk MOSFET, again to provide a best-case scenario against which to compare the quasi-planar bulk MOSFET design. Assuming that the variations due to gate-LER, RDF, and WFV are statistically independent [38], the total standard deviation of V_{TH} variation due to random variations is calculated using the following:

$$\sigma(V_{\mathrm{TH}})|_{\mathrm{Total,random}} \approx \sqrt{\sigma(V_{\mathrm{TH}})^2|_{\mathrm{gate-LER}} + \sigma(V_{\mathrm{TH}})^2|_{\mathrm{RDF}} + \sigma(V_{\mathrm{TH}})^2|_{\mathrm{WFV}}}. \tag{1}$$

(The effects of gate-LER and RDF were previously found to be independent for the planar bulk MOSFET structure, as well as the quasi-planar bulk MOSFET structure [15], [20], [38].)

The impacts of variations (±10%) in L_G, EOT, and W_{STRIPE} are shown in Figs. 3(c)–(e), respectively. The SCE is better suppressed in the quasi-planar bulk MOSFET, due to improved gate control. (This benefit is equivalent to > 6 Å reduction in T_{ox}.) In addition, variations in T_{ox} have less impact for the quasi-planar bulk MOSFET. The quasi-planar bulk MOSFET shows a stronger reverse-narrow-width effect, but it is still less than 10 mV for 10% variation in W_{STRIPE}.

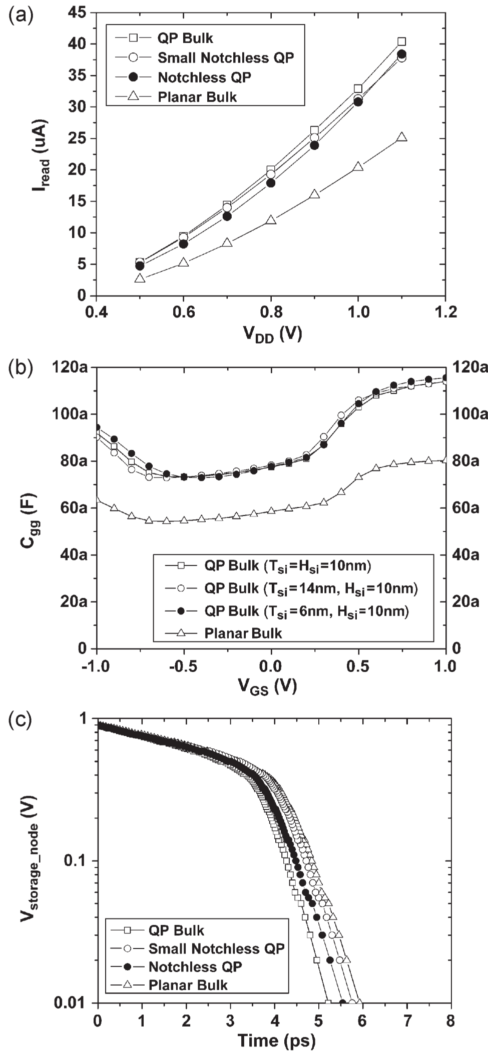

Fig. 6. (a) SRAM cell read current. (b) PD device gate capacitance. (c) Pseudo-transient simulation of the storage-node voltage during a write operation.

III. 6-T SRAM CELL DESIGNS

Layout parameters for 22-nm 6-T SRAM cells (Fig. 4) were selected based on recent publications [1]–[5] and are summarized in Table II. Nominal SNM and I_W values were obtained via 3-D simulations of full cell structures using advanced physical models including the density-gradient/drift-diffusion transport model and the phenomenological van Dort quantum correction model to account for energy quantization in the channel regions.

In a conventional SRAM cell layout [Fig. 4(a)], the width of the NMOS pull-down (PD) device is larger than the width of the NMOS pass-gate (PG) device to achieve a cell beta ratio greater than 1 for sufficient nominal SNM. As a result, the NMOS active area pattern is notched. Due to limitations of optical lithography, the corners of the active area will be rounded in practice, so that (vertical) misalignment between the gate layer and the active layer results in asymmetric variations in NMOS device width (i.e., mismatch) between the left and right sides of the cell, which can significantly degrade SNM [39].

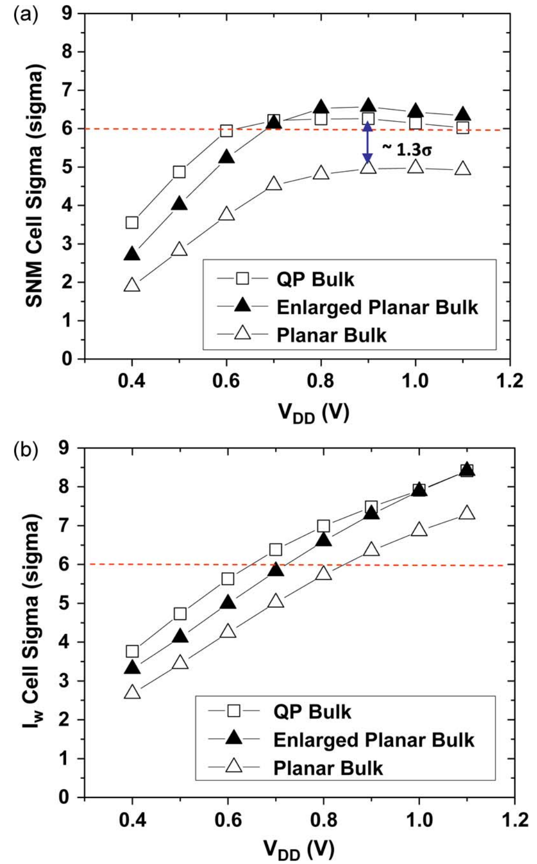

Fig. 7. SRAM cell sigma comparisons for (a) SNM and (b) I_W.

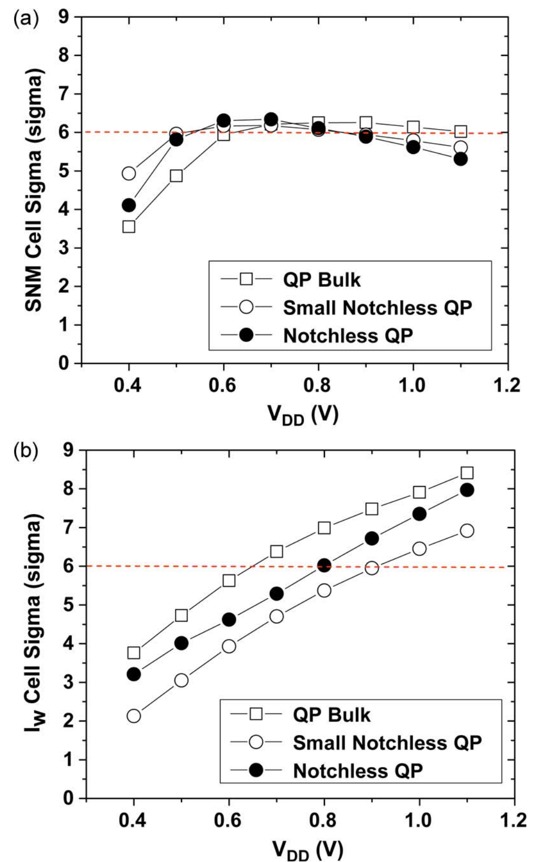

Fig. 8. SRAM cell sigma comparisons for (a) SNM and (b) I_W.

TABLE III
COMPARISON OF PROJECTED PERFORMANCE METRICS AND CELL AREAS FOR PLANAR BULK AND QUASI-PLANAR BULK SRAM CELLS AT $V_{DD} = 0.9$ V.

Technology	SNM [mV]	I_w [μA]	Cell area [μm^2]	$P_{standby}$ per bit [nW]
Planar Bulk	180.5	16.4	0.0741	0.218
Quasi-planar Bulk	183.5	24.1	0.0741	0.186
Small Notchless Quasi-planar Bulk (W_{STRIPE} = 30nm, T_{si} for PD/PG/PU = 14/10/14nm, H_{si} = 10nm)	175.6	20.5	0.0646	0.351
Notchless Quasi-planar Bulk (W_{STRIPE} = 43nm, T_{si} for PD/PG/PU = 10/6/10nm, H_{si} = 10nm)	182.7	22.3	0.0745	0.107

An advantage of the quasi-planar bulk MOSFET design is that it allows for V_{TH} to be adjusted by tuning the depth (T_{si})—rather than the dose (N_{peak})—of the retrograde channel doping profile, without increasing either SCEs or V_{TH} variation [35]. (Note that fringing electric fields through the isolation oxide allow good gate control to be maintained, even if T_{si} is slightly larger than H_{si}.) This remarkable feature can be exploited to tune the SRAM cell beta ratio by adjusting transistor V_{TH} values rather than transistor widths, so that a notchless active area pattern [Fig. 4(b)] can be used. A notchless cell design can provide for area savings as well as reduced variation in NMOS device width resulting from lithographic misalignment, due to improved printability of the active area pattern.

To achieve sufficient SNM with a notchless quasi-planar SRAM cell design, the NMOS PD and PMOS pull-up (PU) devices should have lower V_{TH} values than the NMOS PG device. This is achieved with a deeper retrograde channel doping profile [ref. Figs. 3(c)–(e)], which could be achieved in practice by using a higher ion-implantation energy. Note that H_{si} is constrained to be the same for all of the devices in a quasi-planar SRAM cell for ease of manufacture, i.e., the isolation oxide is uniformly recessed (e.g., by using a timed etch in dilute hydrofluoric acid solution or by elevating the channel with a selective epitaxial growth process) prior to gate-stack formation[1] Furthermore, note that the transistor widths (W_{PU}, W_{PD}, and W_{PG}) are constrained to be equal in a notchless cell design to be compatible with a regularly corrugated starting substrate [40] for improved active-area width control.

As can be seen from Fig. 5, the small notchless quasi-planar SRAM cell achieves comparable SNM and superior write-ability, compared against a conventional notched planar SRAM cell. Significantly larger read current is offered by the quasi-planar SRAM cell designs across a wide range of V_{DD} [Fig. 6(a)]. Although gate capacitance is also higher for the quasi-planar SRAM cell designs [Fig. 6(b)], simulations of the storage-node transient voltage during a write operation [Fig. 6(c)] show that the write time is still shorter for the quasi-planar SRAM cell designs.

Table III summarizes the projected cell performance metrics and cell area values for the planar and quasi-planar SRAM cells. Since V_{TH} is lower for the PD and PU devices in the small notchless quasi-planar cell, it has higher standby power consumption (P_{standby}) than the planar (notched) cell. P_{standby} can be lowered by increasing V_{TH} for all of the transistors in the notchless quasi-planar cell, but then, the transistors must be widened to maintain a comparable level of performance and yield, i.e., there would be no area savings in comparison with the notched cell design. The devices in an optimized notchless quasi-planar cell design have shallower retrograde channel doping depths of 10/6/10 nm for PD/PG/PU and widths of 43 nm.

IV. SRAM YIELD ESTIMATION

In the previous section, the quasi-planar bulk SRAM cell designs were shown to have improved static performance (i.e., better read stability and write-ability current) and better transient performance (i.e., shorter write time). In this section, the corresponding improvement in cell yield is evaluated using the concept of cell sigma, which is defined as the minimum amount of variation for read/write failure [32]. (If an SRAM cell read/write metric has a Gaussian distribution, its cell sigma is simply its mean value divided by its standard deviation.) Random variations due to gate-LER, RDF, and WFV, as well as global variations due to process-induced variations (Gaussian with 3 sigma corresponding to ±10%) in gate length, stripe width, gate oxide thickness, and channel stripe height (H_{si}) are considered together in estimating the cell sigma. Although $\sigma(V_{\mathrm{TH,LIN}})$ is generally smaller than $\sigma(V_{\mathrm{TH,SAT}})$, the worst-case scenario $\sigma(V_{\mathrm{TH,LIN}}) = \sigma(V_{\mathrm{TH,SAT}})$ is assumed herein. Six-sigma (6σ) yield is required for large SRAM arrays to be functional, i.e., no more than one bit cell can fail out of 505 million bit cells to achieve sufficiently high chip yields.

A. Iso-Area and Iso-Yield Comparisons Between Planar and Quasi-Planar Bulk Cell Designs

As shown in Fig. 7, the SNM cell sigma for the quasi-planar cell is ~6.3 at $V_{DD} = 0.9$ V, which is a 1.3-sigma improvement

[1] The quasi-planar bulk MOSFET structure is robust to H_{si} variation by design [41], so that H_{si} adjustment is not an effective means for adjusting the cell beta ratio of a quasi-planar SRAM cell. This is in contrast to a high-aspect-ratio FinFET whose drive current varies directly with H_{si}, so that H_{si} adjustment can be used to adjust the cell beta ratio of a FinFET SRAM cell [2].

over the planar cell. This yield enhancement can be attributed primarily to lower V_{TH} variation for the quasi-planar MOSFET structure. The minimum V_{DD} that meets the six-sigma yield requirement for both SNM and I_W is ~0.65 V for the quasi-planar cell. In stark contrast, the six-sigma yield requirement cannot be met by the planar cell for any value of V_{DD}; it achieves only ~5 SNM cell sigma at $V_{DD} = 0.9$ V.

In order for the planar cell to have read and write yields comparable to those of the quasi-planar cell, the widths of the PD, PG and PU transistors must be increased to 110, 65, and 65 nm, respectively. The planar cell area must therefore be enlarged to $\sim 0.1\ \mu\mathrm{m}^2$ by ~46%. In other words, the area savings offered by the quasi-planar cell design is ~32%.

B. Notchless Quasi-Planar Bulk SRAM Cell Yield

As can be seen from Fig. 8, the notchless quasi-planar cell can meet the 6-sigma yield requirements for V_{DD} down to ~0.8 V, with comparable cell area and faster write time, compared to the conventional planar cell [see Fig. 6(c)]. The small notchless quasi-planar cell (with ~13% smaller area) is projected to meet the 6-sigma cell yield requirement for V_{DD} down to ~0.9 V.

V. Conclusion

Compared with a planar bulk MOSFET, the quasi-planar bulk MOSFET provides for larger drive current and reduced V_{TH} variation, due to improved gate control. As a result, quasi-planar bulk SRAM cells have been projected to have enhanced write-ability current and faster write time for comparable read stability, as well as > 1 sigma improvement in cell yield. A notchless quasi-planar bulk SRAM cell design has been proposed for improved lithographic printability and either smaller area or lower standby power, and has been projected to achieve 6-sigma cell yields at operating voltages down to ~0.8 V.

Although the height (H_{si}) of the quasi-planar bulk MOSFET can be made taller to increase its layout area efficiency, this would require a concomitant reduction in Si width for adequate suppression of SCEs. In general, low-aspect-ratio (short and wide) features are preferred for ease of manufacture and design flexibility (i.e., to allow for finer increments in designed W_{eff}). On the other hand, if H_{si} were very short, the benefit of the quasi-planar bulk structure would be diminished. For example, if H_{si} is only 5 nm, the minimum operating voltage (for 6-sigma cell yield) for the notched quasi-planar SRAM cell is ~0.9 V. Thus, the value of $H_{\mathrm{si}} = 10$ nm chosen in this work represents a good tradeoff between manufacturability and performance/scalability.

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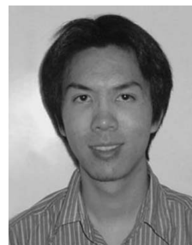

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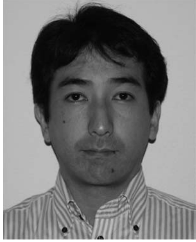

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