Technology Variability From a Design Perspective

Borivoje Nikolić, *Senior Member, IEEE*, Ji-Hoon Park, *Student Member, IEEE*, Jaehwa Kwak, *Student Member, IEEE*, Bastien Giraud, Zheng Guo, *Member, IEEE*, Liang-Teck Pang, Seng Oon Toh, *Student Member, IEEE*, Ruzica Jevtić, *Member, IEEE*, Kun Qian, *Student Member, IEEE*, and Costas Spanos, *Fellow, IEEE*

***Abstract*—Increased variability in semiconductor process technology and devices requires added margins in the design to guarantee the desired yield. Variability is characterized with respect to the distribution of its components, its spatial and temporal characteristics and its impact on specific circuit topologies. Approaches to variability characterization and modeling for digital logic and SRAM are analyzed in this paper. Transistor arrays and ring oscillator arrays are designed to isolate specific systematic and random variability components in the design. Distributions of SRAM design margins are measured by using padded-out cells and observing minimum array operating voltages. Correlations between various components of variability are essential for adding appropriate margins to the design.**

***Index Terms*—CMOS, digital logic, SRAM, static timing analysis, variability.**

I. Introduction

INCREASING process variability is perceived as one of the major roadblocks for continued technology scaling [1]. In sub-100 nm technologies, it is becoming increasingly difficult for the device tolerances to track the scaling rate of the minimum feature sizes. Device performance varies in space and in time. Variations are generally characterized as within-die (WID), die-to-die (D2D), and wafer-to-wafer (W2W) [2]. While the W2W variations dominated in the past, with scaling of the technology, WID and D2D variations can occupy a majority of the process spread. Variation of process and device parameters can be systematic or random, spatially or temporally correlated. Sources of variability are in the transistors, interconnect, and in the operating environment (supply and temperature) [3]. Device parameters vary systematically because of deviations in nominal widths, lengths, film thicknesses, and dose of implants due to the manufacturing process [4]. Random device parameter fluctuations are associated with atomistic variations in device structure.

Simultaneously, with process scaling, the nature of IC design has gradually shifted to become power limited. In current and future technology nodes, the optimization for energy consumption is as important as optimization for performance [5]. To sustain the current trend in technology scaling, which dictates higher parallelism in each technology generation, optimization for energy requires further lowering of the supply voltages. However, to mitigate the impact of increased variability, appropriate design margins have to be added to every component of an integrated circuit. In addition, the sensitivity of power and performance to process variations increases at low supply voltages. Therefore, the requirements for robust operation often contradict the needs for energy efficiency, and this is exacerbated by variability.

This paper reviews various classes of technology variability, analyzes their interactions, and presents methods for their accounting in the design margins. Characterization of variability is essential for setting the appropriate design margins. Numerous characterization structures have been developed that allow for collection of large datasets of process and device parameters, as well as their spatial and temporal characteristics and correlations. Structures for characterizing digital gates and SRAM have been designed to generate large datasets suitable for evaluating the distributions of device parameters and their impact on circuit yield. Characterization of variability allows for adding appropriate margins to the design, as reviewed on the examples of digital logic and memory.

II. Technology Variability

There are many sources of variability in the design and numerous ways to classify them. The primary sources of variability are the transistors, the interconnect, supply, and temperature.

CMOS process parameter variability is often classified into three categories: known systematic, known random, and unknown [6]. Systematic process variations are deterministic shifts in space and time of process parameters, whereas random variations change the performance of any individual instance in the design in an arbitrary way. Systematic variations are, in general, spatially correlated. In practice, although many of the systematic variations have a deterministic source, they are either not known at the design time, or are too complex to model, and are thus treated as random. As a result, many of the sources of variability are not modeled in the design kits and have to be treated as random in the design process. The resulting "random" variation component, depending on the way systematic variability is modeled, will often appear to have a varying degree of spatial correlation [7].

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B. Nikolić, J.-H. Park, J. Kwak, S. O. Toh, R. Jevtić, K. Qian, and C. Spanos are with the Department of Electrical Engineering and computer Sciences, University of California, Berkeley, CA 94720-1770 USA.

B. Giraud is with CEA-Leti, 38000 Grenoble, France.

Z. Guo is with Intel Corp, Hillsboro, OR 97124 USA.

L.-T. Pang is with IBM T. J. Watson Center, Yorktown Heights, NY 10598 USA.

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Spatial variations in the manufacturing process are classified as WID, D2D, W2W, and lot-to-lot (L2L) [2]. Variations reflect both the spatial as well as the temporal characteristics of the process and cause different dies and wafers to have different properties. The performance of the manufacturing equipment, expressed through the dose, speed, vibration, focus, or temperature, varies within one die and from die to die. Those parameters that vary rapidly over distances smaller than the dimension of a die result in WID variations whereas variations that change gradually over the wafer will cause D2D variations. Similarly, even more parameters vary from wafer to wafer (W2W variations) and between different manufacturing runs (L2L variations).

Many sources of systematic spatial variability can be attributed to the different steps of the manufacturing process. The photolithography and etching steps contribute significantly to variations in nominal lengths and widths due to the complexity required to fabricate sublithographic lines that are much narrower than the wavelength of light used to print them [8]. Significant contributors in this area include temperature nonuniformities in the critical postexposure bake (PEB) and etch steps. Variation in film thicknesses (e.g., oxide thickness, gate stacks, wire, and dielectric layer height) is due to the deposition and growth process, as well as the chemical-mechanical planarization (CMP) step. Additional electrical properties of CMOS devices are affected by variations in the dosage of implants, as well as the temperature of annealing steps. In recent technologies, overlay error, mask error, shift in wafer scan speed, rapid thermal anneal, and the dependence of stress and proximity on layout have become notable sources of systematic variations.

Random device parameter fluctuations stem mainly from line-edge roughness (LER) [9], Si/SiO_2 and polysilicon (poly-Si) interface roughness [10], and random dopant fluctuations (RDF) [11]. Impact of random sources of variability increases with reduced device dimensions. RDF increases proportionally to the square root of $1/WL$, where the W is the transistor width and the L is the transistor length.

The operating environment of the devices on a chip spatially varies as well. Global variations in the supply voltage as well as variations in the local supply grid directly affect the CMOS gate delays, presenting sources of spatially correlated variability. Operating temperature varies, both globally and locally, thus adding another spatially correlated component of performance variability.

Device parameters are also variable in time, during the design process or during the chip lifetime. Variations in time include intentional and random changes in the manufacturing process, time-dependent degradation in transistor parameters, and changes in supply and temperature [3]. Time-dependent degradation in transistor performance, particularly due to bias temperature instability (BTI), is a major concern in recent technology nodes. Negative BTI (NBTI) is caused by trapping of the carriers in the PMOS gate interfaces under high biases, which causes threshold increase and degraded current. BTI, which only affected PMOS transistors in Si-O_2 gate stacks, now affects both NMOS and PMOS transistors in high-K metal gate devices [12].

Random telegraph signal (RTS) noise is another time-dependent source of variability that is becoming a significant concern in design with highly scaled transistors. Its magnitude is inversely proportional to the device channel area, WL. It is estimated that Vth fluctuation due to RTS will exceed Vth variation due to RDF at 3 sigma levels at the 22 nm technology node [13].

Chip yield is the probability that a chip is both functional and meets the parametric constraints, such as timing and power. A circuit with more design margin will have a higher yield, as it will be more immune to variability. The challenge is in finding the smallest margin necessary for the required yield so that performance is not overly constrained, which would result in large power overhead. The appropriate design margin generally depends on the type of design, circuit style, its function and use, and will be discussed throughout the paper. The remainder of this paper focuses on the variability impact on combinatorial logic, sequential logic and embedded static random access memory (SRAM), as three distinct digital circuit styles that require different margins.

III. Variability Characterization in Space and Time

In order to incorporate variability in the design, it is necessary to characterize it. Technology variability is characterized during the technology development phase and is continuously monitored during the manufacturing process. Conventional test structures focus on the extraction of the I-V and C-V characteristics of the devices and the interconnect for model corners, while a simple subset of structures is placed in the wafer's scribe lines for continuous process monitoring.

The measured device data is commonly fitted to a compact (SPICE) model and some aspects of variability are captured in the statistics of the model parameters. This information is used to generate process corners and perform Monte Carlo simulations or statistical timing analysis of the circuits. However, it does not consider the spatial correlation of devices and typically does not differentiate between within-die and die-to-die variations. Furthermore, systematic variations due to strain, proximity effects, and time-dependent variations such as BTI and RTS noise are not well modeled and are treated as random. All this leads to overly conservative design margins in advanced processes.

Characterizing more details of variability using suitable test structures allows designers to reduce margins for systematic variations and, with the help of statistical timing and optimization tools, use the right amount of margin to obtain an optimal design that maximizes performance, power, and yield.

Device arrays spread over a large chip area with fine spatial resolution provide information on within-die statistics and spatial correlation. Measuring many chips from several wafers and wafer-lots provides die-to-die variability information [14], [15]. Tracking the location of the measured devices with respect to the chip, the reticle and the wafer provide a means of locating systematic variation in the manufacturing process, allowing the foundry to correct the variation or, allowing designers to absorb the impact of the variation in the design. Averaging the data for an array of devices during the measurements suppresses random variation and exposes systematic effects.

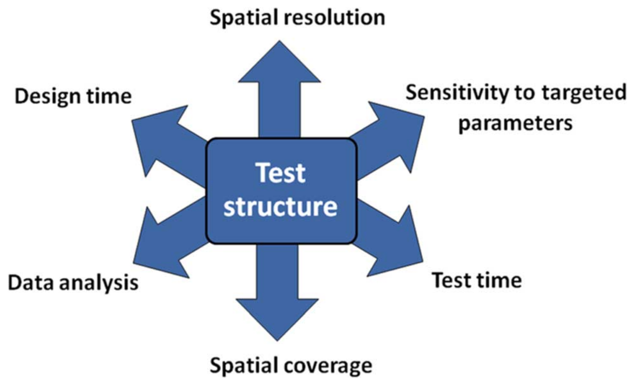


Fig. 1. Trade-offs in test structure design.

A. Logic Characterization

The design of logic characterization structures faces several trade-offs, some of which are illustrated in Fig. 1: spatial resolution versus spatial coverage, the ease of data analysis versus the sensitivity to the desired parameter or the design complexity versus the test time.

Four types of measurement structures are being used in practice: 1) direct measurements of resistances and capacitances [16], [17]; 2) I-V device measurements [20]–[22]; 3) ring oscillators [18], [19]; and 4) functional blocks [23].

Regardless of the test structure, particular schematic designs and layouts of the devices under test can be targeted to explore the impact of processing, such as gate patterning, or circuit topology [4], [15], [24]–[26].

A common method for characterizing transistor variability consists of measuring the current of individual transistors in an array. Direct measurements of resistances, capacitances and I-V characteristics provide the distributions of desired values, but both the stimuli and the measurements are analog, resulting in long test times and limited datasets.

I-V characteristics of larger transistor arrays can be collected using device matrix arrays (DMAs), where many transistors can have drains and sources connected to a single bus, while the gate voltages are externally swept, shown in Fig. 2 [20], [27]. This structure provides a large flexibility in analyzing each device's characteristics and spatial device correlations. The limitation of the structure is in the accuracy of subthreshold current measurements because of many devices that share the same line. In addition, an array of transistors can be formed with its terminals multiplexed to address the measurement nodes of individual devices under test. In this setup, drain currents can be measured with reasonable speed and accuracy. Measurement of gate leakage and subthreshold current requires very sensitive measurements to distinguish small currents or very large devices to generate bigger currents. Parasitic currents need to be removed with calibration and random noise can be reduced by averaging the measurement over time. Using larger devices to get more current is a compromise with having a finer spatial resolution.

On the other hand, variability characterization using ring oscillators (ROs) is commonly performed for high characterization speed and simple frequency measurements [28]. Variation in the frequency of the ROs is related to variation of device parameters that affect transistor switching speed and capacitive

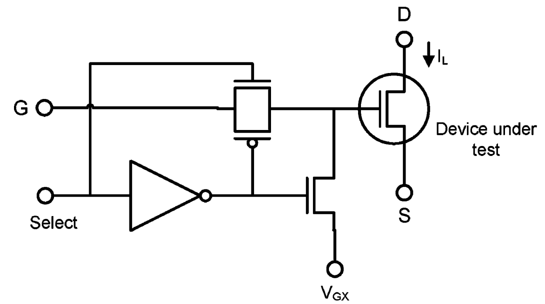


Fig. 2. Instance of the device under test in the DMA structure.

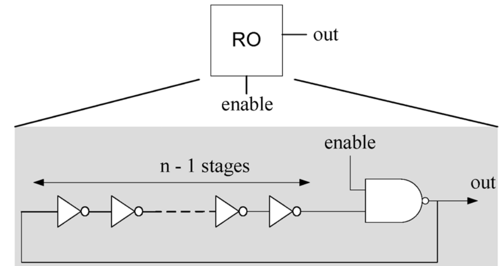


Fig. 3. A simple ring-oscillator structure.

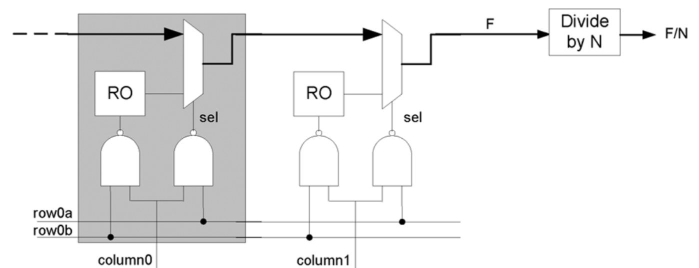


Fig. 4. An addressable array of RO. The local RO frequency is divided down and measured off-chip.

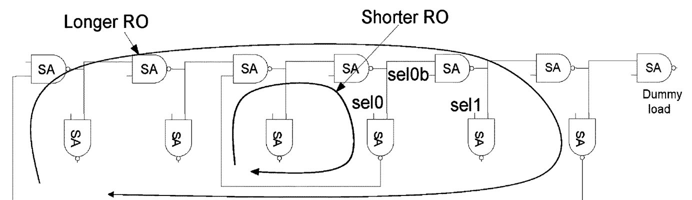


Fig. 5. Variable-length ring oscillator.

load. RO test structures are constructed by using inverting gates such as inverters or NAND/NOR gates, Fig. 3. An array of ROs can be addressed and individual RO frequency can be divided down and measured off-chip, Fig. 4. Measurement of large RO arrays, therefore, can be performed in a fast, accurate and automated manner.

Since a RO averages the gate delays, spatial resolution of variability is limited to the spacing between them. This essentially averages random variation over the RO: the longer the RO the less observable is the local random component of variation. Nevertheless, this method measures the variability of the switching speeds of a gate with a spatial resolution that is smaller than the logic depth of most datapaths.

Designing gates to be more sensitive to a certain process parameter can help correlate the RO frequency variation with that parameter. Differential measurements of two structures that are identical in all aspects except for a certain layout parameter can

be used to isolate particular effects. This has been successfully employed to measure the impact of layout on transistor performance [15], [4] and in the measurement of the effects of NBTI [29]. It has been effective in isolating the effects of lithography on the effective channel length, gate proximity, impact on density and diffusion length on strain and STI-induced stress. Similarly, layouts can be sensitized to measure the impact of processing, such as defocus or misalignment [56].

Making electrical measurements of the same structure under different environmental conditions can help to estimate process parameter variation. For example, by measuring the subthreshold current and RO frequency at different temperatures, supply and back-bias voltages, the variation of the main process parameters responsible for systematic variations can be extracted. The same technique has been used to reveal the impact of strain and proximity on device properties.

B. Characterization of Gate Delays

Ring oscillators efficiently characterize systematic variations, but average out random, spatially uncorrelated effects. A simple concept of variable-length ring oscillators [30], can measure the delay of a pair of gates, and reduce the effect of averaging without compromising the speed and convenience of the method. This is accomplished by measuring the frequency differences between differently configured ring oscillators in [26].

Ring oscillators can be modified to allow for multiplexing in individual delay elements for delay characterization of individual gates [31].

The idea for characterizing individual delays through path differences has been used for on-chip measurements of flip-flop setup times and clock-to-output delays. Individual direct delay measurements have been performed for flip-flop setup and clock-output delays [32]. By placing appropriately configured flip-flops into ring-oscillator configurations, variations in the setup times and clock-to-output delays can be measured as well [33].

C. SRAM Characterization

The use of regular layouts has allowed aggressive scaling of SRAM transistors compared to combinational logic. Simultaneously, these highly scaled devices with design rules relaxed compared to digital logic tend to exhibit higher sensitivities to systematic effects in addition to increased random variation. Systematic effects that affect SRAM have been attributed to temperature nonuniformities during annealing, STI-induced stress, and process-induced cell asymmetry [34]. Increased variability with technology scaling has a large negative impact on SRAM design. SRAM cells use the smallest transistors available, and therefore are susceptible to largest amounts of random variability, while the technology scaling enables integration of twice as many cells in each new process generation. As a result, it is becoming necessary to satisfy the design where the functionality of the cell is guaranteed more than seven standard deviations away from the mean, while the standard deviations in threshold voltages are increasing. Therefore, SRAM variability characterization over a wide range of process parameters presents a particular challenge. SRAM yield is

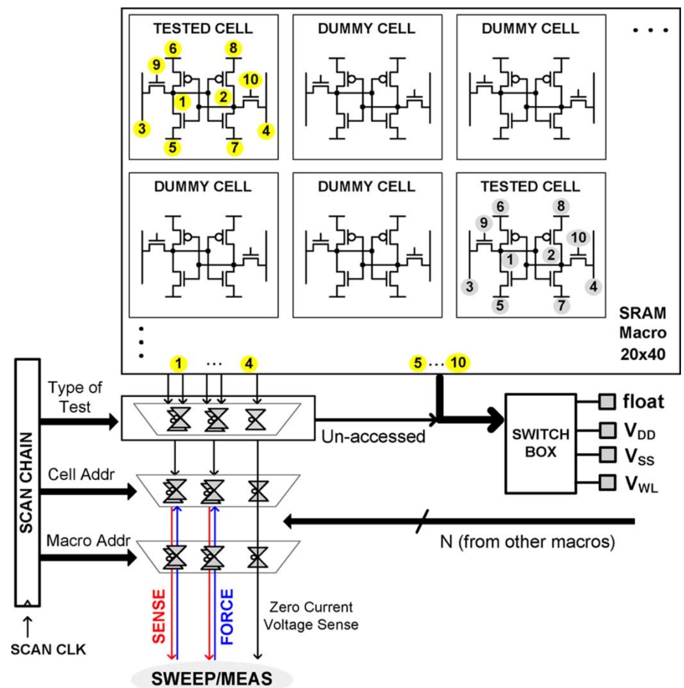


Fig. 6. Measurement macro for padded-out SRAM cells.

guaranteed through appropriate design margins against various failure modes. An array fails if any of its cells cannot be written, loses the value during the read, or cannot retain the value in standby.

Traditionally, SRAM design margins have been estimated through SPICE and TCAD simulations for each of the failure modes. However, as processes become increasingly complex and harder to control, along with the reduced device geometries, designers can no longer rely on model accuracy to fully capture the random effects in large cache memories. Recently, methods have been developed to characterize SRAM variability by measuring dc read/write/retention margins in small SRAM macros with wired-out storage nodes. In these macros SRAM is commonly characterized by measuring the I-V characteristics of its constituent transistors or by characterizing the static read stability or static writability of the SRAM cells [35]. This method requires the insertion of large switch networks to access all internal storage nodes without changing the lithographic environment of the cells, Fig. 6. As a result, this approach is limited to smaller data volumes that may be unsuitable for failure analysis of large cache memory. Recent large-scale 3-D device simulations have demonstrated that even just random dopant fluctuations cause non-Gaussian distributions of transistor threshold voltages in scaled technologies [36], making it difficult to estimate the behavior of cells in the tail of the margin distributions. Conventional padded-out cell characterization techniques fail to characterize many of these effects due to insufficient spatial resolution and small datasets. Large-scale characterization techniques, involving characterization of SRAM cells *in situ* within the array, provide a better estimate of the impact of these systematic effects on SRAM performance. Thus, SRAM designers continue to rely on collecting distributions of bitline read currents [37], [37] and

Fig. 7. Large-scale SRAM margin measurements [34].

Fig. 8. Dynamic SRAM characterization macro [42].

minimum operating voltage (V_{MIN}) [37], [40] to gauge SRAM read stability and writeability in large functional SRAM arrays.

It has been recently demonstrated that read and write margins of a large SRAM array can be measured by bitline current measurements using the setup in Fig. 7, in response to wordline, bitline, and supply voltage sweeps [34]. Distributions of read and write margins correlate well with the distributions of Vmin during read and write. Preserving the structure of the SRAM array allows for collection of orders of magnitude more measured variability data in the same chip area.

However, static margins provide only a partial variability picture needed for robust SRAM design. By its definition, static read margin is pessimistic—it assumes that the cell is under the read stress for an infinitely long time. Conversely, static write margin is overly optimistic, as it allows infinite time for the cell to be written. In practice, wordlines are pulsed for a short amount of time, during which the cells are written and read. There is a recent trend in assessing dynamic SRAM read/write margins, for more accurate estimation of the necessary operating voltages [41].

Fig. 9. SRAM RO for estimating write margins [43].

Dynamic behavior can be characterized by driving the wordlines with variable pulsewidths, Fig. 8. [42]. Shorter pulse widths result in decreased read and increased write failure rates. This method of characterizing the dynamic SRAM behavior is fairly compact and could be even embedded in practical arrays. Another method for characterizing the dynamic SRAM behavior is through the use of ring oscillators [43], [44]. A tunable ring oscillator can be connected to the bitlines; its oscillating frequency would vary with each cell selected through the WL and connected within the RO to assess variability in cell currents. An example RO for characterizing write margins is shown in Fig. 9 [43].

Repeated measurements using many of the presented structures can be used for characterizing the time-dependent variability of the SRAM characteristics. Simple repetitions of the measurements under the same conditions expose the effects of RTS noise. Measurements under increased supply voltage and elevated temperatures reveal the impact of BTI.

SRAM design in the presence of RTS noise therefore requires accurate characterization of the statistical distributions of V_{th} fluctuation, applied to a statistical model of SRAM failure, in order to budget design margins appropriately. Enhanced characterization techniques have been proposed to speed up significantly the measurement of these statistical distributions [45].

IV. Systematic and Random Variations in Logic

The goal of logic variability studies is to improve the understanding of the nature of variability, and to help classification into random and systematic components, including spatial and temporal correlations.

Many systematic variations in process can be exposed by varying circuit layouts. A set of examples of varying inverter layouts shown in Fig. 10, experiments with effects of gate proximity, and impact of STI or diffusion area on channel mobility. Frequency and leakage current measurements collected on ring these oscillators from two 45 nm experimental wafers showed significant across wafer and systematic, layout-depended variations [4]. Fig. 11 shows a spatial wafer map of the die averages of ring oscillator frequency (specifically for the layout P2 from Fig. 10) and the log scale off-state leakage current for NMOS and PMOS transistors of same design as in the ring oscillators. It has been found that the RO frequency and the log scale leakage currents are highly correlated to each other, as illustrated in Fig. 12, and thus can all be very well approximated by a 2-D second-order polynomial function, with a reasonable quality of fit. The two experimental wafers, though subject to an intentional process split mainly in gate CD, share a similar across-wafer spatial signature, shown in Fig. 14, which is the

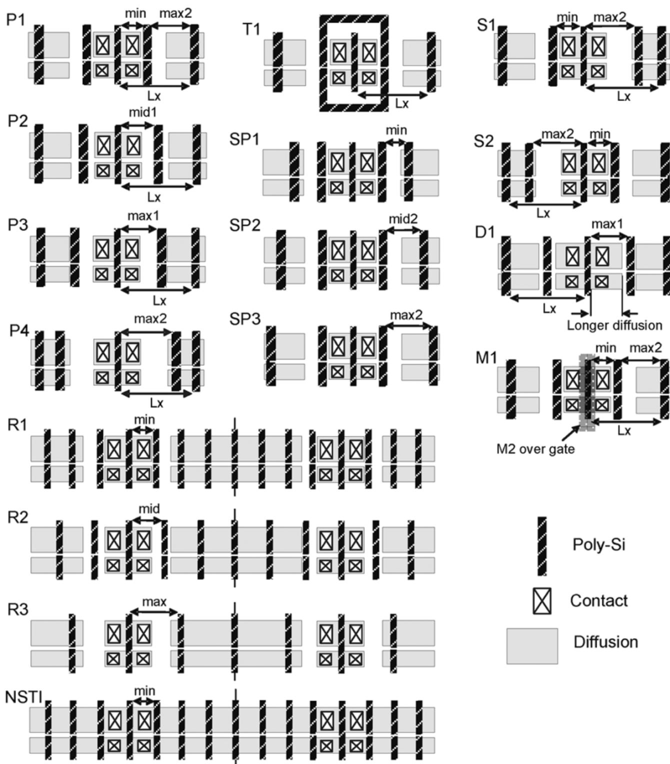
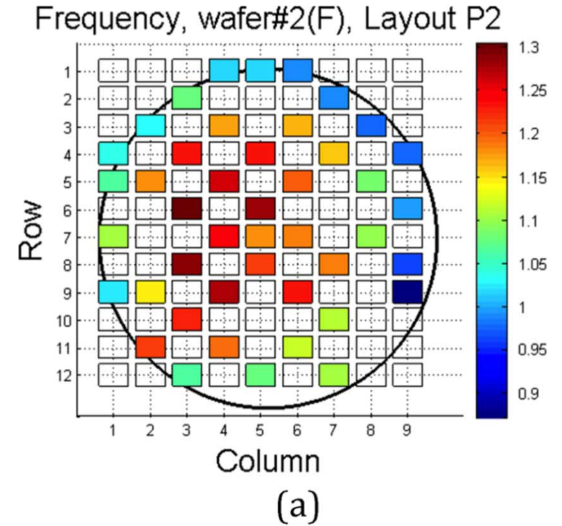
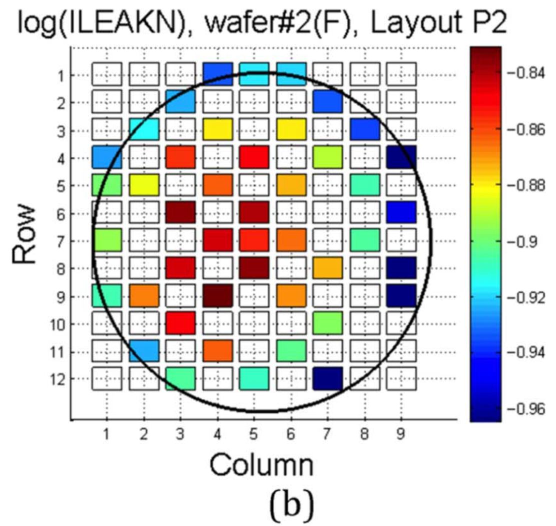


Fig. 10. Various layout patterns in 45 nm ring oscillator design.





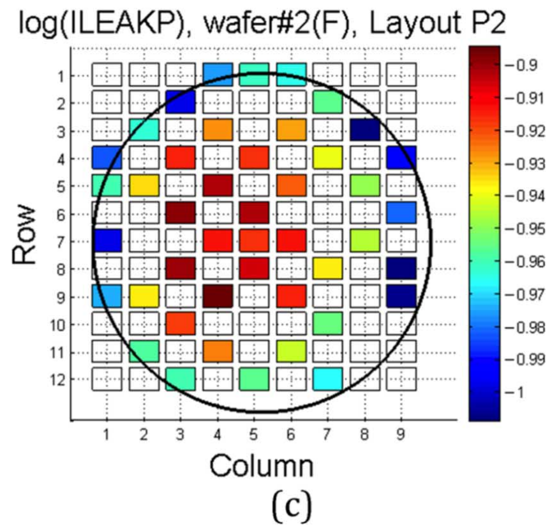


Fig. 11. Spatial map of ring oscillator frequencies and leakage currents for layout P2 from Fig. 10, wafer #2. (a) Die average RO frequency. (b) Die average log (NMOS leakage). (c) Die average log (PMOS leakage).

shape of a dome (Fig. 11). Once the across-wafer systematic function is fitted and removed from either frequency or leakage current data, the die-to-die residuals become relatively small and can be approximated by Gaussian random variables, illustrated in Fig. 16. From a process perspective, the consistent and significant across-wafer signature suggests a bowl-shaped gate CD wafer profile in this manufacturing process, which is confirmed by electrical CD measurement from the foundry.

Another major source of systematic variability comes from the layout pattern dependency. As illustrated in Fig. 15, the ring oscillator frequency and $\log(\mathrm{I_{LEAK}})$ are normalized to its corresponding die mean value before averaged over the whole wafer. There is a clear trend in the layout dependency shared between the RO frequency and $\log(\mathrm{I_{LEAKN}})$, while $\log(\mathrm{I_{LEAKP}})$ has a different pattern and less variations. Given that NMOS and PMOS devices share the same poly gate, and that NMOS mobility is subject to stress enhancement while PMOS is not, it can be reasonably inferred that the layout dependency is not the result of lithographic nonidealities (which seem to be well under controlled by OPC features), but from the layout-dependent stress effect.

Finally, there is little systematic spatial pattern within each die (Fig. 13), which results in very weak spatial correlations. This can be explained by the fact that the overall area of the RO array, is small in this experiment, thus not much spatial gradient can be captured by the test chips. After removal of die averages, the resulting residuals are almost independent of the die average speed/leakage, and can be very well described as simple independent Gaussian random variables.

Efficient energy management often relies on operating chips under dynamically varying supply or threshold voltages. The required supply voltage to maintain the required frequency of operation is maintained by monitoring the supply/substrate voltage controlled set of critical path replicas. These replicas attempt to minimize the additive design margin in this system by tracking

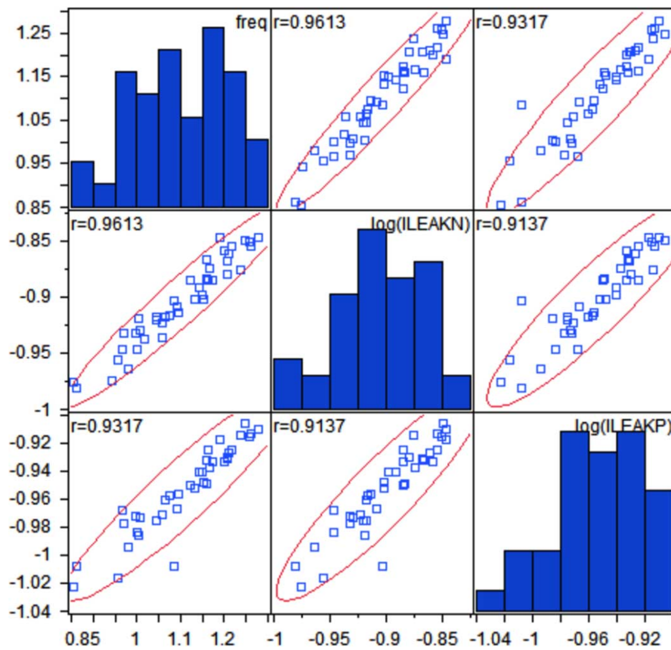


Fig. 12. Correlation among die average RO frequency, $\log(I_{LEAKN})$ and $\log(I_{LEAKP})$, for wafer #2 and layout P2 from Fig. 10.

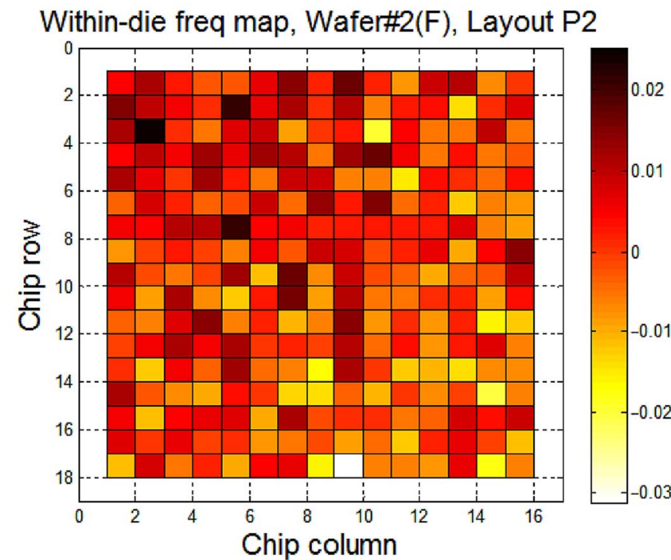
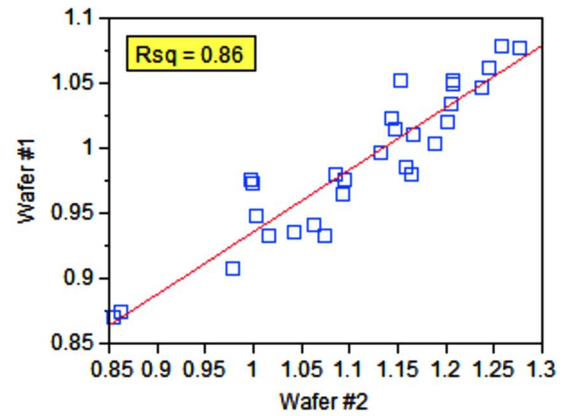
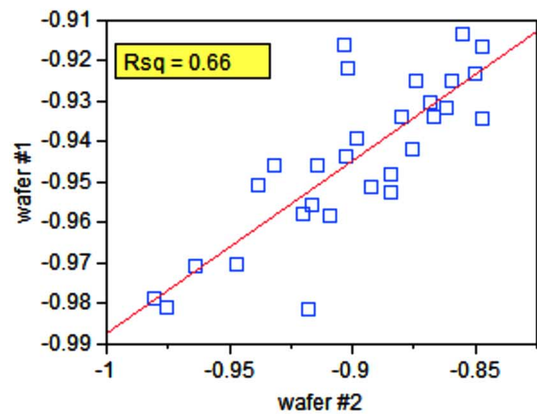


Fig. 13. Within-die RO frequency map of layout pattern P2, averaged over all dies in wafer #2.





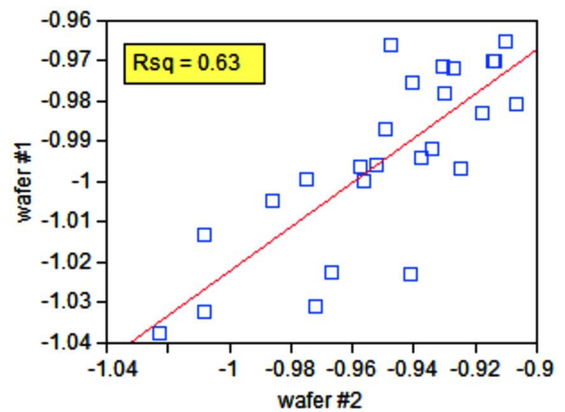


Fig. 14. Correlation between the same die location of the two experimental wafers. (a) Die average RO frequency. (b) Die average $\log(I_{LEAKN})$. (c) Die average $\log(I_{LEAKP})$.

the most likely critical path for the particular supply voltage in the given design corner. The mix of critical paths must be sufficient to identify the slowest path at each supply voltage, and is often composed by mixing the NAND2 NAND3, NOR2 gates, inverters, interconnect, and pass-gates [55].

Measurements have shown that standard deviation of the delay variability varies with the number of transistors in the transistor stack, in addition to the overall transistor area shown in Fig. 17 [26].

One interesting direction in future designs is to allocate the margin for random variability dependent on the composition of gates in the critical paths, to reflect this issue.

V. VARIABILITY IN SRAM

Guaranteeing yield for a large array is a challenging statistical optimization problem, even with Gaussian distributions of each transistor's parameters. This is because of the nonlinear dependence of the margins on the transistor parameters. Fig. 18 illustrates the results obtained using characterization macros from Figs. 6 and 7. All distributions are Gaussian near the center, but deviate in the tails, as illustrated in normal probability plots in

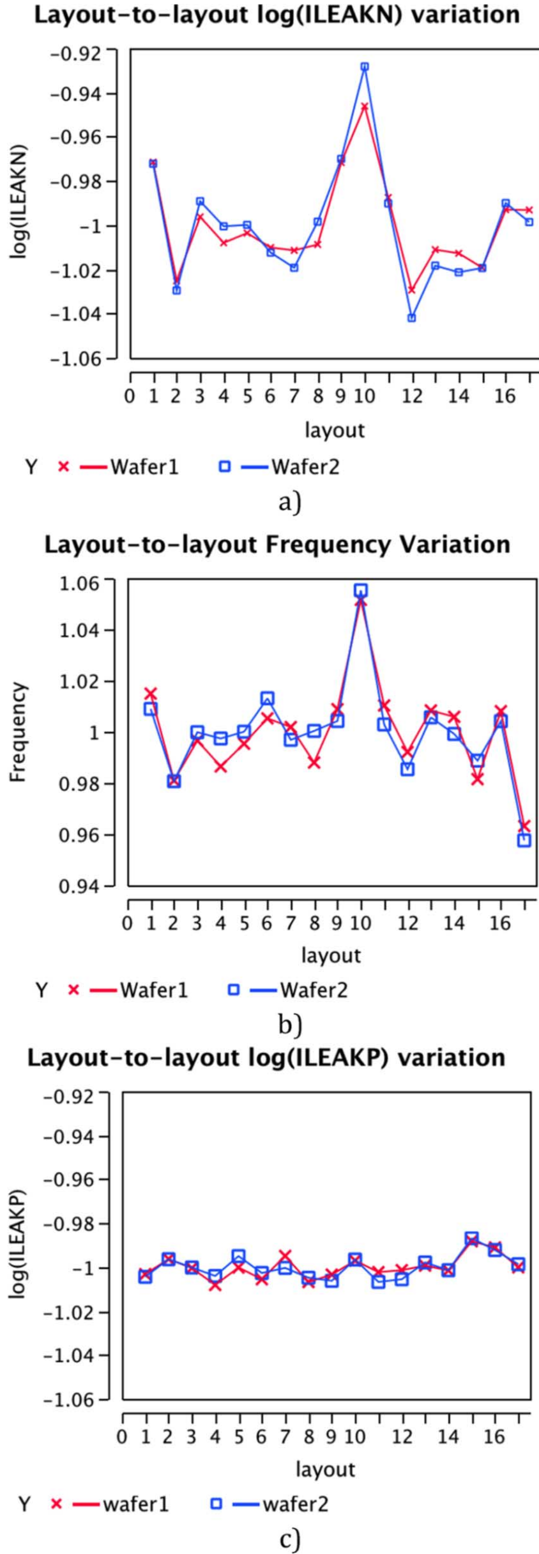


Fig. 15. Mean layout-to-layout variations. (a) Normalized frequency $\overline{fL}_{\bullet,W,P}$. (b) Normalized log NMOS leakage current $\overline{\mathrm{INL}}_{\bullet,W,P}$. (c) Normalized log PMOS leakage current $\overline{\mathrm{IPL}}_{\bullet,W,P}$. Notations here: $\overline{fL}_{D,W,P} \equiv (\bar{f}_{\bullet,D,W,P})/(\bar{f}_{\bullet,D,W,\bullet}), \overline{\mathrm{INL}}_{D,W,P} \equiv (\overline{\log(I_{\mathrm{LEAKN}})}_{\bullet,D,W,P})/(\overline{\log(I_{\mathrm{LEAKN}})}_{\bullet,D,W,\bullet})$, and $\overline{\mathrm{IPL}}_{D,W,P} \equiv (\overline{\log(I_{\mathrm{LEAKN}})}_{\bullet,D,W,P})/(\overline{\log(I_{\mathrm{LEAKN}})}_{\bullet,D,W,\bullet})$.

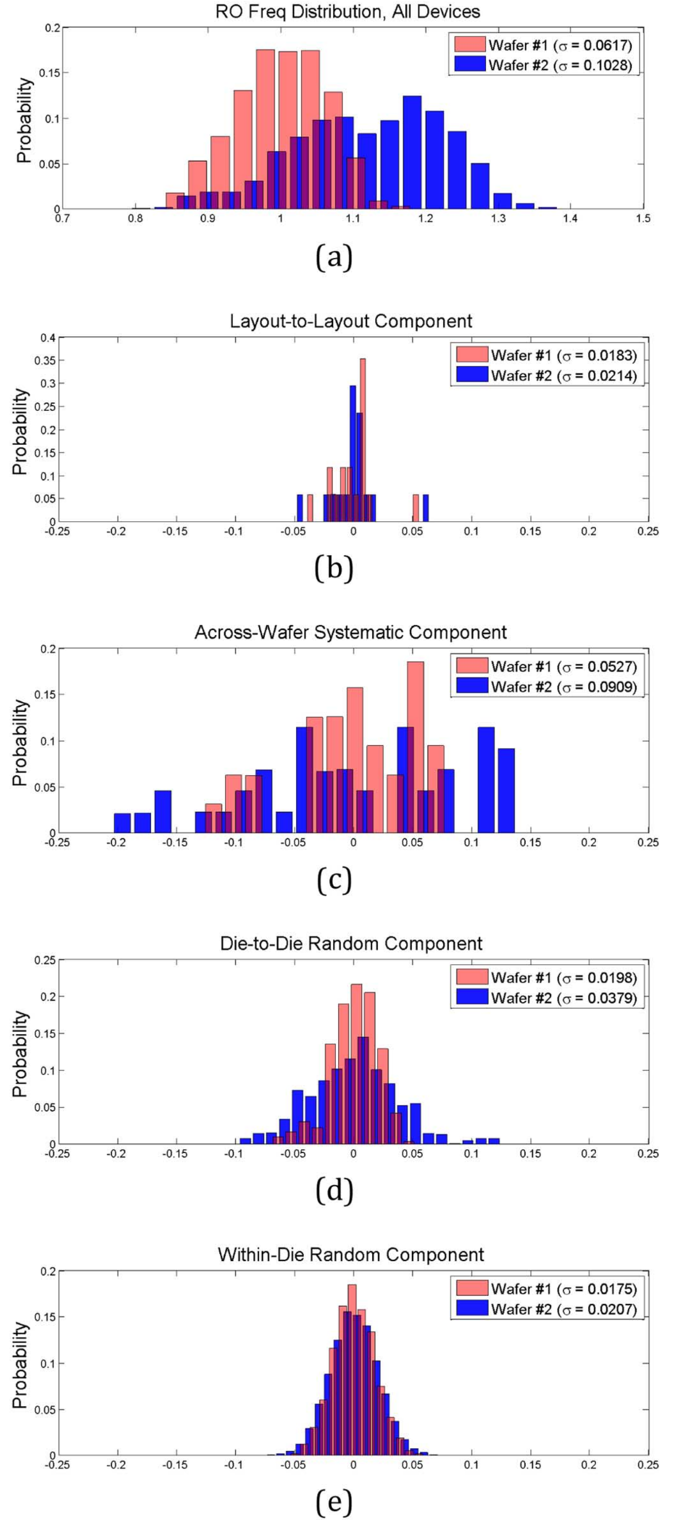


Fig. 16. Variability distribution of: (a) the RO frequency for all devices, and the individual variability components; (b) layout-to-layout; (c) across-wafer systematic; (d) die-to-die random; and (e) within-die random.

Fig. 19. The key parameter often used to qualify a cell, σ/μ, varies with the definition of the margin, and all three write and all three read margins have different σ/μ values. These differences exist because of different setups for evaluating the margins. Each static read or write metric correctly identifies the failure point of the particular cell; however they produce more

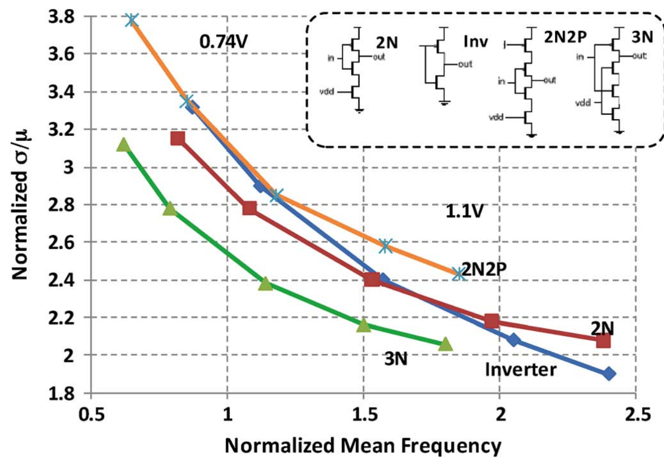


Fig. 17. Increase in standard deviation of variability normalized by the mean ring oscillator frequency, as a function of supply voltage. Numbers indicate different ring-oscillator layouts, with 2 NMOS (2N), 3 NMOS (3N) transistors, and 2 NMOS and 2 PMOS (2N2P) transistors in stack.

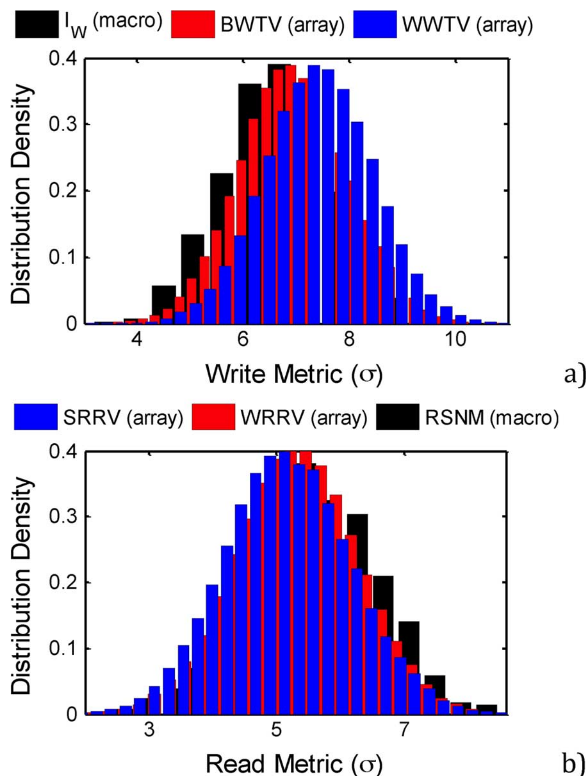


Fig. 18. Distributions of various static read and write metrics measured at low voltages. (a) Write margins, measured on a padded-out macro (IW) and on an SRAM array (BWTV and WWTW). (b) Read margins, measured on a padded-out macro (RSNM) and on an SRAM array (SRRV and WRRV). The metrics are defined in [34].

or less differing values of margins for stable cells, simply because of different cell excitations.

The point of failure for any of the stability criteria can be found by tracing the variables using the steepest gradient method [46], [47]. The method can be accelerated using statistical techniques such as importance sampling [48], [47], [49] and statistical blockade [50].

To improve the read stability or writability in SRAM, the average margin is increased by adjusting one of the terminal voltages. Lowering the column supply voltage or writing with bitline voltages less than 0 V has been used to improve the writability of the cell, meanwhile, lowering the wordline voltage has been demonstrated to improve the read stability while trading off writability.

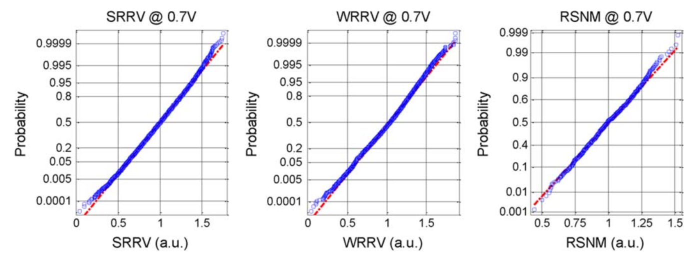


Fig. 19. Illustration of deviation from normality for the three representative SRAM read margins.

While these techniques have been applied at the design time, the design margins can be minimized by tracking the systematic variations in the process. Since the wordline voltage reduction trades off the increased read margin for the reduced write margin, the optimum between the two can be sensed by averaging a number of SRAM cells stressed for both read and write [47].

While all of the current SRAM yield enhancement techniques target systematic components of variability, there is little work in attempting to estimate the tails of distributions. One potentially promising approach is through the use of "canary" cells—cells that are designed to fail before any of the cells in the array [51].

Time-dependent degradation in transistor performance due to BTI is also a major concern in SRAM. In contrast to logic circuits which typically face alternating input logic levels, SRAM transistors face the worst BTI conditions when a cell stores a constant value—a dc bias is applied to the transistors for a prolonged period of time. The fact that BTI affects both NMOS and PMOS devices in high-k processes makes SRAM V_{DD} margin setting more complex because $V_{DD,min}$ degrades at different rates depending on whether the original $V_{DD,min}$ distribution was read- or write-margin limited.

RTS noise is a significant concern in SRAM design involving highly scaled transistors, as its magnitude scales faster than the RDF-induced variations. However, experimental results indicate that while large RTS noise magnitude is present in SRAM transistors, the additional margin needed to compensate for RTS is actually much smaller. This is due to the fact that when convolving a long-tailed distribution (RTS) with a normal distribution (RDF), the outliers in the long-tailed distribution have a low probability of being the most probable failure point in the design [45]. Furthermore, both theoretical and experimental analyses suggest that at least some components of RTS noise and BTI stem from the same traps, and therefore should be included in the same margin [52].

Fig. 20(a) shows that there are no significant spatially correlated effects in SRAM NMOS pull-down currents, which will result in random distribution of static noise margins. Similarly, there is no significant spatial correlation in the distribution of the magnitude of random telegraph noise, shown in Fig. 20(b).

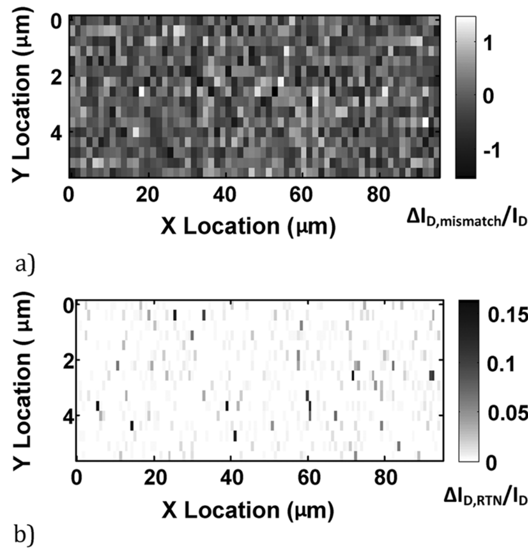


Fig. 20. Spatial distribution of variability in an SRAM array. (a) Mismatch in pull-down drain currents. (b) Random telegraph noise magnitude.

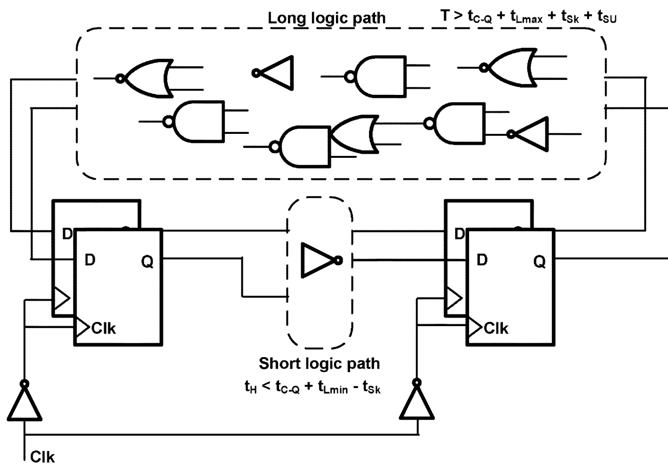


Fig. 21. Illustration of short and long logic paths.

VI. Impact on Digital Logic

Digital logic typically utilizes larger devices than SRAM, which results in lower random variation per gate and a reduction in impact of some of the components of systematic variability. Furthermore, long critical paths in digital logic naturally average random, spatially uncorrelated variations. As a result, longer critical paths reduce the impact of random variability; the σ/μ of random variability roughly decreases with $\sqrt{\mathrm{N}}$, where the N is the number of gates in the path. Longest paths in a circuit need to meet the setup time requirement for the receiving flip-flop, which need to be margined appropriately, as illustrated in Fig. 21. Shortest paths need to be margined for avoiding the hold time violations. Hold margins are often dictated by the timing mismatches between individual gates and are not reduced through averaging. Systematic and spatially correlated variations are not averaged and σ/μ is independent of the logic depth. The hold time margin is essentially dictated by the mismatch in the delays of clock buffers and a Clk-Q path of the flip-flop, which is shown in Fig. 22.

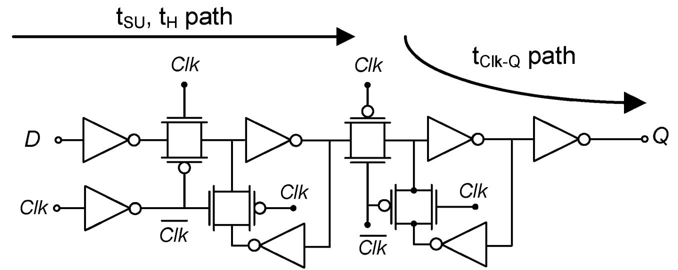


Fig. 22. Illustration of delays that correspond to setup, hold times and clock-to-output delays in a typical flip-flop.

In a typical VLSI design process, satisfying design corners is deemed necessary and assumed sufficient to validate a design. This approach typically regards all variations as D2D, with all devices on a chip having identical process parameters. WID spatial correlations between the clock and data timing paths present an opportunity for reduction in setup time margin. Measurements in earlier technology nodes revealed spatial correlation radii of approximately 1 mm [18], [19]. These correlations are caused by systematic processing effects; however, they are not modeled and therefore appear as random, with a certain degree of spatial correlation [61]. These spatial correlations are of the order of the size of a typical digital block, which makes many paths inside a block partially correlated, allowing for some reduction in margins. However, measurements in 45 nm technology reveal negligible spatial correlations at the block level [4]. This is caused by: 1) improvements in processing technologies; 2) reduced gate sizing, which increases true random variability, potentially masking the spatially correlated component. It is believed, however, that the reticle-level spatial effects are still present [7]. These effects can be used to establish timing correlations for interblock data and clock distributions in timing analysis.

Spatial, processing-induced correlations are not the only ones present in the chip. Layout-induced variations are common for all gates with the same topology or with the same neighborhood, and are therefore systematic. However, since many of the effects are not modeled, they appear to the designer as random. They can be corrected by better processing, accounted for during circuit extraction from the layout and acknowledged in the models, or can be treated statistically in the timing analysis.

Flip-flops are topologically the most complex cells in a standard-cell library. Variability affects their clock-to-output delay, setup and hold times in a partially correlated way, since some of the transistors are shared between these timing paths, as illustrated in Fig. 22. The variability of these gates is proportional to the stack height, not unlike complex combinatorial gates. As a result, flip-flops often limit minimum operating voltage of digital logic [60].

Traditionally, correct functioning of digital logic is verified by using static timing analysis (STA), which checks if all timing paths meet their setup and hold requirements. This is accomplished by building a directed graph that corresponds to the analyzed circuit, where vertices represent the gates and edges represent the interconnect, each labeled with their respective delays. By using a breadth-first algorithm, a timing analysis tool goes through all the nodes of the graph and for each node computes

the maximum of delays from all edges incurring in that node. Simple one time traversal of the graph finds the longest and the shortest path in the circuit. In traditional STA, which is incremental in nature, early and late signal arrivals depend only on the circuit topology; however, to correctly account for variability all delays have to have a lower and an upper bound. To account for variability in STA, this verification has been performed in multiple process corners. However, the closest point of failure does not necessarily correspond to one of the traditional corners; as a result, the number of process corners for design verification has been increasing.

Multicorner STA may introduce artificially large margins in the design. When treating the signal delays as intervals in STA and performing timing analysis with the worst case delays (i.e., taking the lower delay bound for the early signals and the upper delay bound for the late signals) conventional STA cannot distinguish the fact that two paths can have common or correlated part; the common part will be treated as having both, the lower and upper delay bound at the same time. The common-path pessimism removal (CPPR) technique and its generalization [58], [59], alleviate the pessimism of common or spatially correlated paths. For each critical path with a slack still bellow the critical value, additional correlated path delay difference is applied. The delays are expressed as functions of parameters, explicitly showing variations. For each corner, each parameter has a shared global value and an individual local value. One of the main drawbacks of the CPPR technique is its polynomial computational time.

An alternative approach for timing analysis is statistical STA (SSTA). In particular, block-based SSTA tries to recover linear run-time complexity, identification of a critical path and incremental nature of a traditional STA [57]. In SSTA, process parameters are considered to be random variables. A canonical first-order delay model is employed for all timing quantities, consisting of the nominal delay value, and global and local process variations, multiplied by their respective sensitivities. When all delays are represented in the canonical form, graph can be traversed in an STA fashion by using a breath-first search. The graph traversal will result in the paths enumerated in the order of critical probability. A spatial correlation factor can be added to the canonical form as well.

Another way of accounting for systematic and random variability is by adjusting the operating supply and frequency by monitoring a replica of critical path delays [54]. To account for dependences in variability of different gate topologies on the supply voltage, an appropriate mix of gates should compose the set of critical and near-critical path replicas [55]. In contrast, it is possible to monitor the timing violations on a set of actual critical paths using shadow latches [62].

VII. Conclusion

Variability limits the lowest operating voltage for a technology. This presents a challenge for continued scaling, where one of the major scenarios relies on continued improvements in energy efficiency of multicore processors through voltage scaling. To overcome voltage scaling barriers, variability characterization needs to be extended to enable compact, *in situ* energy and performance monitoring of logic and memory blocks. Continued improvement in design techniques, which incorporate mitigation of the effects of variability, in addition to continuous performance monitoring would enable operation of high-volume products at near-threshold supplies.

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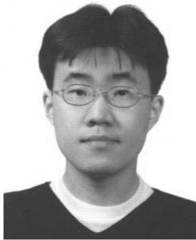
Borivoje Nikolić (S'93-M'99-SM'05) received the Dipl.Ing. and M.Sc. degrees in electrical engineering from the University of Belgrade, Serbia, in 1992 and 1994, respectively, and the Ph.D. degree from the University of California at Davis in 1999.

He lectured electronics courses at the University of Belgrade from 1992 to 1996. He spent two years with Silicon Systems, Inc., Texas Instruments Storage Products Group, San Jose, CA, working on disk-drive signal processing electronics. In 1999, he joined the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, where he is now a Professor. He is coauthor of *Digital Integrated Circuits: A Design Perspective* (2nd ed., Prentice-Hall, 2003). His research activities include digital and analog integrated circuit design and VLSI implementation of communications and signal processing algorithms.

Dr. Nikolić received the NSF CAREER award in 2003, College of Engineering Best Doctoral Dissertation Prize and Anil K. Jain Prize for the Best Doctoral Dissertation in Electrical and Computer Engineering at University of California at Davis in 1999, as well as the City of Belgrade Award for the Best Diploma Thesis in 1992. For work with his students and colleagues he received the best paper awards at the ISSCC, Symposium on VLSI Circuits, ISLPED, and the International SOI Conference.



Ji-Hoon Park (S'06) received his B.S. and M.S. degrees in electrical engineering from Seoul National University, Korea, in 1998 and 2000, respectively. He is currently working toward the Ph.D. degree at the University of California at Berkeley.

From 2000 to 2005, he was with LG Electronics, Korea, where he worked on the design and verification of WCDMA base stations and GSM modems. His current research interests include the variability measurement and the design of multi-Gb/s wireless receivers.

Mr. Park was a recipient of Samsung Scholarship from 2005 to 2009.

Jaehwa Kwak received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea in 2004 and 2006, respectively. He is currently working toward the Ph.D. degree at the University of California, Berkeley.

From 2004 to 2006, he was a Graduate Student Researcher with the Integrated Systems Design Laboratory, Seoul National University, where he worked on the ethernet switch architecture and the bandwidth provision of broadband access networks. In 2006, he joined GCT Research, Inc. (also known as GCT Semiconductor, Inc.), Seoul, where he was a staff engineer in charge of designing digital system architectures for the wireless networks. Since 2009, he has been with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley. His research interests are in the areas of low power process architectures and error detection techniques of the synchronous digital systems.

Bastien Giraud received the M.S. degree from Institut Supérieur d'Electronique et du Numérique (ISEN), France, and Polytechnique Marseille, France, in electrical engineering in 2005 and the Ph.D. degree from Ecole Nationale Supérieure des Télécommunications (ENST), Paris, France, in 2008. His Ph.D. thesis was realized in the laboratories of Institut Supérieur d'Electronique de Paris (ISEP) in cooperation with CEA/Leti (France), and was part of a French multi-laboratories project funded by the ANR (National Research Agency). It is based on IC design about SRAM memory in Double Gate fully depleted silicon-on-insulator sub-32 nm technology, in which in-depth studies of SRAM memory cells and sense amplifiers have been conducted..

In 2005, he interned at IMEC, Belgium, where he studied SRAM memory architecture in Bulk-130n. In 2009, he spent one year as a postdoctoral researcher position at University of California, Berkeley, in the Berkeley Wireless Research Center (BWRC) laboratories under the supervision of Prof. Nikolic. His research interests were in logic circuits and SRAM variability in Bulk 45 nm. Since 2010, he has worked at CEA-Leti, Grenoble, France, as an IC design research engineer. His research interests include large range frequency digital and SRAM circuit design, dynamic multi-Vt, Bulk IP porting in FD-SOI technology.

Zheng Guo (S'03-M'09) received the B.S. degree in computer engineering from the University of Illinois at Urbana-Champaign in 2003 and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley in 2005 and 2009, respectively. His Ph.D. research emphasis was on variability characterization and robust design techniques for nanoscale SRAM.

He attended the University of California at Berkeley in the fall of 2003. There, he joined the Berkeley Wireless Research Center in 2004 as a Graduate Student Researcher under the supervision of Professor Borivoje Nikolić. Upon completion of his Ph.D. program, he joined Intel, Hillsboro, OR, in early 2010 as an SRAM technologist.

Dr. Guo was awarded the National Defense Science and Engineering Graduate (NDSEG) Fellowship in 2004. In 2005, he received the Best Paper Award at the ACM/IEEE International Symposium of Low-Power Electronics. In 2009, his research work was recognized as a winner in the 46th DAC/ISSCC Student Design Contest.

Liang-Teck Pang (S'02-M'08) received the Dipl.Ing. degree from Ecole Centrale de Paris, France, the M.Phil. degree from Cambridge University, U.K., in 1997, and the Ph.D. degree in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley, in 2008. His Ph.D. research involved the design of circuits to measure and characterize CMOS performance variability due to fluctuations in the manufacturing process.

Between 1998 and 2002, he worked in the DSO National Labs in Singapore on VLSI implementation of signal processing algorithms and high performance microarchitecture and circuit design. In 2008, he joined IBM T. J. Watson Research Center, Yorktown Heights, NY, as a research staff member. His research emphasis is on the effects of layout on CMOS performance, measurement of the spatial correlation of logic gates, and analysis of variability data. Currently in IBM, his research focus is in clocking of high performance VLSI chips and 3-D chip design.

Seng Oon Toh received the B.S. degree (highest honors) in computer engineering from the Georgia Institute of Technology, Atlanta, in 2002, the M.S. degree in electrical engineering from the University of California at Berkeley in 2008. He is currently working toward the Ph.D. degree at the University of California at Berkeley.

He is also currently working at Advanced Micro Devices, Sunnyvale, CA, on process technology development. His research emphasis is on power-performance optimization as well as robust design of nanoscale SRAM, with emphasis on dynamic stability, RTS, and BTI.

Mr. Toh was awarded an IBM Ph.D. fellowship in 2010 and won the DAC/ISSCC student design contest in 2011.

Ruzica Jevtić received the B.S. degree in electrical engineering from the University of Belgrade, Serbia, in 2004 and the Ph.D. degree in electrical engineering with European Ph.D. mention from the Technical University of Madrid, Spain, in 2009. Her Ph.D. work was oriented towards CAD tools for high-level modeling, power estimation, measurements, and architecture design for high-speed computational systems in FPGAs.

She was a Predoctoral Visiting Researcher at the OFFIS Research Institute in Oldenburg, Germany, in 2007. She is currently working as a Postdoctoral Researcher at the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley. Her current research interests are in energy efficient microprocessor design.

Dr. Jevtić is a recipient of FP7 Marie Curie International Outgoing Fellowship.

Kun Qian (S'05) received the B.S. degree from Department of Microelectronics, Peking University, Beijing, China, in 2005. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, under the guidance of Prof. Costas J. Spanos.

Between 2003 and 2005 he did his undergrad research with the Novel Devices Research Group of Institute of Microelectronics at PKU, which involves modeling of high-K dielectric based nonvolatile memory devices. His Ph.D. research is focused on characterization, analysis, and modeling of integrated circuit manufacturing process and performance variability, and the robust and accurate statistical extraction of compact model parameters. He is also interested in general design for manufacturability techniques.

Costas J. Spanos (F'00) received the Electrical Engineering Diploma degree from the National Technical University of Athens, Greece, in 1980 and the M.S. and Ph.D. degrees in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, in 1981 and 1985, respectively.

From 1985 to 1988 he was with the advanced Computer-Aided Design Group of Digital Equipment Corporation, where he worked on the statistical characterization, simulation, and diagnosis of VLSI processes. In 1988 he joined the Faculty at the department of Electrical Engineering and Computer Sciences of the University of California at Berkeley, where he is now a Professor. He was the Director of the Berkeley Microfabrication Laboratory from 1994 to 2000, the Director of the Electronics Research Laboratory from 2004 to 2005, and the Associate Dean for Research in the College of Engineering from 2004 to 2008. He is presently the Department Chair of EECS at UC Berkeley. His present research interests include the application of statistical analysis in the design and fabrication of integrated circuits, and the development and deployment of novel sensors and computer-aided techniques in semiconductor manufacturing. He is also working towards the deployment of information technology and statistical data mining techniques for energy efficiency applications.

Prof. Spanos has served in the technical committees of numerous conferences and was the editor of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING from 1991 to 1994. In 2009 he was appointed in the Andrew S. Grove Distinguished Professorship in the Department of EECS.