Low-Power Inductorless RF Receiver Front-End with IIP2 Calibration through Body Bias Control in 28nm UTBB FDSOI

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***Abstract*— A compact energy-efficient receiver front-end designed and implemented in 28nm UTBB FDSOI CMOS supports in-device coexistence of Bluetooth (BT) with an LTE FDD Band 7 transmitter module. The receiver is based on an inductorless low-IF current-mode LNTA-first architecture and features IIP2 calibration. IIP2 improvement is implemented through the body bias of the passive mixer switching pairs. The fabricated receiver has an active area of 0.12mm^2, power consumption of 4.4mW, achieves IIP2 improvement of over 25dB through body bias tuning, NF of 8.6dB and gain of 26.7dB, all within BT specification.**

***Index Terms*— FDSOI, Bluetooth, current-mode receiver, low-power, second-order intercept point (IIP2), passive mixer, noise.**

I. Introduction

Emerging connected devices must support coexistence with other wireless systems to enable dense deployment. IoT devices are expected to be connected by using both machine-to-machine modes of cellular systems and local-area wireless operating in the unlicensed bands such as Bluetooth LE and Zigbee and require very low power consumption.

Opening up the new LTE bands that surround the ISM band – Band 7 and Band 40, increases the residual interference from cellular on the unlicensed radios. A BT radio intended for use on the same platforms with cellular transceivers needs to coexist with the other cellular radios. Such a radio is integrated on a SoC, and therefore needs to be implemented in a scaled 'digital' technology node, with the minimum external bulky components such as inductors and relaxed requirements for off-chip filters.

Recent open research addresses receiver architectures with a goal of supporting multi-mode operation and coexistence while minimizing the external component count. Notable architectures include the LNTA-first [1], mixer first and noise cancelling [2]. These implementations can achieve excellent noise, linearity and blocker resilience performance on one hand, but are often complex and can consume high power. In contrast, the reported low-power BT receivers compromise the coexistence requirements.

This paper presents an LNTA-first receiver design that supports LTE coexistence, while minimizing area by excluding bulky passives and optimizing the power.

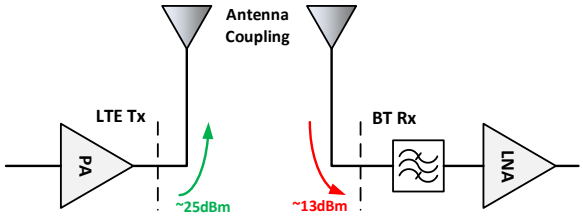

Fig. 1. Antenna to antenna isolation in the system

II. System Considerations

The in-device coexistence scenario between BT receiver and the LTE FDD Band 7 (2.5-2.57GHz) is considered more critical than from the TDD Band 40 (2.3-2.4GHz), because in the TDD case it is possible to avoid interference by scheduling transmissions. Fig. 1 shows this system where antenna-to-antenna isolation inside the same mobile device is estimated to be 12dB therefore having 13dBm LTE blocker at the BT receiver input. Band 40 is only 20MHz away from the highest BT channel requiring strong off-chip filtering.

The residual blocker can affect the receiver in two ways. First, the saturation of the receiver is characterized by the compression point (P1dB) at blocker frequency. The specification of P1dB depends on the blocker power and the amount of filtering:

$$P1dB(f_{blocker}) > P_{blocker} - |Filter\_Attenuation\ (f_{blocker})|.$$

Second is receiver desensitization due to the noise figure degradation caused by the circuit nonlinearities. The noise budget for the required sensitivity needs to be larger than the sum of all contributing components.

The target system specifications are based on 45dB off-chip filtering at 2.5GHz for -90dBm sensitivity and achieved by an iterative optimization loop, and the resulting requirements are shown in the last column of Table I. To summarize, it is required to have compact inductorless, low power solution with a high IIP2 performance and a good noise figure.

III. Receiver Architecture

To achieve the target objectives, a low-IF LNTA-first architecture was chosen for implementation. This architecture is characterized by a favorable noise-linearity

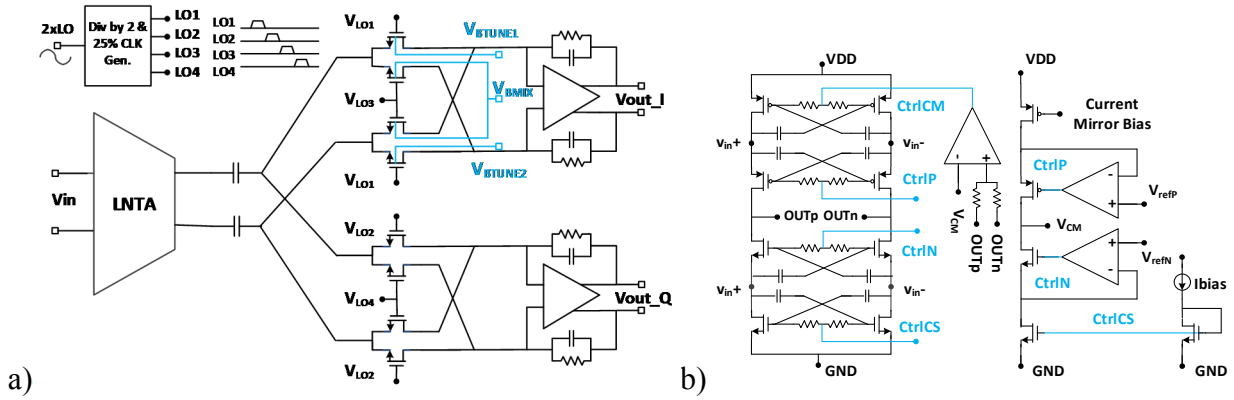

Fig. 2 a) Receiver architecture b) LNTA and its biasing scheme

compromise and the potential for low power consumption. The schematic of the receiver front-end is shown in Fig. 2a, and consist of the LNTA, a passive mixer and baseband filter.

A. LNTA

A common-gate LNTA has been chosen to provide input matching and enable broadband operation, so multiple systems can be supported. In this receiver, the LNTA noise is the major contributor to the system noise and, therefore is the major candidate for optimization. A cross-coupled common-gate LNTA is chosen based on a comprehensive theoretical design considerations [3].

The LNTA is implemented with a common-gate input stage for inductorless input-matching (Fig. 2b). Cross-coupled capacitors across the input transistors are used to boost g_m and therefore reduce the noise and power consumption. Complementary NMOS-PMOS structure renders the output signal more linear with respect to the input swing. Cross coupling of the current sources to the input partially cancels the thermal noise from the input devices. This cancelation is done with respect to the gain of the amplifier and the noise performance of the complete receiver chain [3].

Fig. 2b shows the biasing section of the LNTA. Conceptually, it provides equal drain-to-source voltage over each pair of transistors, $V_{DS}=V_{DD}/4$ for maximizing the input voltage swing. Biasing of the amplifier is implemented via three mechanisms:

- *Current mirror bias* is applied on the NMOS current sources (CtrlCS). This means that the current through the amplifier branches is controlled by this transistor pair.
- *Common-mode control*: In order to establish the output common-mode voltage equal to $V_{DD}/2$ (V_{CM}), the PMOS current sources are biased through the common-mode control loop (CtrlCM).
- *Replica biasing*: The replica circuit mimics one branch of the amplifier and provides biasing for input devices. Current through the replica is set by the same current mirror, the voltage on the drains of corresponding devices is directly set to $V_{CM}=V_{DD}/2$ and the biasing is provided through the negative feedback loop which sets $V_{DS}=V_{DD}/4$. Biasing of the replica devices (CtrlN, CtrlP) is further applied to the amplifier input devices. In Fig. 2b, $V_{refN}=V_{DD}/4$ and $V_{refP}=3V_{DD}/4$.

B. Passive Mixer

The LNTA is followed by 25% duty cycle passive mixers in I and Q paths. One of the two switching pairs in the passive mixer has been used to compensate the mismatch in the rest of the chain. The compensation is done directly in the switching pair itself through the body bias node of the FDSOI device by counter-balancing mismatch accumulated in the other blocks. This is explained in detail in Section IV.

C. Other Blocks

The baseband part is implemented as a simple trans-impedance amplifier (TIA) whose main role is to convert baseband current to output voltage, while preserving the performance of the preceding blocks. The TIA consists of an operational amplifier in a negative RC feedback loop providing this way the first order filtering and low input impedance. The amplifier is implemented as a two stage Miller amplifier with common-mode feedback loop. It is designed such that in the required pass-band frequency range it has a large gain in order not to degrade the transfer function of the TIA. Since this is a current mode architecture, complete voltage gain is implemented at the output of the chain, which is at the same time the output of the operational amplifier. Therefore the amplifier has to be able to handle enough output voltage swing.

An on-chip frequency divider generates the 25% duty cycle clock phases from an external oscillator, which is running at double frequency, at 4.8GHz. These signals are driving the mixer switches through a properly sized chain of inverters in order to minimize the power consumption. The divider consists of two latches in a master-slave

configuration with negative feedback. This structure provides 25% duty cycle phases directly at the outputs by using the latch proposed in [4].

IV. IIP2 Tuning by Body Biasing

A cross-section of LVT 28nm FDSOI CMOS transistor is shown in Fig.3a. Due to the channel isolation from the substrate, bulk-source and bulk-drain junction diodes are eliminated, which allows body biasing over a large voltage range (0 to |3V|). Together with a threshold voltage (V_{th}) sensitivity of 85mV/V to the substrate potential specific only to UTBB FDSOI, it is possible to achieve a large V_{th} variation range (few hundreds of mV). Bulk technology has a sensitivity of only 25mV/V at the 28nm node and body bias voltage range is very limited due to the junction diodes and GIDL (Fig.3b). While the wide range of V_{th} adjustment in FDSOI has been utilized in digital and memory designs for power-performance optimization, there have been very few publications in field of RF and analog design in this technology, exploiting this feature.

The mechanisms of creating a second-order intermodulation (IM2) have been extensively studied in theory [5]. In practice, the dominating mechanism will largely depend on the architecture, design and process technology. In the proposed architecture, IM2 is expected to be dominated by the mismatch between the mixer switching devices. To counter this effect, the IIP2 performance of the receiver is improved by intentionally introducing threshold voltage (V_{th}) mismatch for one switching pair. This will create IM2, which can be tuned to cancel other accumulated second order nonlinearities in the chain. In the implemented receiver this idea is realized by tuning the V_{th} of the switching pair through the body biasing of the respective devices.

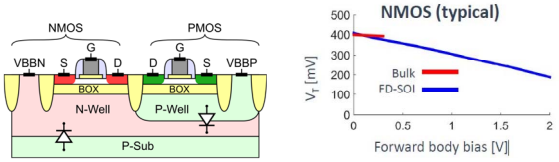

Fig. 3. a) FDSOI transistor b) V_{th} versus back bias voltage

Fig. 2a shows the back gate signal terminals on the passive mixer switches in the I path. V_{Btune1} and V_{Btune2} signals provide the tuning on one pair of the switches in order to calibrate the IIP2 performance. The other pair of switches has a constant body bias voltage of V_{Bmix}=1V. This is also a default voltage value for V_{Btune1} and V_{Btune2} in order to avoid the requirement for negative voltage on these nodes during the calibration. Tuning voltages should be symmetrical with respect to the default value:

$$V_{Btune1}=V_{Bmix}+dV$$
$$V_{Btune2}=V_{Bmix}-dV \qquad -1\text{V}\leq dV\leq 1\text{V}$$

A similar effect can be achieved by tuning the mismatch on the front gate. In this case the front gate does not adjust the threshold voltage but the overdrive voltage $V_{OV}=V_{GS}-V_{th}$, which is equivalent in this case. However, tuning on the back gate is better for two reasons. First, sensitivity of the V_{OV} mismatch on changing the V_{th} by back gate (~85mV/V) is smaller than changing the front gate voltage (1V/V). This means that 1mV change on the front gate makes the same change on the V_{OV} mismatch, while 1mV change on the back gate changes V_{OV} around 85µV. Therefore tuning on the back gate can has a better resolution, which is important as IIP2 is very sensitive to

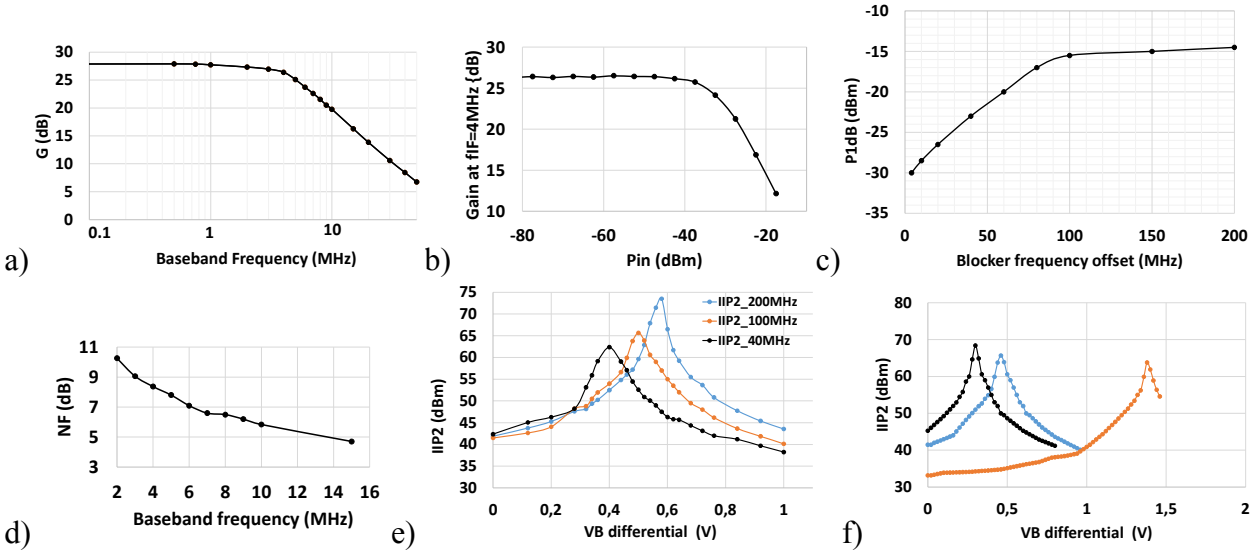

Fig. 4. Bluetooth receiver front-end measured performance a) Receiver gain transfer function b) Gain compression with increasing the input power c) P1dB for different blocker distance d) Noise figure performance e) Calibrated IIP2 for different blocker scenario f) Calibrated IIP2 for different chips

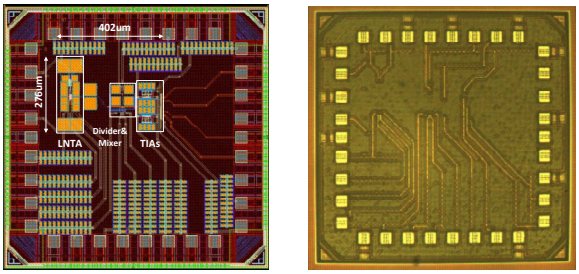

Fig. 5. Chip layout and micro-photograph

mV-level changes of the mismatch. Second, tuning on the back gate is simpler to implement since access to the back gate terminal is direct and it is decoupled by an oxide layer from any signal path, while tuning through the front gate requires decoupling from the LO.

V. Measurement Results

Fig. 5 shows the micrograph of the front-end fabricated in STMicroelectronics 28nm UTBB FDSOI CMOS process. The active area of the chip is 0.12mm^2 and it consumes 4.4mW of power under 1.2V supply.

Fig. 4 a–f shows the measurement results over the receiver, where all off-chip losses are carefully de-embedded. Fig. 4a shows the receiver RF transfer function with the gain of 26.7dB in the pass-band, a corner frequency of 6MHz and 20dB/decade roll-off.

Fig. 4b shows gain compression with varying in-band signal input power. The received signal is at IF frequency of 4MHz and measured P1dB is -33dBm. Fig. 4c shows measured P1dB for different out-of-band blocker signals. Fig. 4d shows measured noise figure. At desired output frequency of 4MHz, measured noise figure of the receiver chain is 8.4dB. Measured S11 magnitude in the required frequency range of 2.4-2.5GHz stays below -10dB.

Finally and specifically to this circuit, Fig.4e and 4f show measured IIP2 calibration by using the body bias voltage tuning. The x axis presents the difference of tuning voltages: $V_{Bdifferential}=V_{Btune1}-V_{Btune2}=2dV$. Tuning was performed with the step of 20mV for VB differential.

TABLE I
Comparison, Measured BT Rx Front-End Performance

	[1]	*[2]*	*[6]*	*[7]*	***This work***	***Specs***
RF freq. [GHz]	1.8-2.4	0.08-2.7	2.4	2.5-2.6	2.4	2.4
Gain [dB]	45.4/44.5	70	42	41	26.7	>25
NF[dB]	3.8/3.1	1.9	6	2.7	8.4	<9
IIP2 [dBm]	66	68	-	>60	**73**	>70
P1dB [dBm]	-	-	-34	-33	-33	~-35
Supply [V]	1.2-1.8	1.3	1.3	1.2V	1.2	1.2
Power [mW]	24.3	31.2	1.95	20	**4.4**	<5
Tech	40	40	65	65	28 FDSOI	28 FDSOI
Area [mm^2]	0.84/0.74	1.2	-	1.45	0.12	min
Inductors	Yes	No	Yes	No	No	No

Fig. 4e shows the calibration of IIP2 for three different blocker scenarios: 40MHz, 100MHz and 200MHz blocker distance from the desired channel. The IIP2 is improved by 20dB, 25dB and 31dB respectively. The response of the chain depends on the frequency, therefore the optimum tuning voltage is different for different blocker frequencies. Fig. 4f shows the IIP2 calibration for three different chips. Mismatch is different from chip to chip, so it is expected that different chips have different optimum point in the sense of tuning voltages. Measured IIP2 improvements for these chips are 23dB, 24dB and 30dB.

Table I shows the summary of measured performance compared to the specifications needed for standard coexistence and to stated references. References [1] and [2] show blocker resilient, low noise solutions but are not suitable for a BT applications due to the high power consumption. A BT receiver optimized for low power [6] does not include blocker considerations addressed in this work, multiple inductors make this design non-scalable and increase the area. A similar approach of IIP2 improvement through the back gates of passive mixer is presented in [7] published after this chip was fabricated. Intended for LTE/WCDMA purpose, it consumes higher power and employs the inductors.

VI. Conclusion

This work demonstrates a low-power receiver front-end fabricated in 28nm UTBB FDSOI for Bluetooth applications, resilient to a co-located LTE Band 7 blocker. The inductorless design results in the active chip area of only 0.12mm^2. This front-end consumes 4.4mW of power, the NF is 8.4dB and IIP2 improvement of over 20dB is achieved, reaching absolute IIP2 values of 73dBm. The UTBB FDSOI technology enables a simple solution for IIP2 calibration of a full RF front-end low-power receiver chain. Besides Bluetooth, this architecture can be applied to the design of a wider range of low-power receivers.

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